256-Kbit (32,768 x 8) Industrial High-Speed Parallel EEPROM

AT28HC256

Features

- Fast Read Access Time: 70 ns
- Automatic Page Write Operation:
  - Internal address and data latches for 64 bytes
  - Internal control timer
- Fast Write Cycle Time:
  - Page Write cycle time: 3 ms or 10 ms maximum
  - 1 to 64-byte Page Write operation
- Low-Power Dissipation:
  - 80 mA active current
  - 3 mA standby current
- Hardware and Software Data Protection
- $\overline{\text{DATA}}$ Polling for End of Write Detection
- High Reliability CMOS Technology:
  - Endurance: 10,000 or 100,000 cycles
  - Data retention: 10 years
- Single 5V ± 10% Supply
- CMOS and TTL Compatible Inputs and Outputs
- JEDEC® Approved Byte-Wide Pinout
- Industrial Temperature Range
- Green (RoHS-compliant) Packaging Option Only

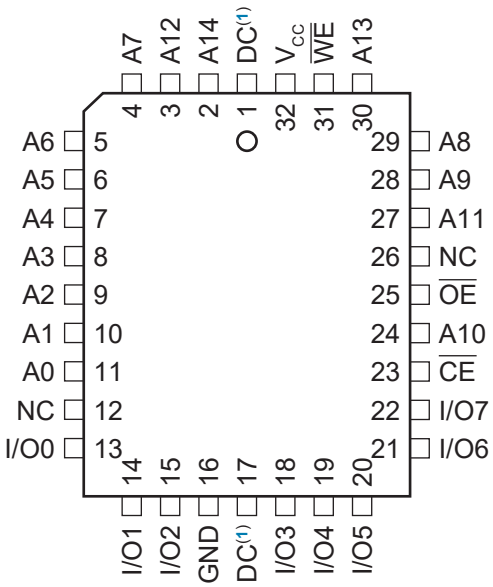
Packages

- 32-Lead PLCC and 28-Lead SOIC

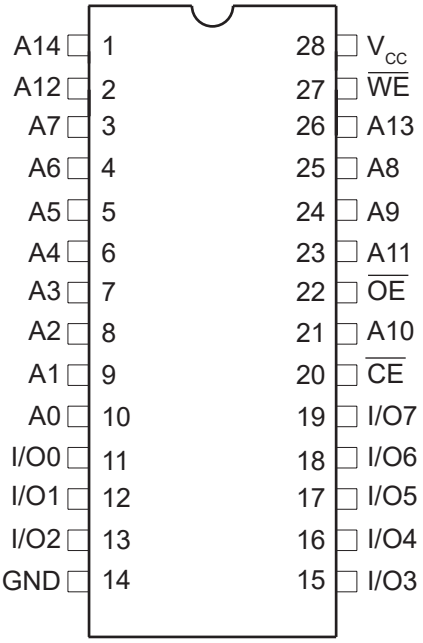
Table of Contents

1. Package Types (not to scale)

32-Lead PLCC
Top View



28-Lead SOIC
Top View



Note 1: PLCC package pins 1 and 17 are “Don’t Connect”.

2. Pin Descriptions

The descriptions of the pins are listed in Table 2-1.

Table 2-1. Pin Function Table

Name	32-Lead PLCC	28-Lead SOIC	Function
DC	1	—	Don't Connect
A14	2	1	Address
A12	3	2	Address
A7	4	3	Address
A6	5	4	Address
A5	6	5	Address
A4	7	6	Address
A3	8	7	Address
A2	9	8	Address
A1	10	9	Address
A0	11	10	Address
NC	12	—	No Connect
I/O0	13	11	Data Input/Output
I/O1	14	12	Data Input/Output
I/O2	15	13	Data Input/Output
GND	16	14	Ground
DC	17	—	Don't Connect
I/O3	18	15	Data Input/Output
I/O4	19	16	Data Input/Output
I/O5	20	17	Data Input/Output
I/O6	21	18	Data Input/Output
I/O7	22	19	Data Input/Output
$\overline{CE}$	23	20	Chip Enable
A10	24	21	Address
$\overline{OE}$	25	22	Output Enable
NC	26	—	No Connect
A11	27	23	Address
A9	28	24	Address
A8	29	25	Address
A13	30	26	Address
$\overline{WE}$	31	27	Write Enable
V_{CC}	32	28	Device Power Supply

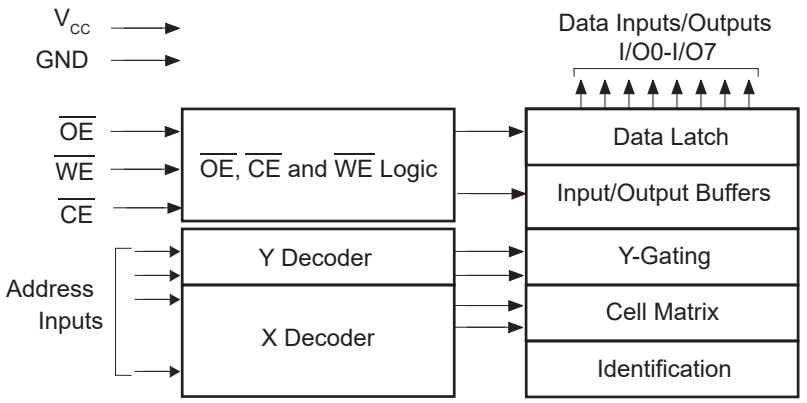
3. Description

The AT28HC256 is a high-performance Electrically Erasable and Programmable Read-Only Memory (EEPROM). Its 256-Kbit memory is organized as 32,768 words by 8 bits. Manufactured with Microchip's advanced nonvolatile CMOS technology, the device offers access times to 70 ns with power dissipation of just 440 mW. When the device is deselected, the standby current is less than 3 mA.

The AT28HC256 is accessed like a Static RAM for the read or write cycle without the need for external components. The device contains a 64-byte page register to allow writing of up to 64 bytes simultaneously. During a write cycle, the address and one to 64 bytes of data are internally latched, freeing the address and data bus for other operations. Following the initiation of a write cycle, the device will automatically write the latched data using an internal control timer. The end of a write cycle can be detected by $\overline{DATA}$ Polling of I/O7. Once the end of a write cycle has been detected, a new access for a read or write can begin.

The AT28HC256 has additional features to ensure high quality and manufacturability. The device utilizes internal error correction for extended endurance and improved data retention characteristics. An optional software data protection mechanism is available to guard against inadvertent writes. The device also includes an extra 64 bytes of EEPROM for device identification or tracking.

3.1 Block Diagram



4. Electrical Characteristics

4.1 Absolute Maximum Ratings

Temperature under bias	-55°C to +125°C
Storage temperature	-65°C to +150°C
All input voltages (including NC pins) with respect to ground	-0.6V to +6.25V
All output voltages with respect to ground	-0.6V to V_{CC} + 0.6V
Voltage on $\overline{OE}$ and A9 with respect to ground	-0.6V to +13.5V

Note: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operation listings of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

4.2 DC and AC Operating Range

Table 4-1. DC and AC Operating Range

		AT28HC256-70	AT28HC256-90	AT28HC256-12
Operating Temperature (Case)	Industrial	-40°C to +85°C	-40°C to +85°C	-40°C to +85°C
V_{CC} Power Supply		5V ± 10%	5V ± 10%	5V ± 10%

4.3 DC Characteristics

Table 4-2. DC Characteristics

Parameter	Symbol	Minimum	Maximum	Units	Test Conditions
Input Load Current	I_{LI}	—	10	µA	V_{IN} = 0V to V_{CC} + 1V
Output Leakage Current	I_{LO}	—	10	µA	$V_{I/O}$ = 0V to V_{CC}
V_{CC} Standby Current TTL	I_{SB1}	—	3	mA	$\overline{CE}$ = 2.0V to V_{CC} for AT28HC256-90, -12
		—	60	mA	$\overline{CE}$ = 2.0V to V_{CC} for AT28HC256-70
V_{CC} Standby Current CMOS	I_{SB2}	—	300	µA	$\overline{CE}$ = V_{CC} - 0.3V to V_{CC} for AT28HC256-90, -12
V_{CC} Active Current	I_{CC}	—	80	mA	f = 5 MHz; I_{OUT} = 0 mA
Input Low Voltage	V_{IL}	—	0.8	V	
Input High Voltage	V_{IH}	2.0	—	V	
Output Low Voltage	V_{OL}	—	0.45	V	I_{OL} = 6.0 mA
Output High Voltage	V_{OH}	2.4	—	V	I_{OH} = -4 mA

4.4 Pin Capacitance

Table 4-3. Pin Capacitance[1,2]

Symbol	Typical	Maximum	Units	Conditions
C_{IN}	4	6	pF	V_{IN} = 0V
C_{OUT}	8	12	pF	V_{OUT} = 0V

Notes:

1. This parameter is characterized but is not 100% tested in production.
2. f = 1 MHz, T_A = 25°C

5. Normalized I_{CC} Graphics

Figure 5-1. Normalized Supply Current vs. Temperature

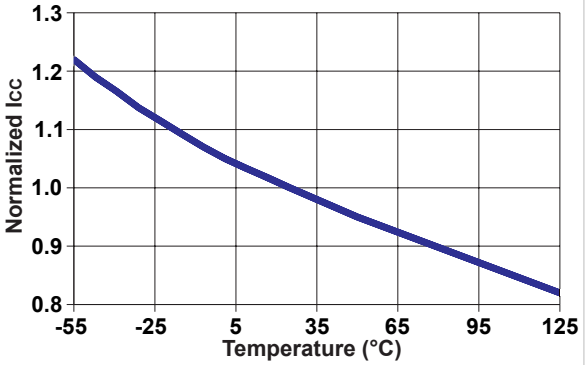


Figure 5-2. Normalized Supply Current vs. Address Frequency

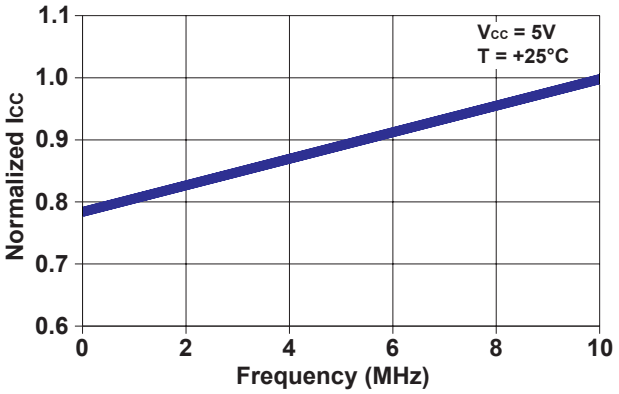
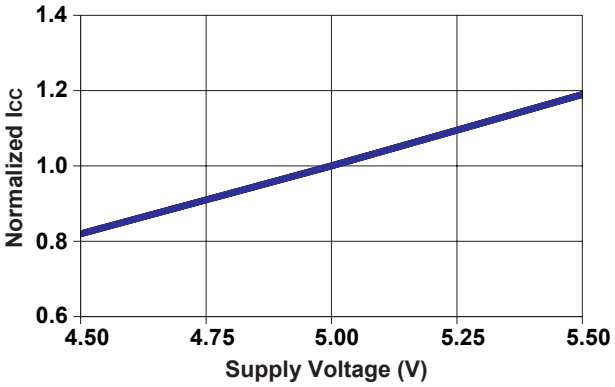


Figure 5-3. Normalized Supply Current vs. Supply Voltage



6. Device Operation

READ: The AT28HC256 is accessed like a Static RAM. When $\overline{CE}$ and $\overline{OE}$ are low and $\overline{WE}$ is high, the data stored at the memory location determined by the address pins are asserted on the outputs. The outputs are put in the high-impedance state when either $\overline{CE}$ or $\overline{OE}$ is high. This dual-line control gives designers flexibility in preventing bus contention in their system.

BYTE WRITE: A low pulse on the $\overline{WE}$ or $\overline{CE}$ input with $\overline{CE}$ or $\overline{WE}$ low (respectively) and $\overline{OE}$ high initiates a write cycle. The address is latched on the falling edge of $\overline{CE}$ or $\overline{WE}$, whichever occurs last. The data is latched by the first rising edge of $\overline{CE}$ or $\overline{WE}$. Once a byte write is started, it will automatically time itself to completion. Once a programming operation is initiated and for the duration of t_{WC}, a read operation will effectively be a polling operation.

PAGE WRITE: The page write operation of the AT28HC256 allows one to 64 bytes of data to be written into the device during a single internal programming period. A page write operation is initiated in the same manner as a byte write; the first byte written can then be followed by one to 63 additional bytes. Each successive byte must be written within 150 µs (t_{BLC}) of the previous byte. If the t_{BLC} limit is exceeded, the AT28HC256 will cease accepting data and commence the internal programming operation. All bytes during a page write operation must reside on the same page as defined by the state of the A6-A14 inputs. For each $\overline{WE}$ high-to-low transition during the page write operation, A6-A14 must be the same. The A0 to A5 inputs are used to specify which bytes within the page are to be written. The bytes may be loaded in any order and may be altered within the same load period. Only bytes which are specified for writing will be written; unnecessary cycling of other bytes within the page does not occur.

DATA POLLING: The AT28HC256 features $\overline{DATA}$ Polling to indicate the end of a write cycle. During a byte or page write cycle, an attempted read of the last byte written will result in the complement of the written data to be presented on I/O7. Once the write cycle has been completed, true data is valid on all outputs and the next write cycle may begin. $\overline{DATA}$ Polling may begin at any time during the write cycle.

TOGGLE BIT: In addition to $\overline{DATA}$ Polling, the AT28HC256 provides another method for determining the end of a write cycle. During the write operation, successive attempts to read data from the device will result in I/O6 toggling between one and zero. Once the write is completed, I/O6 will stop toggling and valid data will be read. Testing the toggle bit may begin at any time during the write cycle.

DATA PROTECTION: If precautions are not taken, inadvertent writes to any 5-volt-only nonvolatile memory may occur during transitions of the host system power supply. Microchip incorporated both hardware and software features that will protect the memory against inadvertent writes.

HARDWARE PROTECTION: Hardware features protect against inadvertent writes to the AT28HC256 in the following ways:

- V_{CC} sense – if V_{CC} is below 3.8V (typical), the write function is inhibited
- V_{CC} power-on delay – once V_{CC} reached 3.8V, the device will automatically time out 5 ms (typical) before allowing a write
- Write inhibit – holding any one of $\overline{OE}$ low, $\overline{CE}$ high or $\overline{WE}$ high inhibits write cycles
- Noise filter – pulses of less than 15 ns (typical) on the $\overline{WE}$ or $\overline{CE}$ inputs will not initiate a write cycle

SOFTWARE DATA PROTECTION: A software-controlled data protection feature was implemented on the AT28HC256. When enabled, the software data protection (SDP) feature will prevent inadvertent writes. SDP may be enabled or disabled by the user; the AT28HC256 is shipped with SDP disabled.

SDP is enabled when the user issues a series of three write commands in which three specific bytes of data are written to three specific addresses. After writing the 3-byte command sequence and after t_{WC}, the entire AT28HC256 will be protected against inadvertent write operations. It should be noted that, once protected, the host may still perform a byte or page write to the AT28HC256. This

is done by preceding the data to be written by the same 3-byte command sequence used to enable SDP.

Once set, SDP will remain active unless the disable command sequence is issued. Power transitions do not disable SDP and SDP will protect the AT28HC256 during power-up and power-down conditions. All command sequences must conform to the page write timing specifications. The data in the enable and disable command sequences are not written to the device and the memory addresses used in the sequence may be written with data in either a byte or page write operation.

After setting SDP, any attempt to write to the device without the 3-byte command sequence will start the internal write timers. No data will be written to the device. However, for the duration of t_{WC}, read operations will effectively be polling operations.

DEVICE IDENTIFICATION: An extra 64 bytes of EEPROM memory are available to the user for device identification. By raising A9 to 12V ± 0.5V and using address locations 7FC0H to 7FFFH, the bytes may be written to or read from in the same manner as the regular memory array.

OPTIONAL CHIP ERASE MODE: The entire device can be erased using a 6-byte software code. Refer to the following application note, available at the corporate website (www.microchip.com), for details: AN0544, *Software Chip Erase*.

6.1 Operating Modes

Table 6-1. Operating Modes

Mode	$\overline{CE}$	$\overline{OE}$	$\overline{WE}$	I/O
Read	V_{IL}	V_{IL}	V_{IH}	D_{OUT}
Write(1)	V_{IL}	V_{IH}	V_{IL}	D_{IN}
Standby/Write Inhibit	V_{IH}	X(2)	X	High-Z
Write Inhibit	X	X	V_{IH}	—
Write Inhibit	X	V_{IL}	X	—
Output Disable	X	V_{IH}	X	High-Z
Chip Erase	V_{IL}	V_H(3)	V_{IL}	High-Z

Notes:

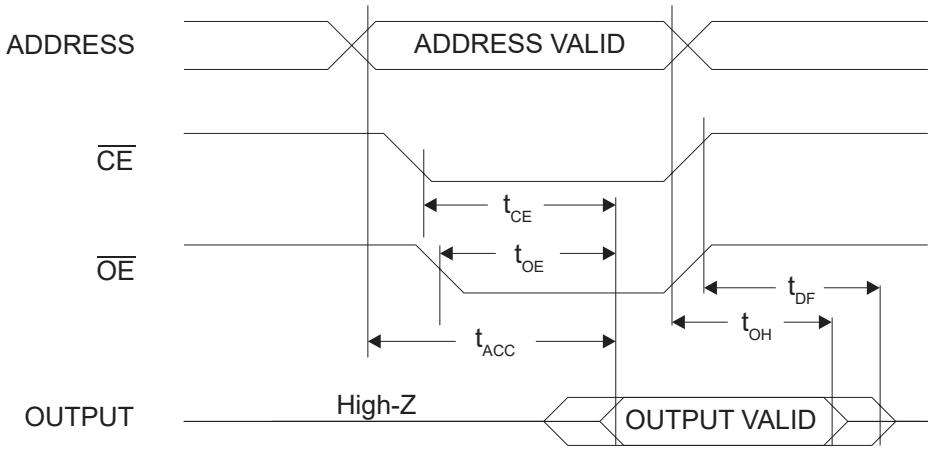
1. Refer to AC Write Waveforms.
2. X can be V_{IL} or V_{IH}.
3. V_H = 12.0 V ± 0.5V

6.2 AC Read Characteristics

Table 6-2. AC Read Characteristics

Parameter	Symbol	AT28HC256-70		AT28HC256-90		AT28HC256-12		Units
		Min.	Max.	Min.	Max.	Min.	Max.	
Address to Output Delay	t_{ACC}	—	70	—	90	—	120	ns
$\overline{CE}$ to Output Delay	t_{CE}(1)	—	70	—	90	—	120	ns
$\overline{OE}$ to Output Delay	t_{OE}(2)	0	35	0	40	0	50	ns
$\overline{CE}$ or $\overline{OE}$ to Output Float	t_{DF}(3,4)	0	35	0	40	0	50	ns
Output Hold from $\overline{OE}$, $\overline{CE}$ or Address, whichever occurred first	t_{OH}	0	—	0	—	0	—	ns

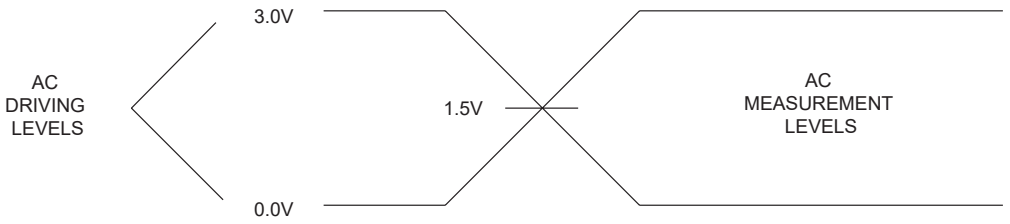
6.3 AC Read Waveforms[1,2,3,4]



Notes:

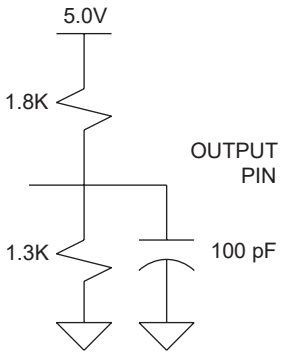
1. $\overline{CE}$ may be delayed up to t_{ACC}-t_{CE} after the address transition without impact on t_{ACC}.
2. $\overline{OE}$ may be delayed up to t_{CE}-t_{OE} after the falling edge of $\overline{CE}$ without impact on t_{CE} or by t_{ACC}-t_{OE} after an address change without impact in t_{ACC}.
3. t_{DF} is specified from $\overline{OE}$ or $\overline{CE}$, whichever occurs first (C_L = 5 pF).
4. This parameter is characterized and is not 100% tested.

6.4 Input Test Waveforms and Measurement Level



Note: t_R, t_F < 5 ns.

6.5 Output Test Load



6.6 AC Write Characteristics

Table 6-3. AC Write Characteristics

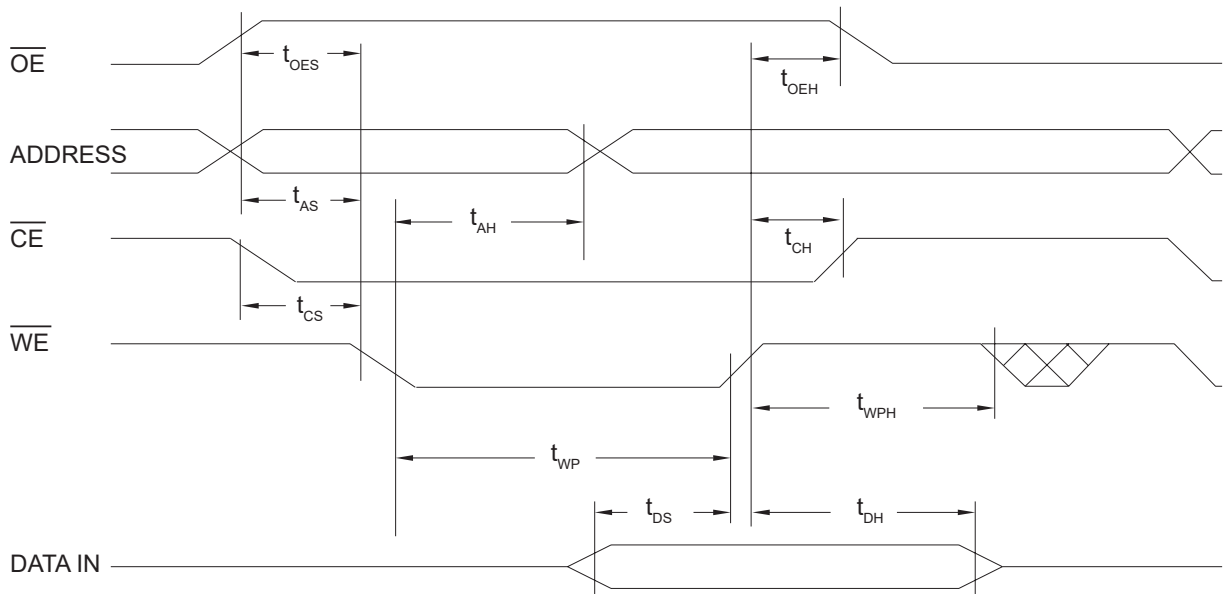
Parameter	Symbol	Minimum	Maximum	Units
Address, $\overline{OE}$ Setup Time	t_{AS}, t_{OES}	0	—	ns
Address Hold Time	t_{AH}	50	—	ns
Chip Select Setup Time	t_{CS}	0	—	ns
Chip Select Hold Time	t_{CH}	0	—	ns
Write Pulse Width ($\overline{WE}$ or $\overline{CE}$)	t_{WP}	100	—	ns
Data Setup Time	t_{DS}	50	—	ns
Data, $\overline{OE}$ Hold Time	t_{DH}, t_{OEH}	0	—	ns
Time to Data Valid	t_{DV}	NR(1)	—	

Note:

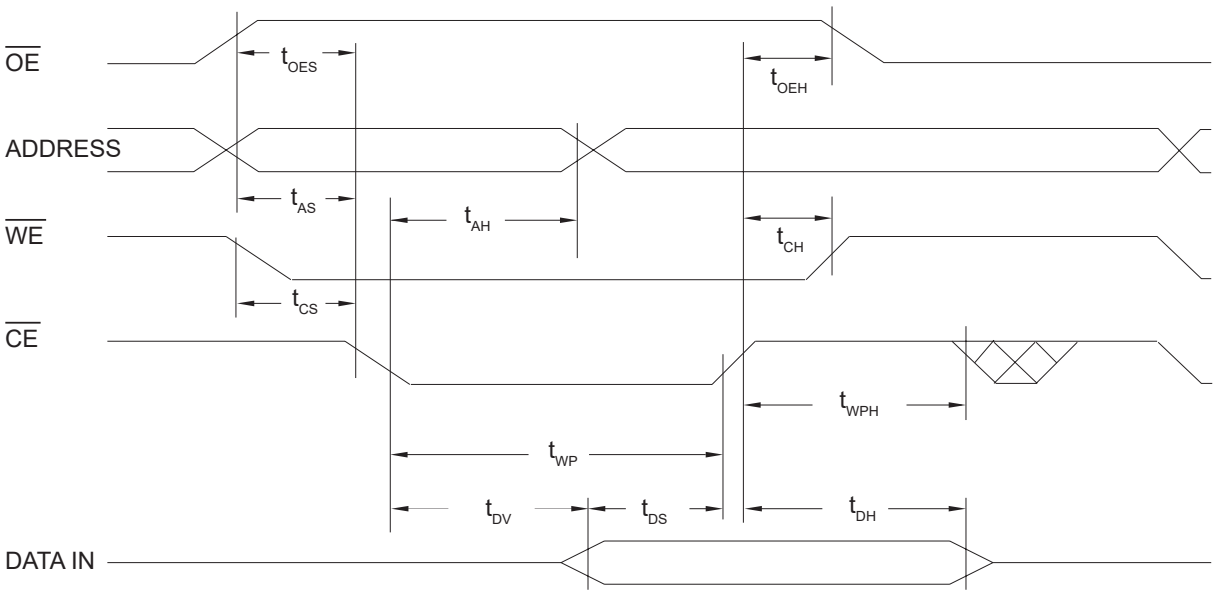
1. NR = No Restriction

6.7 AC Write Waveforms

6.7.1 $\overline{WE}$ Controlled



6.7.2 $\overline{CE}$ Controlled

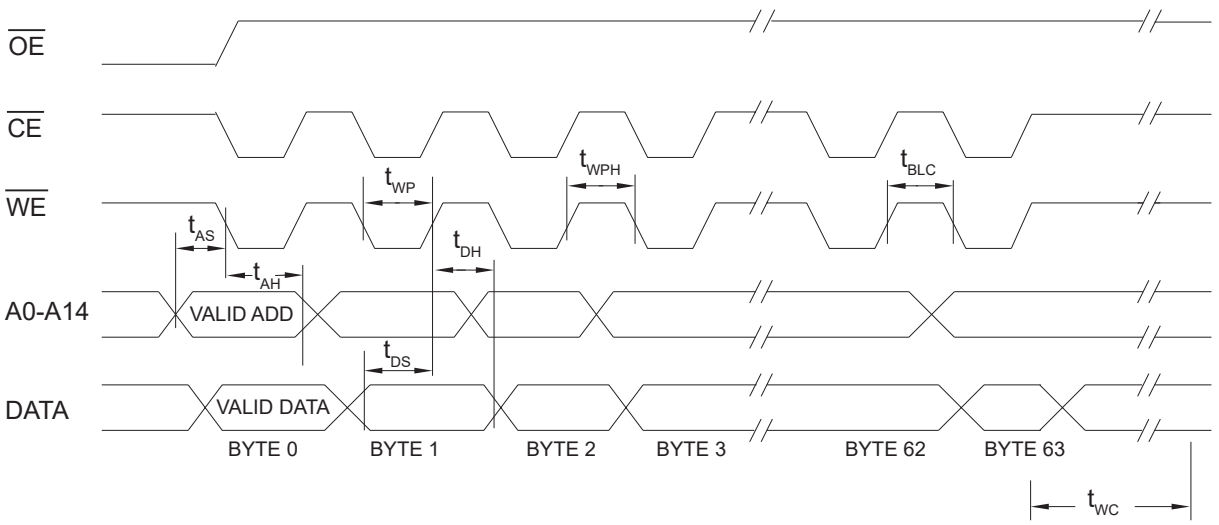


6.8 Page Mode Characteristics

Table 6-4. Page Mode Write Characteristics

Parameter		Symbol	Minimum	Maximum	Units
Write Cycle Time (option available)	AT28HC256	t_{WC}	—	10	ms
	AT28HC256F		—	3	ms
Address Setup Time		t_{AS}	0	—	ns
Address Hold Time		t_{AH}	50	—	ns
Data Setup Time		t_{DS}	50	—	ns
Data Hold Time		t_{DH}	0	—	ns
Write Pulse Width		t_{WP}	100	—	ns
Byte Load Cycle Time		t_{BLC}	—	150	µs
Write Pulse Width High		t_{WPH}	50	—	ns

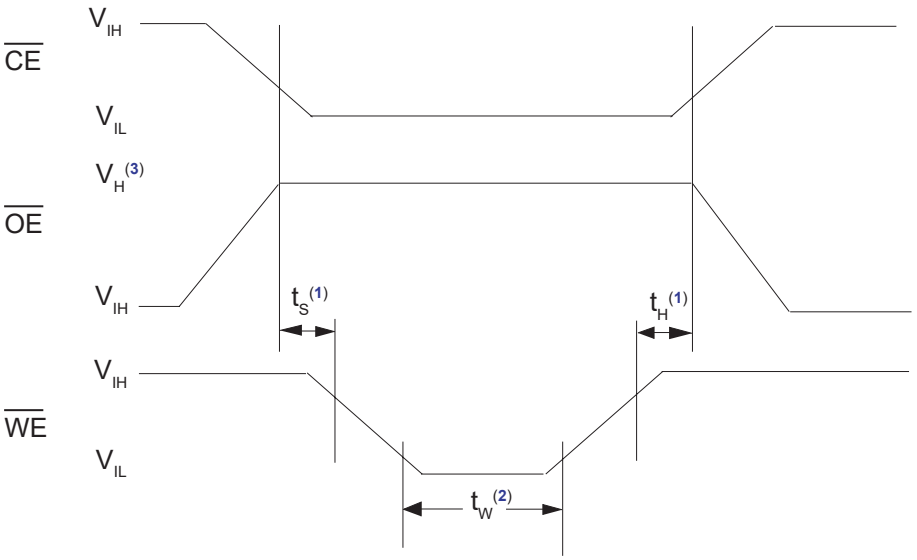
6.9 Page Mode Write Waveforms[1,2]



Notes:

1. A6 through A14 must specify the same page address during each high-to-low transition of $\overline{WE}$ (or $\overline{CE}$).
2. $\overline{OE}$ must be high only when $\overline{WE}$ and $\overline{CE}$ are both low.

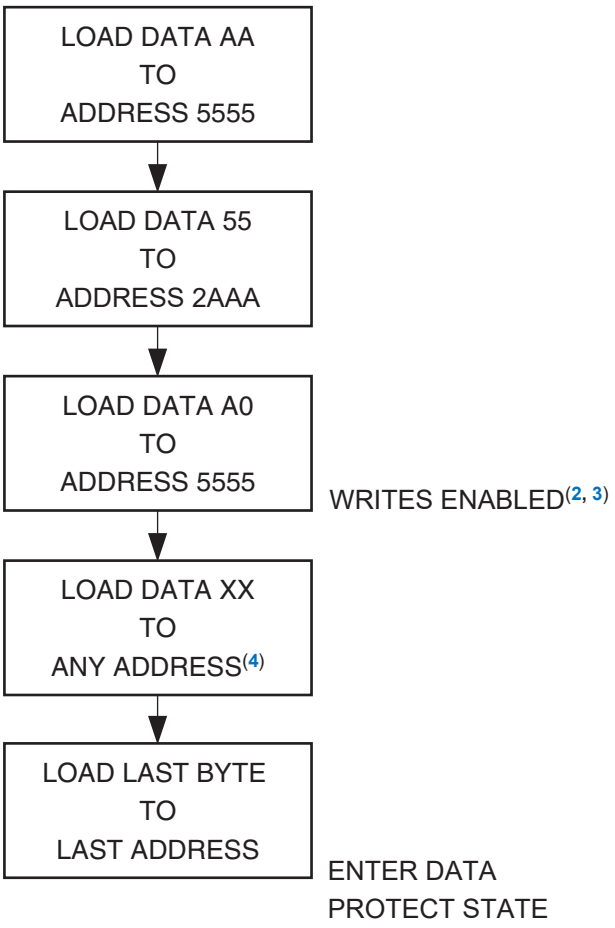
6.10 Chip Erase Waveforms



Notes:

1. $t_S = t_H = 5$ µsec (minimum)
2. $t_W = 10$ msec (minimum)
3. $V_H = 12.0V \pm 0.5V$

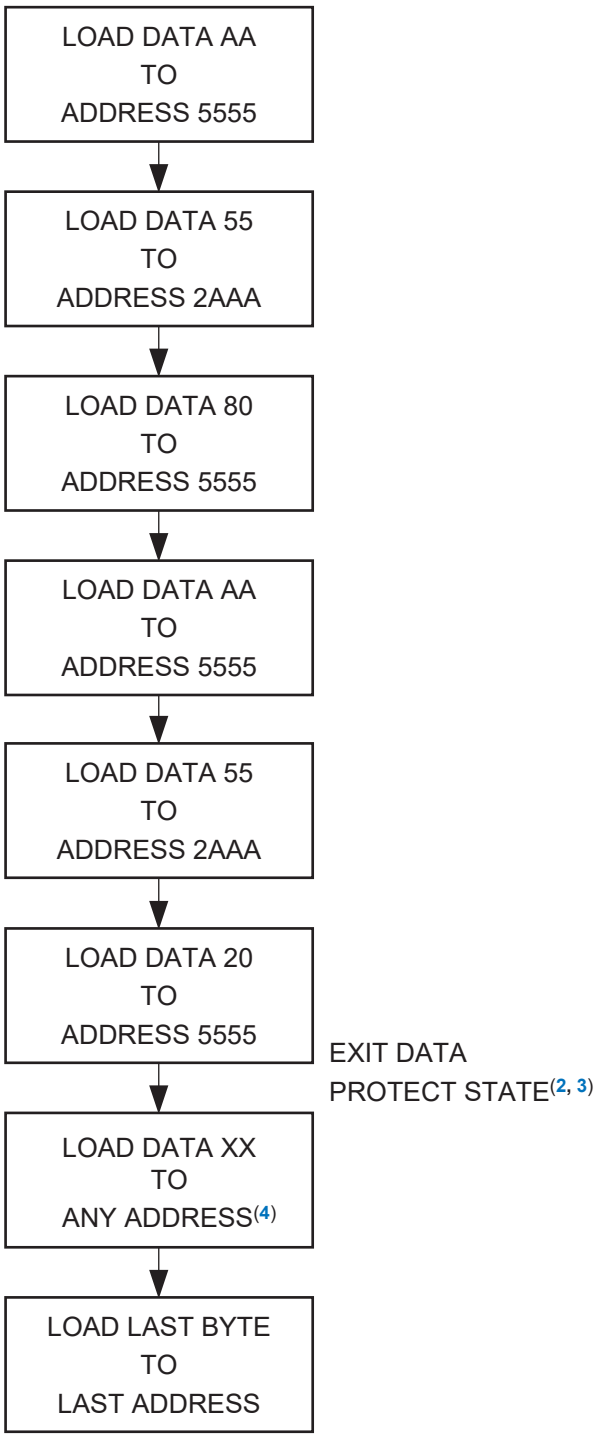
6.11 Software Data Protection Enable Algorithm[1]



Notes:

1. Data format: I/O7-I/O0 (Hex); Address format: A14-A0 (Hex).
2. Write-Protect state will be activated at end of write even if no other data is loaded.
3. Write-Protect state will be deactivated at end of write period even if no other data is loaded.
4. One to 64 bytes of data are loaded.

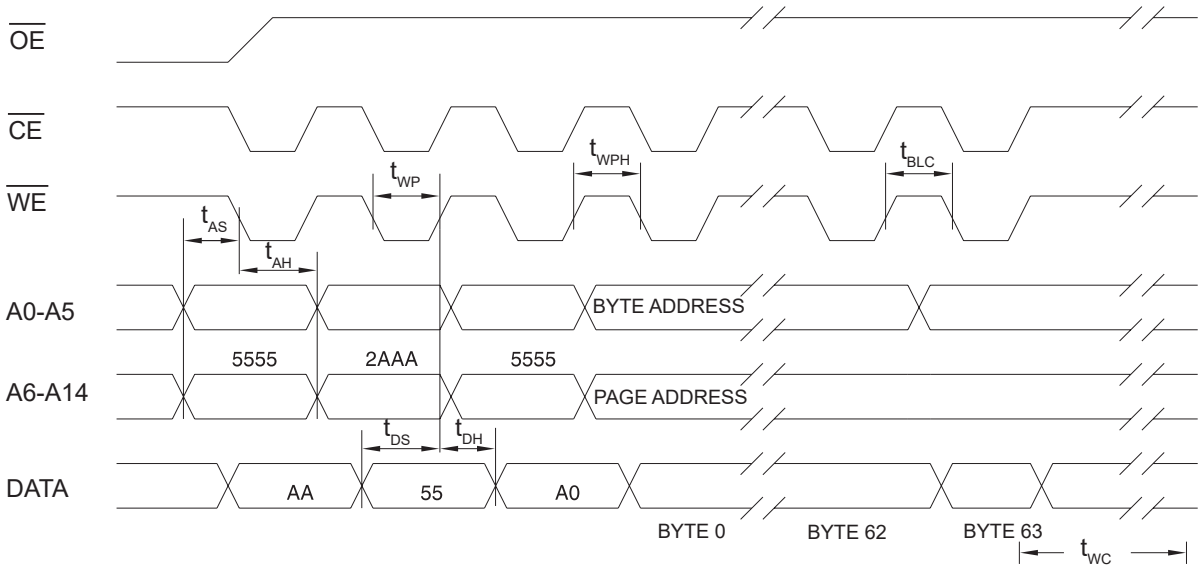
6.12 Software Data Protection Disable Algorithm[1]



Notes:

1. Data format: I/O7-I/O0 (Hex); Address format: A14-A0 (Hex).
2. Write-Protect state will be deactivated at end of write period even if no other data is loaded.
3. Write-Protect state will be deactivated at end of write period even if no other data is loaded.
4. One to 64 bytes of data are loaded.

6.13 Software Protected Program Cycle Waveform[1,2]



Notes:

1. A6-A14 must specify the same page address during each high-to-low transition of $\overline{WE}$ (or $\overline{CE}$) after the software code has been entered.
2. $\overline{OE}$ must be high only when $\overline{WE}$ and $\overline{CE}$ are both low.

6.14 $\overline{Data}$ Polling Characteristics[1]

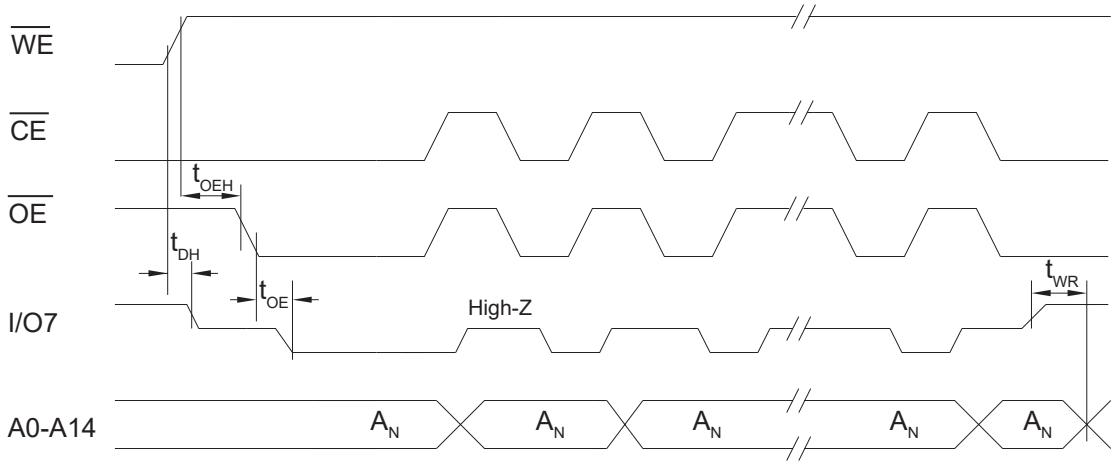
Table 6-5. Data Polling Characteristics

Parameter	Symbol	Minimum	Typical	Maximum	Units
Data Hold Time	t_{DH}	0	—	—	ns
$\overline{OE}$ Hold Time	t_{OEH}	0	—	—	ns
$\overline{OE}$ to Output Delay[2]	t_{OE}	—	—	—	ns
Write Recovery Time	t_{WR}	0	—	—	ns

Notes:

1. These parameters are characterized and not 100% tested.
2. See AC Read Characteristics.

6.15 $\overline{\text{Data}}$ Polling Waveforms



6.16 Toggle Bit Characteristics[1]

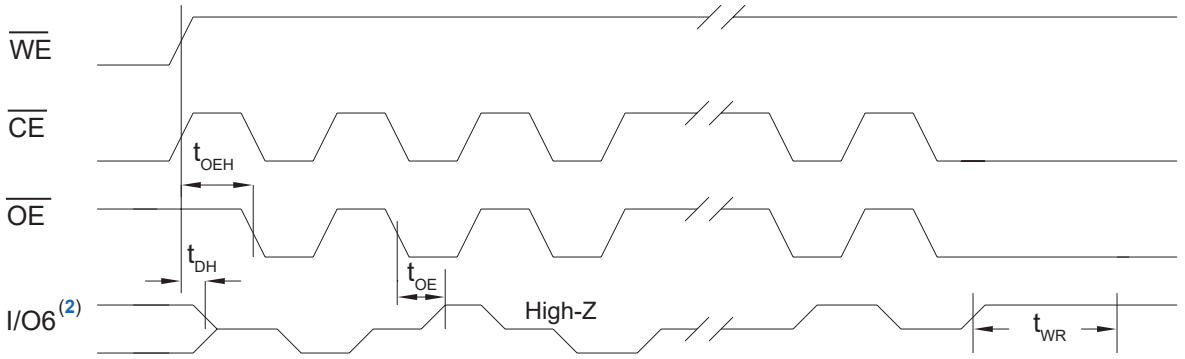
Table 6-6. Toggle Bit Characteristics

Parameter	Symbol	Minimum	Typical	Maximum	Units
Data Hold Time	t_{DH}	10	—	—	ns
$\overline{\text{OE}}$ Hold Time	t_{OEH}	10	—	—	ns
$\overline{\text{OE}}$ to Output Delay[2]	t_{OE}	—	—	—	ns
$\overline{\text{OE}}$ High Pulse[2]	t_{OEHP}	150	—	—	ns
Write Recovery Time	t_{WR}	0	—	—	ns

Notes:

1. These parameters are characterized and not 100% tested.
2. See AC Read Characteristics.

6.17 Toggle Bit Waveforms



Notes:

1. Toggling either $\overline{OE}$ or $\overline{CE}$ or both $\overline{OE}$ and $\overline{CE}$ will operate toggle bit.
2. Beginning and ending state of I/O6 will vary.
3. Any address location may be used but the address should not vary.

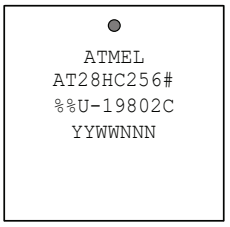
7. Packaging Information

7.1 Package Marking Information

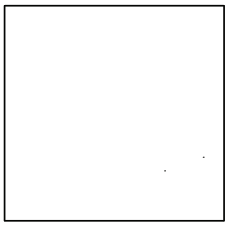
AT28HC256: Package Marking Information

32-Lead PLCC

Topside

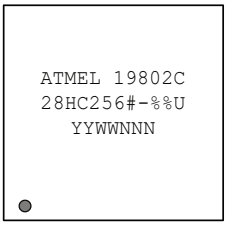


Backside

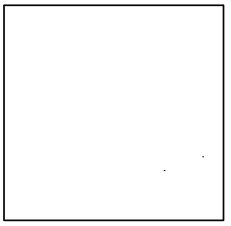


28-Lead SOIC

Topside



Backside

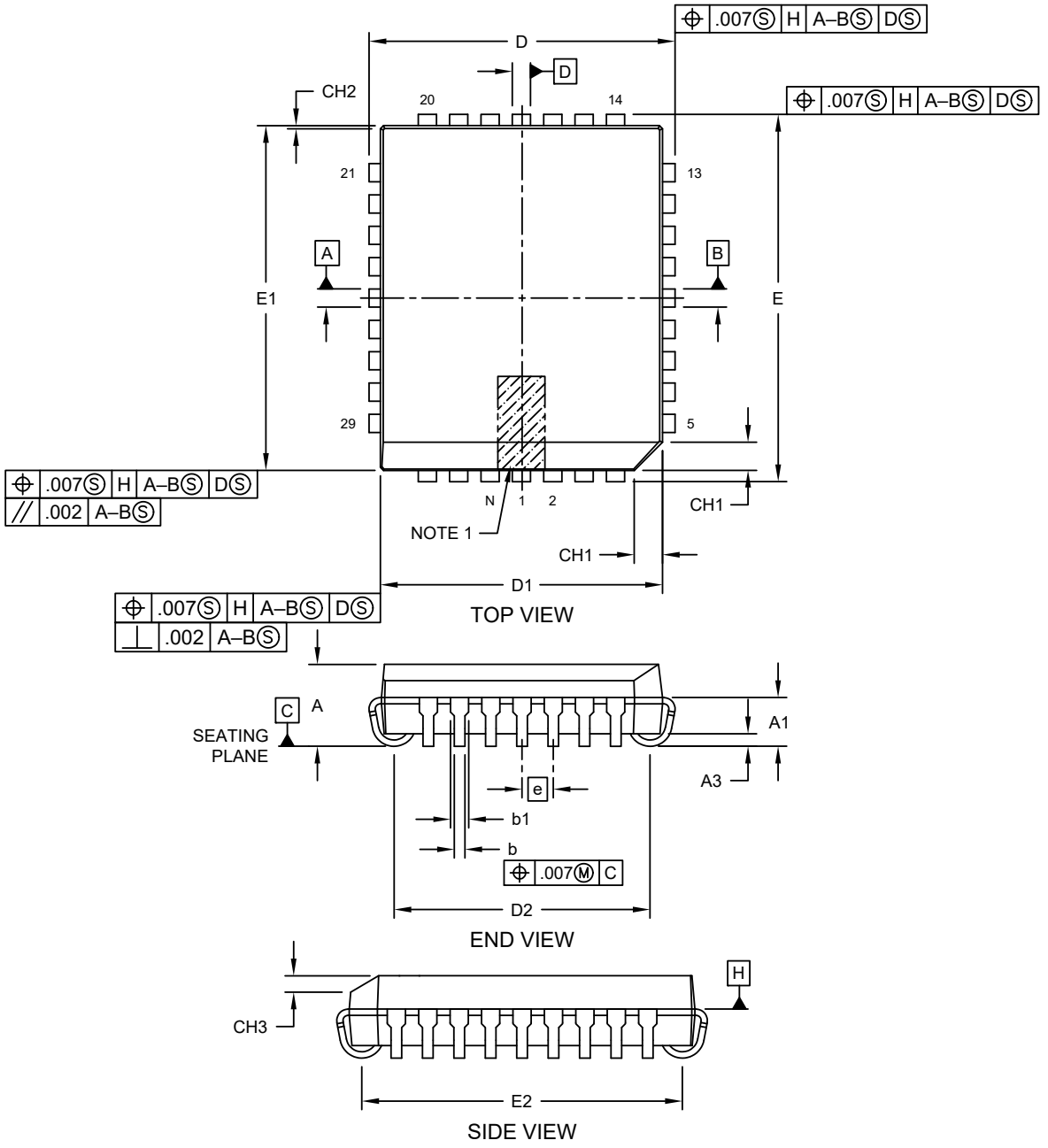


Note: no backside markings

		%% = Access Time	
		70: 70 ns 90: 90 ns 12: 120 ns	
# Options		**Lot Trace Code**	
Blank = 10k writes, 10ms standard E = 100k writes, Extended endurance F = 3ms Fast write cycle		YYWWNNN: Lot Trace Code YY = Year, WW = Work Week NNN = Assembly Trace Code	

32-Lead Plastic Leaded Chip Carrier (L) - Rectangle [PLCC]

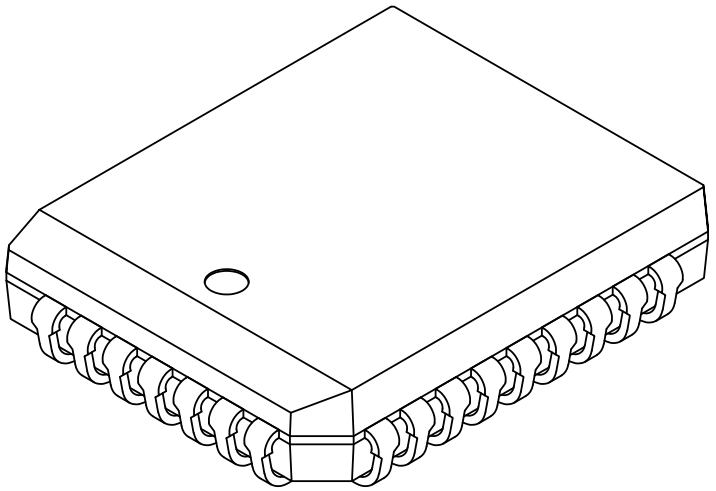
Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



Microchip Technology Drawing C04-023 Rev C Sheet 1 of 2

32-Lead Plastic Leaded Chip Carrier (L) - Rectangle [PLCC]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



Units		INCHES		
Dimension Limits		MIN	NOM	MAX
Number of Pins	N		32	
Pitch	e		.050 BSC	
Pins along Length	ND		7	
Pins along Width	NE		9	
Overall Height	A	.125	.132	.140
Contact Height	A1	.060	.0775	.095
Standoff §	A3	.015	-	-
Corner Chamfer	CH1	.042	.045	.048
Chamfers	CH2	-	-	.020
Side Chamfer Height	CH3	.023	.026	.029
Overall Length	D	.485	.490	.495
Overall Width	E	.585	.590	.595
Molded Package Length	D1	.447	.450	.453
Molded Package Width	E1	.547	.550	.553
Footprint Length	D2	.376	.411	.446
Footprint Width	E2	.476	.511	.546
Lead Thickness	c	.008	.010	.013
Upper Lead Width	b1	.026	.029	.032
Lower Lead Width	b	.013	.017	.021

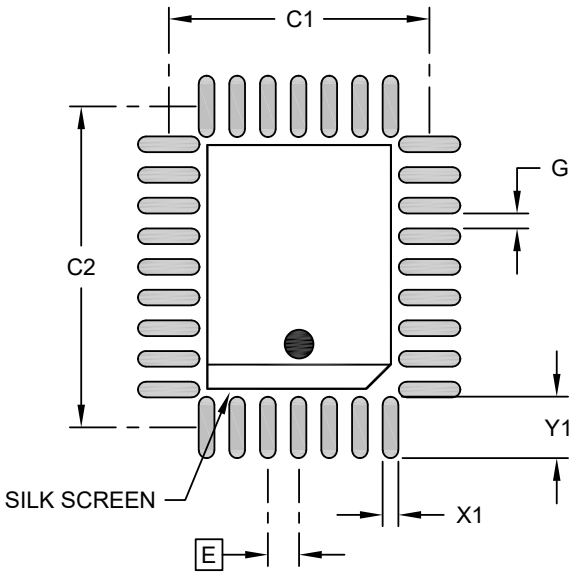
Notes:

1. Pin 1 visual index feature may vary, but must be located within the hatched area.
2. Dimensioning and tolerancing per ASME Y14.5M
   BSC: Basic Dimension. Theoretically exact value shown without tolerances.
   REF: Reference Dimension, usually without tolerance, for information purposes only.

Microchip Technology Drawing C04-023 Rev C Sheet 2 of 2

32-Lead Plastic Leaded Chip Carrier (L) - Rectangle [PLCC]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



RECOMMENDED LAND PATTERN

Units		INCHES		
Dimension Limits		MIN	NOM	MAX
Contact Pitch	E	.050 BSC		
Contact Pad Spacing	C1		.425	
Contact Pad Spacing	C2		.524	
Contact Pad Width (X32)	X1			.026
Contact Pad Length (X32)	Y1			.100
Contact Pad to Center Pad (X28)	G	.008		

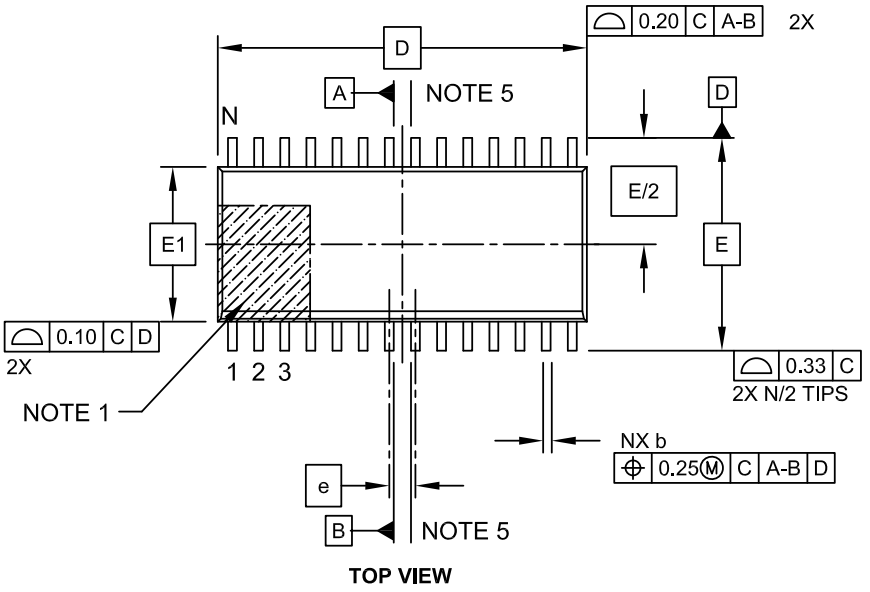
Notes:

1. Dimensioning and tolerancing per ASME Y14.5M
   BSC: Basic Dimension. Theoretically exact value shown without tolerances.
2. For best soldering results, thermal vias, if used, should be filled or tented to avoid solder loss during reflow process

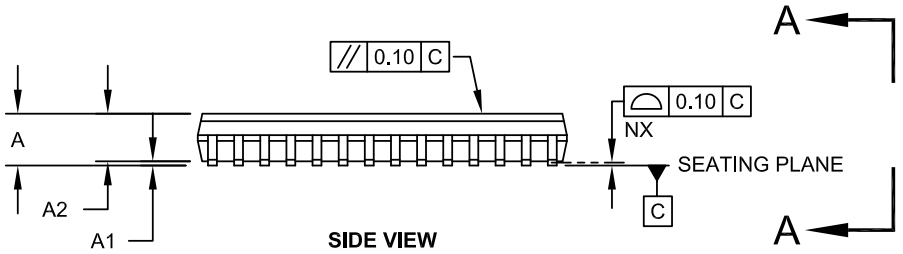
Microchip Technology Drawing C04-2023 Rev C

28-Lead Plastic Small Outline (SO) - Wide, 7.50 mm Body [SOIC]

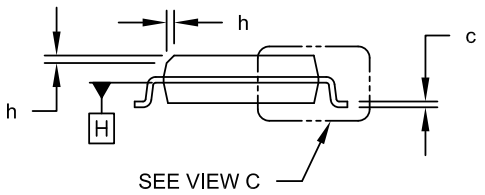
Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



TOP VIEW



SIDE VIEW

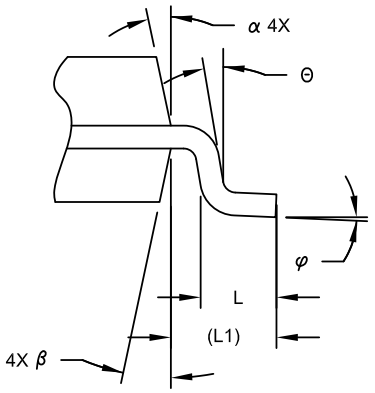


VIEW A-A

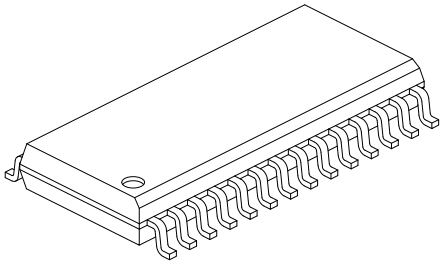
Microchip Technology Drawing C04-052C Sheet 1 of 2

28-Lead Plastic Small Outline (SO) - Wide, 7.50 mm Body [SOIC]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



VIEW C



Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Number of Pins	N		28	
Pitch	e		1.27 BSC	
Overall Height	A	-	-	2.65
Molded Package Thickness	A2	2.05	-	-
Standoff §	A1	0.10	-	0.30
Overall Width	E		10.30 BSC	
Molded Package Width	E1		7.50 BSC	
Overall Length	D		17.90 BSC	
Chamfer (Optional)	h	0.25	-	0.75
Foot Length	L	0.40	-	1.27
Footprint	L1		1.40 REF	
Lead Angle	Θ	0°	-	-
Foot Angle	φ	0°	-	8°
Lead Thickness	c	0.18	-	0.33
Lead Width	b	0.31	-	0.51
Mold Draft Angle Top	α	5°	-	15°
Mold Draft Angle Bottom	β	5°	-	15°

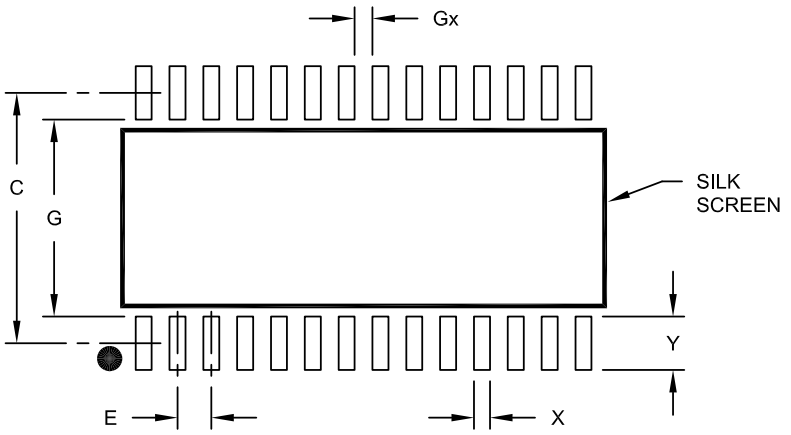
Notes:

1. Pin 1 visual index feature may vary, but must be located within the hatched area.
2. § Significant Characteristic
3. Dimension D does not include mold flash, protrusions or gate burrs, which shall not exceed 0.15 mm per end. Dimension E1 does not include interlead flash or protrusion, which shall not exceed 0.25 mm per side.
4. Dimensioning and tolerancing per ASME Y14.5M
   BSC: Basic Dimension. Theoretically exact value shown without tolerances.
   REF: Reference Dimension, usually without tolerance, for information purposes only.
5. Datums A & B to be determined at Datum H.

Microchip Technology Drawing C04-052C Sheet 2 of 2

28-Lead Plastic Small Outline (SO) - Wide, 7.50 mm Body [SOIC]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



RECOMMENDED LAND PATTERN

Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Contact Pitch	E		1.27 BSC	
Contact Pad Spacing	C		9.40	
Contact Pad Width (X28)	X			0.60
Contact Pad Length (X28)	Y			2.00
Distance Between Pads	Gx	0.67		
Distance Between Pads	G	7.40		

Notes:

1. Dimensioning and tolerancing per ASME Y14.5M

BSC: Basic Dimension. Theoretically exact value shown without tolerances.

Microchip Technology Drawing No. C04-2052A

8. Revision History

Revision B (August 2023)

Removed 28-Lead TSOP package. Updated 32-Lead PLCC package drawing to latest revision (no change to form, fit or function).

Revision A (October 2020)

Updated to the Microchip template. Microchip DS20006428 replaces Atmel document 0007. Added updated Part Markings to include new trace code format.

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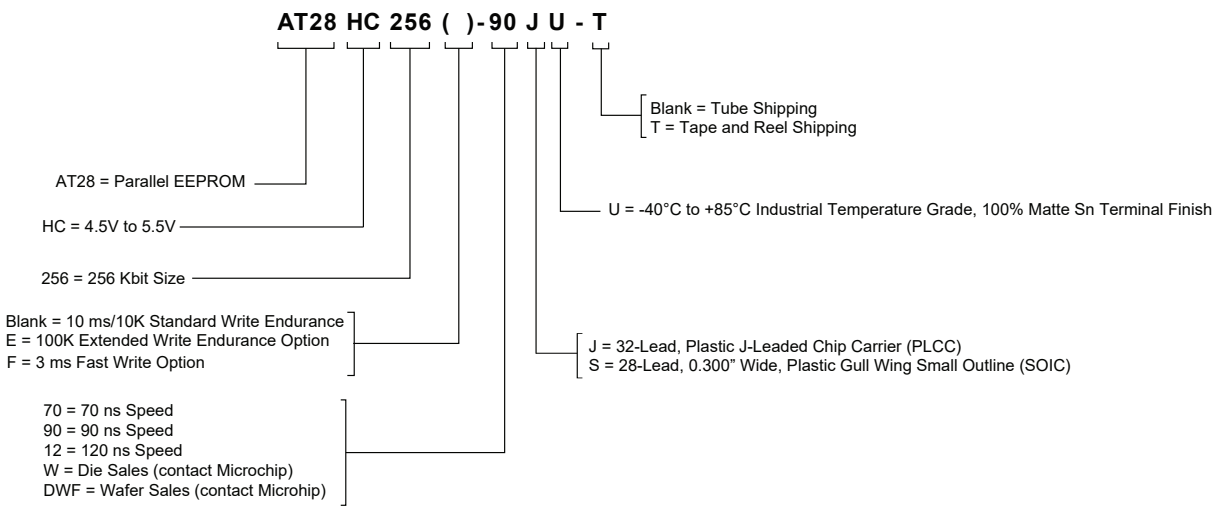

Examples

Table 9-1. AT28HC256 Industrial Ordering Information

Ordering Code	Package Drawing Code	Package Option	t_{ACC}(ns)	Quantity	Operating Range
AT28HC256-70JU	L	J	70	32 Tube	Industrial Temperature (-40°C to +85°C)
AT28HC256-70JU-T				750 Reel	
AT28HC256-90JU	L	J	90	32 Tube	
AT28HC256-90JU-T				750 Reel	
AT28HC256-90SU	SO	S		27 Tube	
AT28HC256-90SU-T				1000 Reel	
AT28HC256-12JU	L	J	120	32 Tube	
AT28HC256-12JU-T				750 Reel	
AT28HC256-12SU	SO	S		27 Tube	
AT28HC256-12SU-T				1000 Reel	

Table 9-2. AT28HC256E Industrial Ordering Information

Ordering Code	Package Drawing Code	Package Option	t_{ACC}(ns)	Quantity	Operating Range
AT28HC256E-70JU	L	J	70	32 Tube	Industrial Temperature (-40°C to +85°C)
AT28HC256E-70JU-T				750 Reel	
AT28HC256E-70SU-T	SO	S		1000 Reel	
AT28HC256E-90JU	L	J	90	32 Tube	
AT28HC256E-90JU-T				750 Reel	
AT28HC256E-90SU	SO	S		27 Tube	
AT28HC256E-90SU-T				1000 Reel	

Table 9-3. AT28HC256F Industrial Ordering Information

Ordering Code	Package Drawing Code	Package Option	t_{ACC}(ns)	Quantity	Operating Range
AT28HC256F-90JU	L	J	90	32 Tube	Industrial Temperature (-40°C to +85°C)
AT28HC256F-90JU-T				750 Reel	
AT28HC256F-90SU	SO	S		27 Tube	
AT28HC256F-90SU-T				1000 Reel	

Package Types	
J	32-Lead, Plastic J-leaded Chip Carrier (PLCC)
S	28-Lead, 0.300" Wide, Plastic Gull Wing Small Outline (SOIC)
W	Diced Die in Waffle Tray
DWF	Die in Wafer Form Shipped in 6-inch Round Jars

Options	
Blank	Standard Device: Endurance = 10K Write Cycles; Write Time 10 ms
E	High Endurance Option: Endurance = 100K Write Cycles
F	Fast Write Option: Write Time = 3 ms

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