MIC5321

High-Performance, Dual 150 mA µCap Ultra-Low Dropout Regulator

Features

- 2.3V to 5.5V Input Voltage Range
- Ultra-Low Dropout Voltage 35 mV @ 150 mA
- Tiny 6-Pin 1.6 mm x 1.6 mm Thin UDFN Leadless Package
- Low Cost 6-Lead TSOT-23 Package
- Bypass Pin for Improved Noise Performance
- High PSRR: >75 dB on Each LDO
- Ultra-Low Noise Output: >30 µV_{RMS}
- Dual 150 mA Outputs
- µCap Stable with 1 µF Ceramic Capacitor
- Low Quiescent Current: 150 µA
- Fast Turn-On Time: 45 µs
- Thermal Shutdown Protection
- Current Limit Protection

Applications

- Mobile Phones
- PDAs
- GPS Receivers
- Portable Electronics
- Portable Media Players
- Digital Still and Video Cameras

General Description

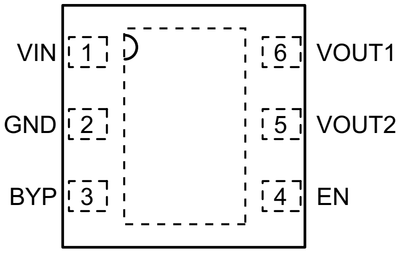
The MIC5321 is a tiny, dual ultra-low dropout linear regulator ideally suited for applications that require high PSRR because it provides a bypass pin for those noise sensitive portable electronics. The MIC5321 integrates two high-performance 150 mA ULDOs into a very compact 1.6 mm x 1.6 mm leadless UDFN package that provides exceptional thermal package characteristics.

The MIC5321 is a µCap design that enables operation with very small ceramic output capacitors for stability, thereby reducing required board space and component cost. The combination of extremely low dropout voltage, very high power supply rejection, very low output noise, and exceptional thermal package characteristics makes it ideal for powering RF application, cellular phone camera modules, imaging sensors for digital still cameras, PDAs, MP3 players and WebCam applications.

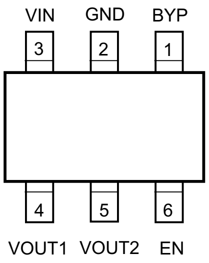
The MIC5321 is available in fixed-output voltages in the tiny 6-pin 1.6 mm x 1.6 mm leadless UDFN package, which is only 2.56 mm^2 in area, less than 30% the area of the SOT-23 and TSOP 3x3 packages. It's also available in the thin SOT-23 6-lead package and the standard size 6-pin 1.6 mm x 1.6 mm leadless WDFN package. Additional voltage options are available. For more information, contact Microchip.

Package Types

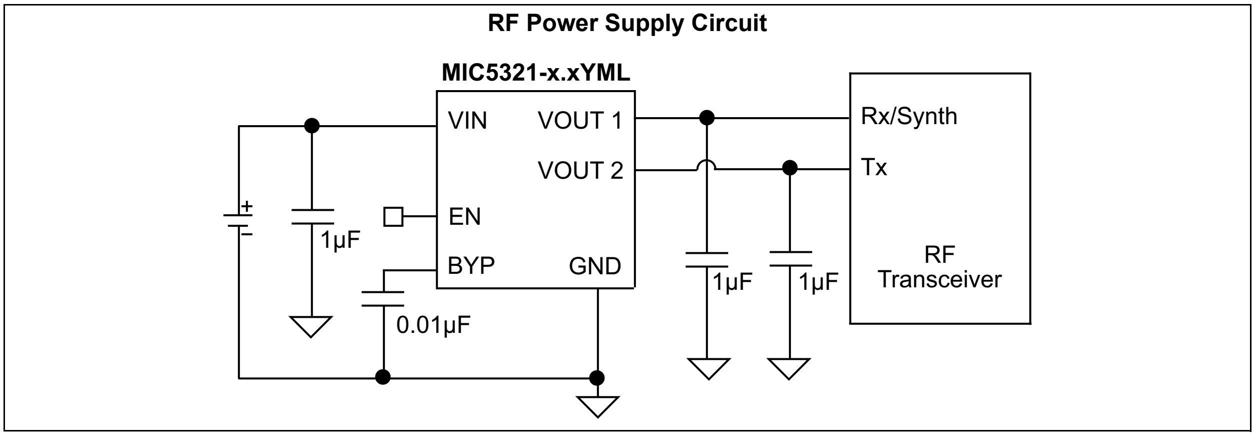
MIC5321
6-Pin 1.6 mm x 1.6 mm UDFN (MT)/WDFN (ML)
(Top View)



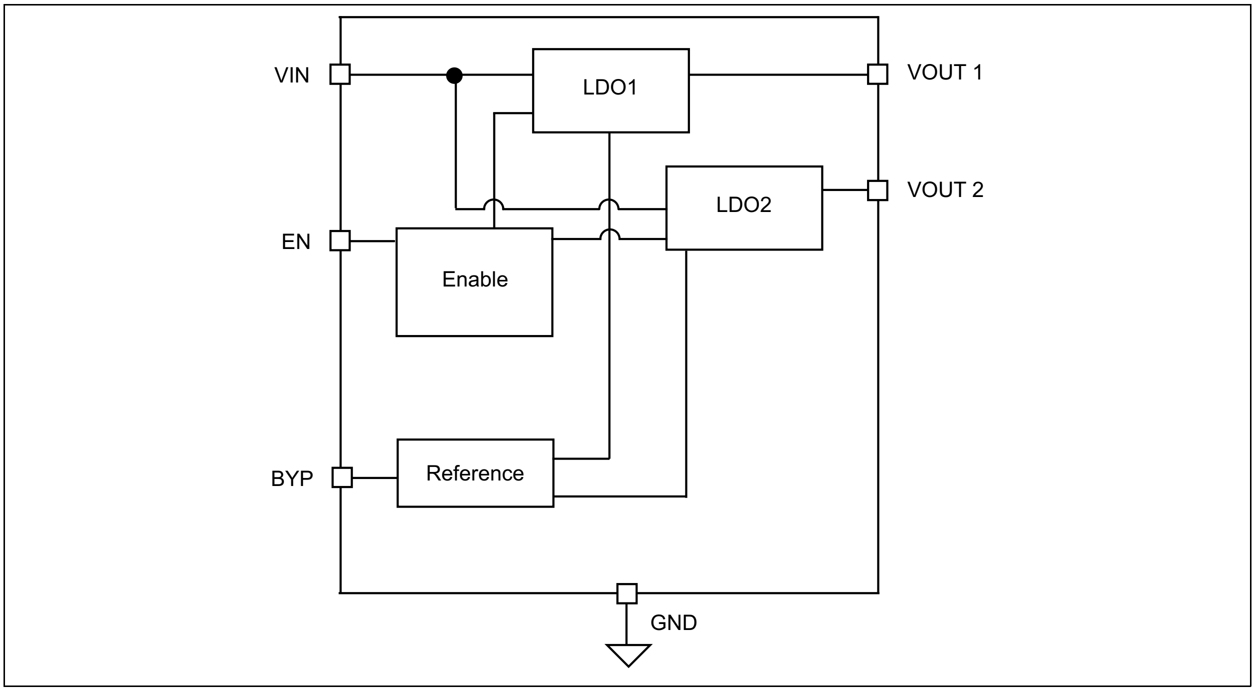
MIC5321
6-Lead SOT-23 (D6)
(Top View)



Typical Application Circuit



Functional Block Diagram



1.0 ELECTRICAL CHARACTERISTICS

Absolute Maximum Ratings †

Supply Input Voltage (V_{IN}) .... 0V to +6V
Enable Input Voltage (V_{EN}) .... 0V to +6V
Power Dissipation (P_D) Note 1 .... Internally Limited
ESD Rating (Note 2) .... 2 kV

Operating Ratings ‡

Supply Input Voltage (V_{IN}) .... +2.3V to +5.5V
Enable Input Voltage (V_{EN}) .... 0V to V_{IN}

† Notice: Stresses above those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress rating only and functional operation of the device at those or any other conditions above those indicated in the operational sections of this specification is not intended. Exposure to maximum rating conditions for extended periods may affect device reliability.

‡ Notice: The device is not guaranteed to function outside its operating ratings.

Note 1: The maximum allowable power dissipation at any T_A (ambient temperature) is $P_{D(MAX)} = (T_{J(MAX)} – T_A)/θ_{JA}$. Exceeding the maximum allowable power dissipation will result in excessive die temperature, and the regulator will go into thermal shutdown.

2: Devices are ESD sensitive. Handling precautions recommended. Human body model, 1.5 kΩ in series with 100 pF.

ELECTRICAL CHARACTERISTICS

Electrical Characteristics: V_{IN} = EN = V_{OUT} + 1.0V; higher of the two regulator outputs, $I_{OUTLDO1}$ = $I_{OUTLDO2}$ = 100 µA; C_{OUT1} = C_{OUT2} = 1 µF; C_{BYP} = 0.01 µF; T_J = 25°C, **bold** values valid for –40°C ≤ T_J ≤ +125°C, unless noted. (Note 1)

Parameter	Symbol	Min.	Typ.	Max.	Units	Conditions
Output Voltage Accuracy	V_{OUT}	–2.0	—	2.0	%	Variation from nominal V_{OUT}
		–3.0	—	**3.0**		Variation from nominal V_{OUT}; –40°C to +125°C
Line Regulation	$\Delta V_{OUT}/(V_{OUT} \times \Delta V_{IN})$	—	0.02	0.3	%/V	V_{IN} = V_{OUT} + 1V to 5.5V; I_{OUT} = 100 µA
		—	—	**0.6**		
Load Regulation	$\Delta V_{OUT}/V_{OUT}$	—	0.5	**2.0**	%	I_{OUT} = 100 µA to 150 mA
Dropout Voltage (Note 2)	V_{DO}	—	0.1	—	mV	I_{OUT} = 100 µA
		—	12	**50**		I_{OUT} = 50 mA
		—	25	**75**		I_{OUT} = 100 mA
		—	35	**100**		I_{OUT} = 150 mA
Ground Current	I_{GND}	—	150	**190**	µA	EN = High; I_{OUT1} = 150 mA, I_{OUT2} = 150 mA
Ground Current in Shutdown	I_{SHDN}	—	0.01	**2**	µA	EN1 ≤ 0.2V
Ripple Rejection	PSRR	—	75	—	dB	f = 1 kHz; C_{OUT} = 1.0 µF; C_{BYP} = 0.1 µF
		—	45	—		f = 20 kHz; C_{OUT} = 1.0 µF; C_{BYP} = 0.1 µF
Current Limit	I_{LIM}	**300**	550	**950**	mA	V_{OUT} = 0V
Output Voltage Noise	e_N	—	30	—	$µV_{RMS}$	C_{OUT} = 1.0 µF; C_{BYP} = 0.01 µF; 10 Hz to 100 kHz

ELECTRICAL CHARACTERISTICS (CONTINUED)

Electrical Characteristics: V_{IN} = EN = V_{OUT} + 1.0V; higher of the two regulator outputs, $I_{OUTLDO1}$ = $I_{OUTLDO2}$ = 100 µA; C_{OUT1} = C_{OUT2} = 1 µF; C_{BYP} = 0.01 µF; T_J = 25°C, **bold** values valid for –40°C ≤ T_J ≤ +125°C, unless noted. (Note 1)

Parameter	Symbol	Min.	Typ.	Max.	Units	Conditions
Enable Inputs (EN)						
Enable Input Voltage	V_{IL}	—	—	**0.2**	V	Logic Low
	V_{IH}	**1.1**	—	—		Logic High
Enable Input Current	I_{IL}	—	0.01	1	µA	V_{IL} ≤ 0.2V
	I_{IH}	—	0.01	1		V_{IH} ≥ 1.0V
Turn-On Time						
Turn-On Time (LDO1 and LDO2)	t_{ON}	—	40	**100**	µs	C_{OUT} = 1.0 µF; No C_{BYP}
		—	45	**100**		C_{OUT} = 1.0 µF; C_{BYP} = 0.01 µF

Note 1: Specification for packaged product only.

2: Dropout voltage is defined as the input-to-output differential at which the output voltage drops 2% below its nominal V_{OUT}. For outputs below 2.3V, the dropout voltage is the input-to-output differential with the minimum input voltage 2.3V.

TEMPERATURE SPECIFICATIONS

Parameters	Sym.	Min.	Typ.	Max.	Units	Conditions
Temperature Ranges						
Operating Junction Temperature Range	T_J	–40	—	+125	°C	Note 1
Lead Temperature	T_{LEAD}	—	—	+260	°C	Soldering, 3 sec.
Storage Temperature	T_S	–65	—	+150	°C	—
Package Thermal Resistances						
Thermal Resistance, UDFN/WDFN 6-Ld	θ_{JA}	—	100	—	°C/W	—
Thermal Resistance, TSOT-23 6-Ld	θ_{JA}	—	235	—	°C/W	—

Note 1: The maximum allowable power dissipation is a function of ambient temperature, the maximum allowable junction temperature and the thermal resistance from junction to air (i.e., T_A, T_J, θ_{JA}). Exceeding the maximum allowable power dissipation will cause the device operating junction temperature to exceed the maximum +125°C rating. Sustained junction temperatures above +125°C can impact the device reliability.

2.0 TYPICAL PERFORMANCE CURVES

Note: The graphs and tables provided following this note are a statistical summary based on a limited number of samples and are provided for informational purposes only. The performance characteristics listed herein are not tested or guaranteed. In some graphs or tables, the data presented may be outside the specified operating range (e.g., outside specified power supply range) and therefore outside the warranted range.

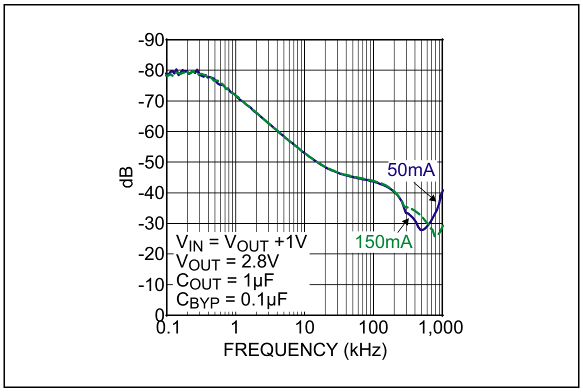


FIGURE 2-1: *Power Supply Rejection Ratio.*

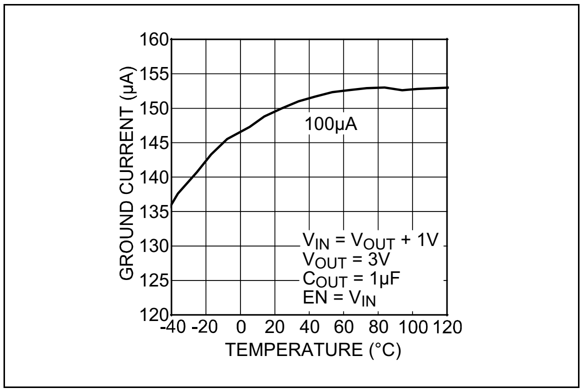


FIGURE 2-4: *Ground Current vs. Temperature.*

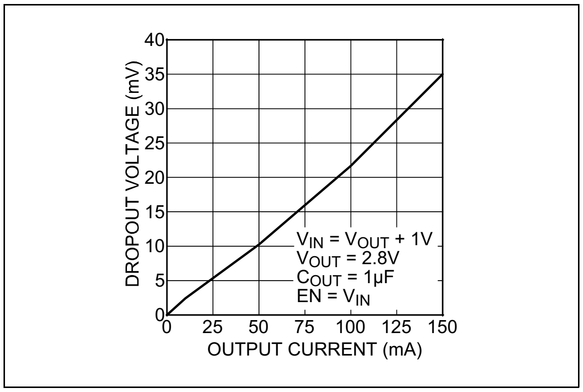


FIGURE 2-2: *Dropout Voltage vs. Output Current.*

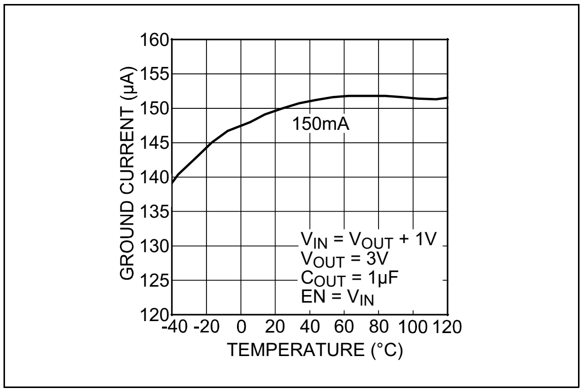


FIGURE 2-5: *Ground Current vs. Temperature.*

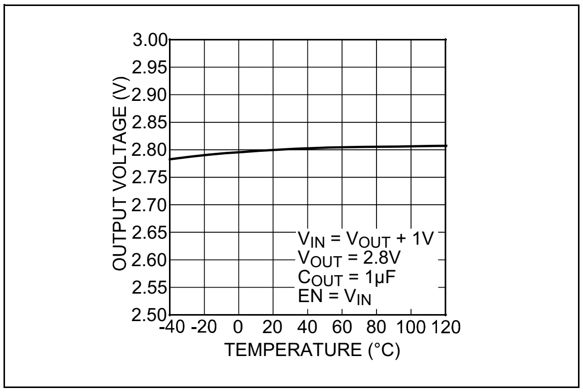


FIGURE 2-3: *Output Voltage vs. Temperature.*

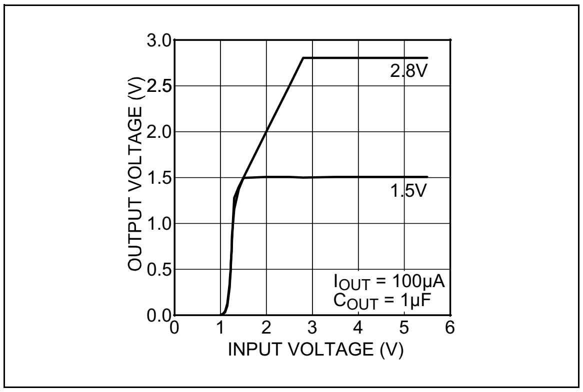


FIGURE 2-6: *Output Voltage vs. Input Voltage.*

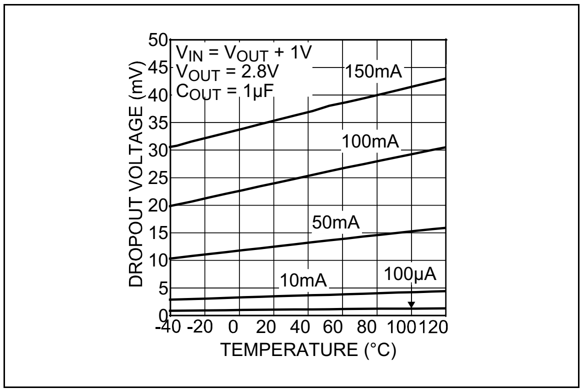


FIGURE 2-7: *Dropout Voltage vs. Temperature.*

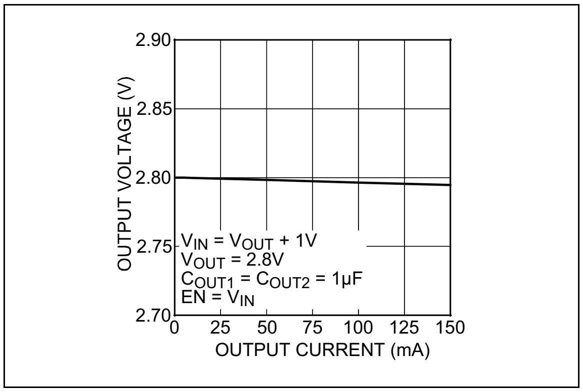


FIGURE 2-8: *Output Voltage vs. Output Current.*

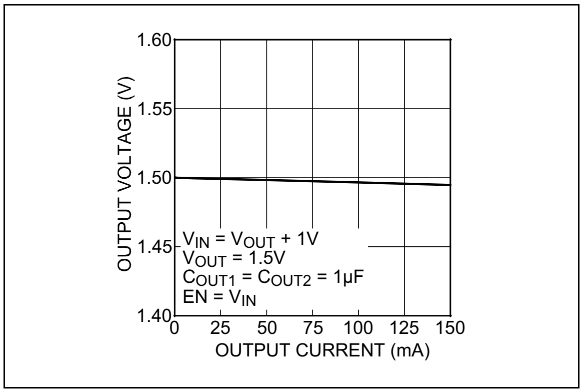


FIGURE 2-9: *Output Voltage vs. Output Current.*

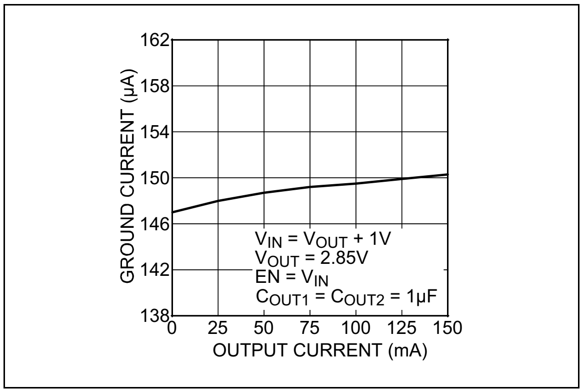


FIGURE 2-10: *Ground Current vs. Output Current.*

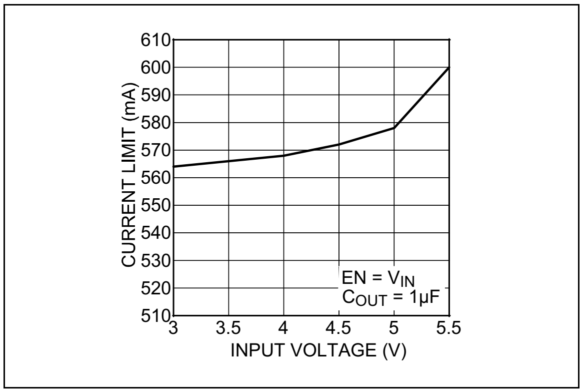


FIGURE 2-11: *Current Limit vs. Input Voltage.*

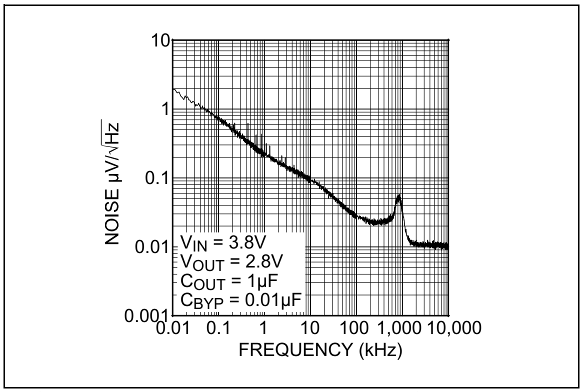


FIGURE 2-12: *Output Noise Spectral Density.*

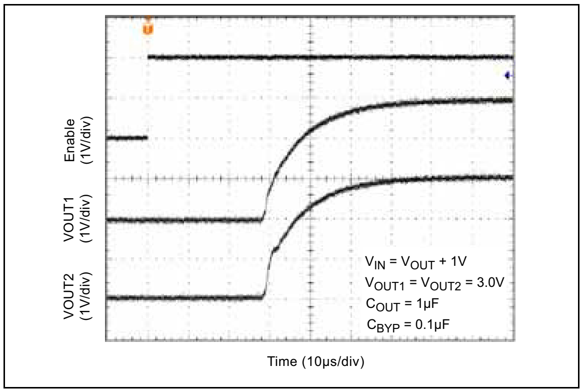


FIGURE 2-13: *Enable Turn-On.*

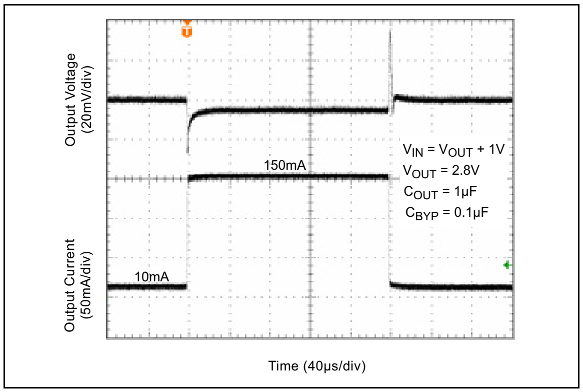


FIGURE 2-14: *Load Transient.*

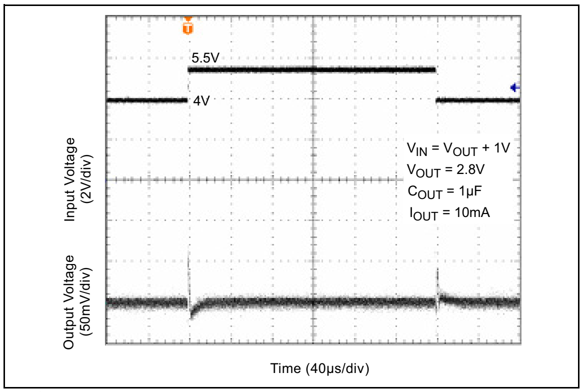


FIGURE 2-15: *Line Transient.*

3.0 PIN DESCRIPTIONS

The descriptions of the pins are listed in Table 3-1.

TABLE 3-1: PIN FUNCTION TABLE

Pin Number UDFN/WDFN	Pin Number TSOT	Pin Name	Description
1	3	VIN	Supply Input.
2	2	GND	Ground.
3	1	BYP	Reference Bypass: Connect external 0.01µF to GND to reduce output noise. May be left open.
4	6	EN	Enable Input (both regulators): Active-High Input. Logic High = On; Logic Low = Off; Do not leave floating.
5	5	VOUT2	Regulator Output: LDO2
6	4	VOUT1	Regulator Output: LDO1
HS Pad	—	ePAD	Exposed heatsink pad connected internally 3rto ground.

4.0 APPLICATION INFORMATION

4.1 Enable/Shutdown

The MIC5321 comes with a single active-high enable pin that allows both regulators to be disabled simultaneously. Forcing the enable pin low disables the regulator and sends it into a “zero” off-mode current state. In this state, current consumed by the regulator goes nearly to zero. Forcing the enable pin high enables the output voltage. The active-high enable pin uses CMOS technology and the enable pin cannot be left floating; a floating enable pin may cause an indeterminate state on the output.

4.2 Input Capacitor

The MIC5321 is a high-performance, high-bandwidth device. Therefore, it requires a well-bypassed input supply for optimal performance. A 1 µF capacitor is required from the input to ground to provide stability. Low-ESR ceramic capacitors provide optimal performance at a minimum of space. Additional high-frequency capacitors, such as small-valued NPO dielectric-type capacitors, help filter out high-frequency noise and are good practice in any RF-based circuit.

4.3 Output Capacitor

The MIC5321 requires an output capacitor of 1 µF or greater to maintain stability. The design is optimized for use with low-ESR ceramic chip capacitors. High ESR capacitors may cause high frequency oscillation. The output capacitor can be increased, but performance has been optimized for a 1 µF ceramic output capacitor and does not improve significantly with larger capacitance.

X7R/X5R dielectric-type ceramic capacitors are recommended because of their temperature performance. X7R-type capacitors change capacitance by 15% over their operating temperature range and are the most stable type of ceramic capacitors. Z5U and Y5V dielectric capacitors change value by as much as 50% and 60%, respectively, over their operating temperature ranges. To use a ceramic chip capacitor with Y5V dielectric, the value must be much higher than an X7R ceramic capacitor to ensure the same minimum capacitance over the equivalent operating temperature range.

4.4 Bypass Capacitor

A capacitor can be placed from the noise bypass pin to ground to reduce output voltage noise. The capacitor bypasses the internal reference. A 0.1 µF capacitor is recommended for applications that require low-noise outputs. The bypass capacitor can be increased, further reducing noise and improving PSRR. Turn-on time increases slightly with respect to bypass capacitance. A unique, quick-start circuit allows the MIC5321 to drive a large capacitor on the bypass pin without significantly slowing turn-on time. Refer to the Typical Performance Curves section for performance with different bypass capacitors.

4.5 No-Load Stability

Unlike many other voltage regulators, the MIC5321 will remain stable and in regulation with no load. This is especially important in CMOS RAM keep-alive applications.

4.6 Thermal Considerations

The MIC5321 is designed to provide 150 mA of continuous current for both outputs in a very small package. Maximum ambient operating temperature can be calculated based on the output current and the voltage drop across the part. Given that the input voltage is 3.3V, the output voltage is 2.8V for V_{OUT1}, 2.5V for V_{OUT2} and the output current equals 150 mA. The actual power dissipation of the regulator circuit can be determined using the equation:

EQUATION 4-1:

$$P_D = (V_{IN} - V_{OUT1}) \times I_{OUT1} + (V_{IN} - V_{OUT2}) \times I_{OUT2} + V_{IN} \times I_{GND}$$

Because this device is CMOS and the ground current is typically <150 µA over the load range, the power dissipation contributed by the ground current is less than 1% and can be ignored for this calculation.

EQUATION 4-2:

$$P_D = (3.3V - 2.8V) \times 150mA + (3.3V - 1.5V) \times 150mA$$

$$P_D = 0.345W$$

To determine the maximum ambient operating temperature of the package, use the junction-to-ambient thermal resistance of the device and the following basic equation:

EQUATION 4-3:

$$P_{D(MAX)} = \frac{T_{J(MAX)} - T_A}{\theta_{JA}}$$

Where:

$T_{J(MAX)}$ = 125°C, the max. junction temp. of the die.

θ_{JA} = Thermal resistance of 100°C/W.

The table below shows the junction-to-ambient thermal resistance for the UDFN package option.

Package	θ_{JA} Rec. Min. Footprint	θ_{JC}
6-Lead UDFN	100°C/W	2°C/W

Substituting P_D for $P_{D(MAX)}$ and solving for the ambient operating temperature will give the maximum operating conditions for the regulator circuit. The junction-to-ambient thermal resistance for the minimum footprint is 100°C/W.

The maximum power dissipation must not be exceeded for proper operation.

For example, when operating the MIC5321-MFYMT at an input voltage of 3.3V and 150 mA loads at each output with a minimum footprint layout, the maximum ambient operating temperature T_A can be determined as follows:

EQUATION 4-4:

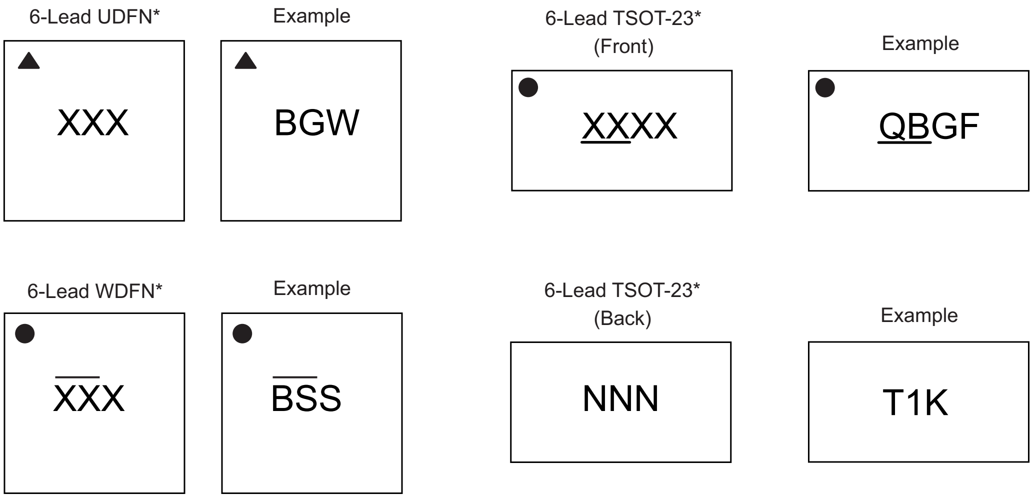
$$0.345W = (125°C - T_A)/(100°\mathrm{C/W})$$

$$T_A = 90.5°C$$

Therefore, a 2.8V/1.5V application with 150 mA at each output current can accept an ambient operating temperature of 90.5°C in a 1.6 mm x 1.6 mm UDFN package. For a full discussion of heat sinking and thermal effects on voltage regulators, refer to the “Regulator Thermals” section of Microchip’s Designing with Low-Dropout Voltage Regulators handbook.

5.0 PACKAGING INFORMATION

5.1 Package Marking Information



Note: MIC5321 has many voltage options and corresponding marking codes. The full list of them appear in Table 5-1 on the next page.

Legend:	XX...X	Product code or customer-specific information
	Y	Year code (last digit of calendar year)
	YY	Year code (last 2 digits of calendar year)
	WW	Week code (week of January 1 is week '01')
	NNN	Alphanumeric traceability code
	e3	Pb-free JEDEC® designator for Matte Tin (Sn)
	*	This package is Pb-free. The Pb-free JEDEC designator (e3) can be found on the outer packaging for this package.
	●, ▲, ▼	Pin one index is identified by a dot, delta up, or delta down (triangle mark).

Note: In the event the full Microchip part number cannot be marked on one line, it will be carried over to the next line, thus limiting the number of available characters for customer-specific information. Package may or may not include the corporate logo.

Underbar (_) symbol may not be to scale.

Note: If the full seven-character YYWWNNN code cannot fit on the package, the following truncated codes are used based on the available marking space:
6 Characters = YWWNNN; 5 Characters = WWNNN; 4 Characters = WNNN; 3 Characters = NNN;
2 Characters = NN; 1 Character = N

TABLE 5-1: MIC5321 PACKAGE MARKING CODES

Part Number	Marking	Voltage	Package
MIC5321-GFYMT	BGF	1.8V/1.5V	6-Lead 1.6 mm x 1.6 mm UDFN
MIC5321-GGYMT	BGG	1.8V/1.8V	6-Lead 1.6 mm x 1.6 mm UDFN
MIC5321-GWYMT	BGW	1.8V/1.6V	6-Lead 1.6 mm x 1.6 mm UDFN
MIC5321-JGYMT	BJG	2.5V/1.8V	6-Lead 1.6 mm x 1.6 mm UDFN
MIC5321-JJYMT	BJJ	2.5V/2.5V	6-Lead 1.6 mm x 1.6 mm UDFN
MIC5321-KDYMT	BKD	2.6V/1.85V	6-Lead 1.6 mm x 1.6 mm UDFN
MIC5321-KGYMT	BKG	2.6V/1.8V	6-Lead 1.6 mm x 1.6 mm UDFN
MIC5321-LLYMT	BLL	2.7V/2.7V	6-Lead 1.6 mm x 1.6 mm UDFN
MIC5321-MFYMT	BMF	2.8V/1.5V	6-Lead 1.6 mm x 1.6 mm UDFN
MIC5321-MGYMT	BMG	2.8V/1.8V	6-Lead 1.6 mm x 1.6 mm UDFN
MIC5321-MKYMT	BMK	2.8V/2.6V	6-Lead 1.6 mm x 1.6 mm UDFN
MIC5321-MMYMT	BMM	2.8V/2.8V	6-Lead 1.6 mm x 1.6 mm UDFN
MIC5321-NDYMT	BND	2.85V/1.85V	6-Lead 1.6 mm x 1.6 mm UDFN
MIC5321-NKYMT	BNK	2.85V/2.6V	6-Lead 1.6 mm x 1.6 mm UDFN
MIC5321-NNYMT	BNN	2.85V/2.85V	6-Lead 1.6 mm x 1.6 mm UDFN
MIC5321-OFYMT	BOF	2.9V/1.5V	6-Lead 1.6 mm x 1.6 mm UDFN
MIC5321-OGYMT	BOG	2.9V/1.8V	6-Lead 1.6 mm x 1.6 mm UDFN
MIC5321-OOYMT	BOO	2.9V/2.9V	6-Lead 1.6 mm x 1.6 mm UDFN
MIC5321-PGYMT	BPG	3.0V/1.8V	6-Lead 1.6 mm x 1.6 mm UDFN
MIC5321-PJYMT	BPJ	3.0V/2.5V	6-Lead 1.6 mm x 1.6 mm UDFN
MIC5321-PKYMT	BPK	3.0V/2.6V	6-Lead 1.6 mm x 1.6 mm UDFN
MIC5321-PMYMT	BPM	3.0V/2.8V	6-Lead 1.6 mm x 1.6 mm UDFN
MIC5321-PNYMT	BPN	3.0V/2.85V	6-Lead 1.6 mm x 1.6 mm UDFN
MIC5321-PPYMT	BPP	3.0V/3.0V	6-Lead 1.6 mm x 1.6 mm UDFN
MIC5321-SFYMT	BSF	3.3V/1.5V	6-Lead 1.6 mm x 1.6 mm UDFN
MIC5321-SGYMT	BSG	3.3V/1.8V	6-Lead 1.6 mm x 1.6 mm UDFN
MIC5321-SJYMT	BSJ	3.3V/2.5V	6-Lead 1.6 mm x 1.6 mm UDFN
MIC5321-SKYMT	BSK	3.3V/2.6V	6-Lead 1.6 mm x 1.6 mm UDFN
MIC5321-SLYMT***	BSL	3.3V/2.7V	6-Lead 1.6 mm x 1.6 mm UDFN
MIC5321-SMYMT	BSM	3.3V/2.8V	6-Lead 1.6 mm x 1.6 mm UDFN
MIC5321-SNYMT	BSN	3.3V/2.85V	6-Lead 1.6 mm x 1.6 mm UDFN
MIC5321-SOYMT	BSO	3.3V/2.9V	6-Lead 1.6 mm x 1.6 mm UDFN
MIC5321-SPYMT	BSP	3.3V/3.0V	6-Lead 1.6 mm x 1.6 mm UDFN
MIC5321-SRYMT	BSR	3.3V/3.2V	6-Lead 1.6 mm x 1.6 mm UDFN
MIC5321-SSYMT	BSS	3.3V/3.3V	6-Lead 1.6 mm x 1.6 mm UDFN
MIC5321-MFYML	$\overline{\text{BM}}$F	2.8V/1.5V	6-Lead 1.6 mm x 1.6 mm UDFN
MIC5321-MGYML	$\overline{\text{BM}}$G	2.8V/1.8V	6-Lead 1.6 mm x 1.6 mm UDFN
MIC5321-MMYML	$\overline{\text{BM}}$M	2.8V/2.8V	6-Lead 1.6 mm x 1.6 mm UDFN
MIC5321-PPYML	$\overline{\text{BP}}$P	3.0V/3.0V	6-Lead 1.6 mm x 1.6 mm UDFN
MIC5321-GFYD6	$\underline{\text{QB}}$GF	1.8V/1.5V	6-Lead 1.6 mm x 1.6 mm WDFN
MIC5321-GGYD6	$\underline{\text{QB}}$GG	1.8V/1.8V	6-Lead 1.6 mm x 1.6 mm WDFN
MIC5321-GWYD6***	$\underline{\text{QB}}$GW	1.8V/1.6V	6-Lead 1.6 mm x 1.6 mm WDFN
MIC5321-JGYD6***	$\underline{\text{QB}}$JG	2.5V/1.8V	6-Lead 1.6 mm x 1.6 mm WDFN
MIC5321-JJYD6***	$\underline{\text{QB}}$JJ	2.5V/2.5V	6-Lead 1.6 mm x 1.6 mm WDFN

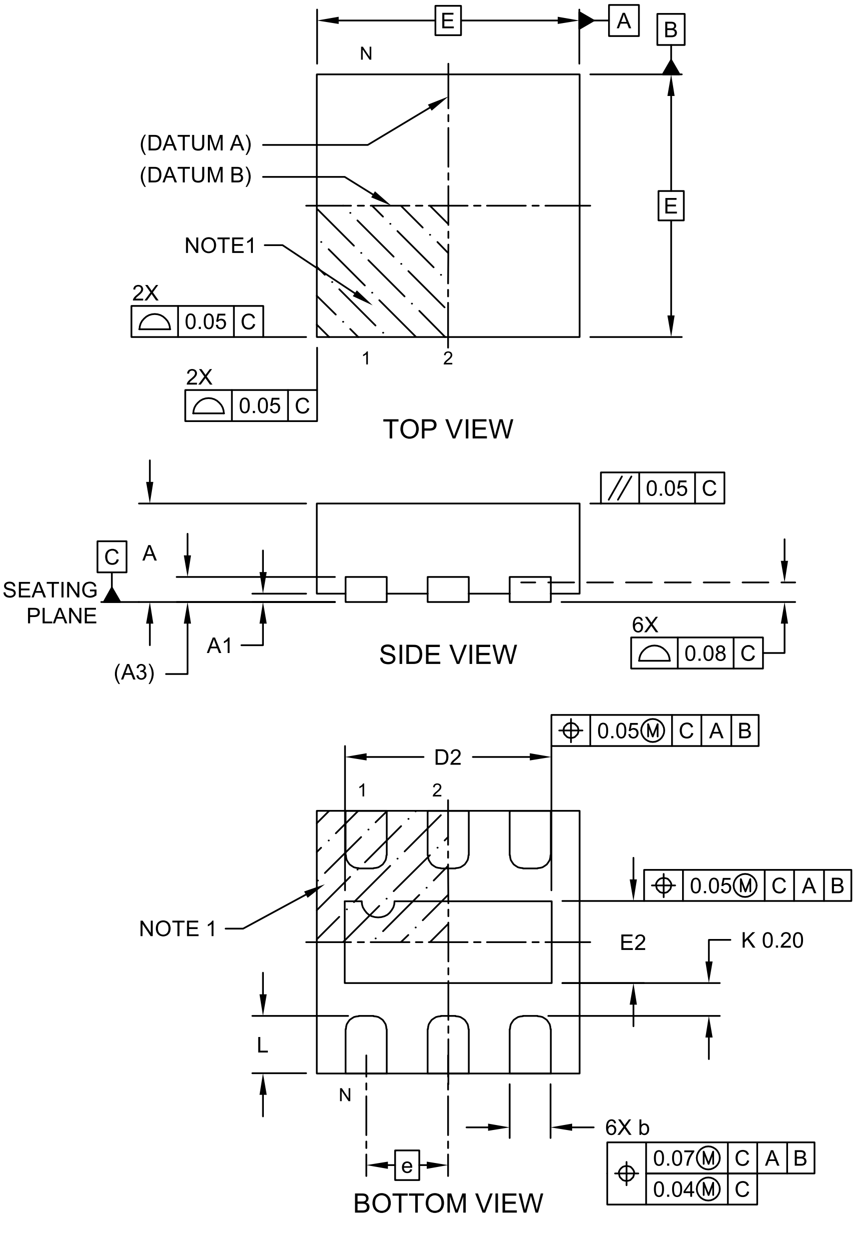
TABLE 5-1: MIC5321 PACKAGE MARKING CODES (CONTINUED)

Part Number	Marking	Voltage	Package
MIC5321-KDYD6***	QBKD	2.6V/1.85V	6-Lead TSOT-23
MIC5321-KGYD6***	QBKG	2.6V/1.8V	6-Lead TSOT-23
MIC5321-LLYD6	QBLL	2.7V/2.7V	6-Lead TSOT-23
MIC5321-MFYD6	QBMF	2.8V/1.5V	6-Lead TSOT-23
MIC5321-MGYD6	QBMG	2.8V/1.8V	6-Lead TSOT-23
MIC5321-MKYD6	QBMK	2.8V/2.6V	6-Lead TSOT-23
MIC5321-MMYD6	QBMM	2.8V/2.8V	6-Lead TSOT-23
MIC5321-NDYD6***	QBND	2.85V/1.85V	6-Lead TSOT-23
MIC5321-NKYD6***	QBNK	2.85V/2.6V	6-Lead TSOT-23
MIC5321-NNYD6***	QBNN	2.85V/2.85V	6-Lead TSOT-23
MIC5321-OFYD6***	QBOF	2.9V/1.5V	6-Lead TSOT-23
MIC5321-OGYD6***	QBOG	2.9V/1.8V	6-Lead TSOT-23
MIC5321-OOYD6***	QBOO	2.9V/2.9V	6-Lead TSOT-23
MIC5321-PGYD6	QBPG	3.0V/1.8V	6-Lead TSOT-23
MIC5321-PJYD6***	QBPJ	3.0V/2.5V	6-Lead TSOT-23
MIC5321-PKYD6***	QBPK	3.0V/2.6V	6-Lead TSOT-23
MIC5321-PMYD6***	QBPM	3.0V/2.8V	6-Lead TSOT-23
MIC5321-PNYD6***	QBPN	3.0V/2.85V	6-Lead TSOT-23
MIC5321-PPYD6	QBPP	3.0V/3.0V	6-Lead TSOT-23
MIC5321-SFYD6***	QBSF	3.3V/1.5V	6-Lead TSOT-23
MIC5321-SGYD6***	QBSG	3.3V/1.8V	6-Lead TSOT-23
MIC5321-SJYD6	QBSJ	3.3V/2.5V	6-Lead TSOT-23
MIC5321-SKYD6***	QBSK	3.3V/2.6V	6-Lead TSOT-23
MIC5321-SLYD6***	QBSL	3.3V/2.7V	6-Lead TSOT-23
MIC5321-SMYD6***	QBSM	3.3V/2.8V	6-Lead TSOT-23
MIC5321-SNYD6***	QBSN	3.3V/2.85V	6-Lead TSOT-23
MIC5321-SOYD6***	QBSO	3.3V/2.9V	6-Lead TSOT-23
MIC5321-SPYD6***	QBSP	3.3V/3.0V	6-Lead TSOT-23
MIC5321-SRYD6***	QBSR	3.3V/3.2V	6-Lead TSOT-23
MIC5321-SSYD6	QBSS	3.3V/3.3V	6-Lead TSOT-23

6-Lead 1.6 mm x 1.6 mm UDFN Package Outline and Recommended Land Pattern

6-Lead Ultra Thin Plastic Dual Flat, No Lead (HKA) - 1.6x1.6x0.6 mm Body [UDFN] With 1.26x0.50 mm Exposed Pad; Micrel Legacy Package TDFN1616-6LD-PL-1

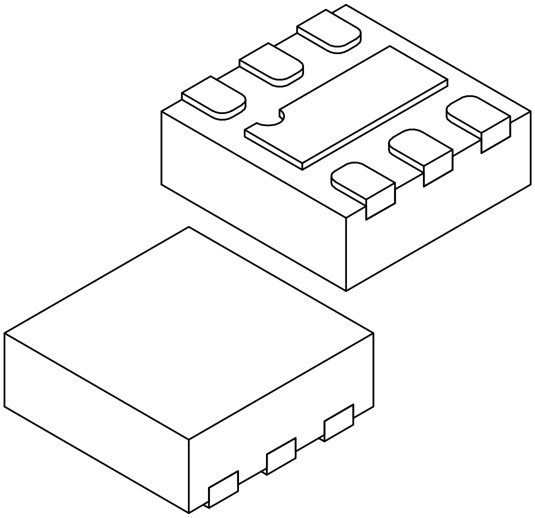
Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



Microchip Technology Drawing C04-1154 Rev A Sheet 1 of 2

6-Lead Ultra Thin Plastic Dual Flat, No Lead (HKA) - 1.6x1.6x0.6 mm Body [UDFN] With 1.26x0.50 mm Exposed Pad; Micrel Legacy Package TDFN1616-6LD-PL-1

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



	Units	MILLIMETERS		
	Dimension Limits	MIN	NOM	MAX
Number of Terminals	N		6	
Pitch	e		0.50 BSC	
Overall Height	A	0.50	0.55	0.60
Standoff	A1	0.00	0.02	0.05
Terminal Thickness	A3		0.152 REF	
Overall Length	D		1.60 BSC	
Exposed Pad Length	D2	1.21	1.26	1.31
Overall Width	E		1.60 BSC	
Exposed Pad Width	E2	0.45	0.50	0.55
Terminal Width	b	0.20	0.25	0.30
Terminal Length	L	0.30	0.35	0.40
Terminal-to-Exposed-Pad	K	0.20	–	–

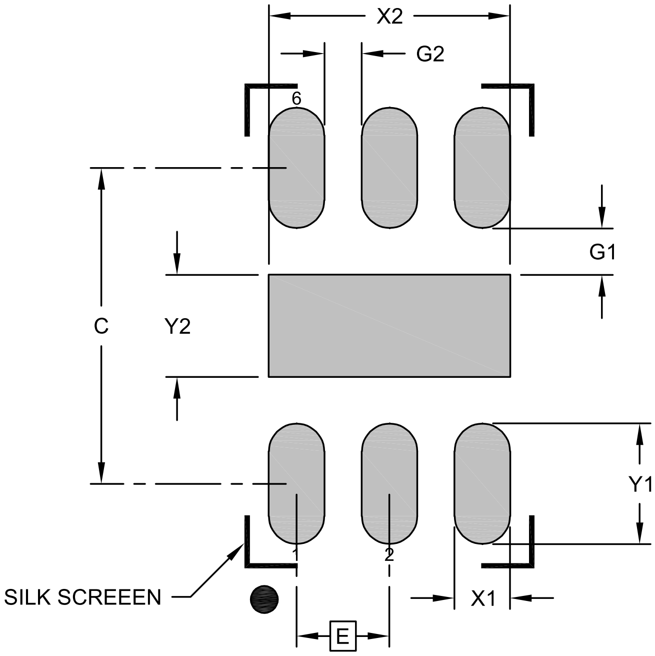
Notes:

1. Pin 1 visual index feature may vary, but must be located within the hatched area.
2. Package is saw singulated
3. Dimensioning and tolerancing per ASME Y14.5M
   BSC: Basic Dimension. Theoretically exact value shown without tolerances.
   REF: Reference Dimension, usually without tolerance, for information purposes only.

Microchip Technology Drawing C04-1154 Rev A Sheet 2 of 2

6-Lead Ultra Thin Plastic Dual Flat, No Lead (HKA) - 1.6x1.6x0.6 mm Body [UDFN] With 1.26x0.50 mm Exposed Pad; Micrel Legacy Package TDFN1616-6LD-PL-1

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



RECOMMENDED LAND PATTERN

	Units	MILLIMETERS		
	Dimension Limits	MIN	NOM	MAX
Contact Pitch	E	0.50 BSC		
Center Pad Width	X2			1.30
Center Pad Length	Y2			0.55
Contact Pad Spacing	C		1.70	
Contact Pad Width (X6)	X1			0.30
Contact Pad Length (X6)	Y1			0.65
Contact Pad to Center Pad (X6)	G1	0.25		
Contact Pad to Contact Pad (X4)	G2	0.20		

Notes:

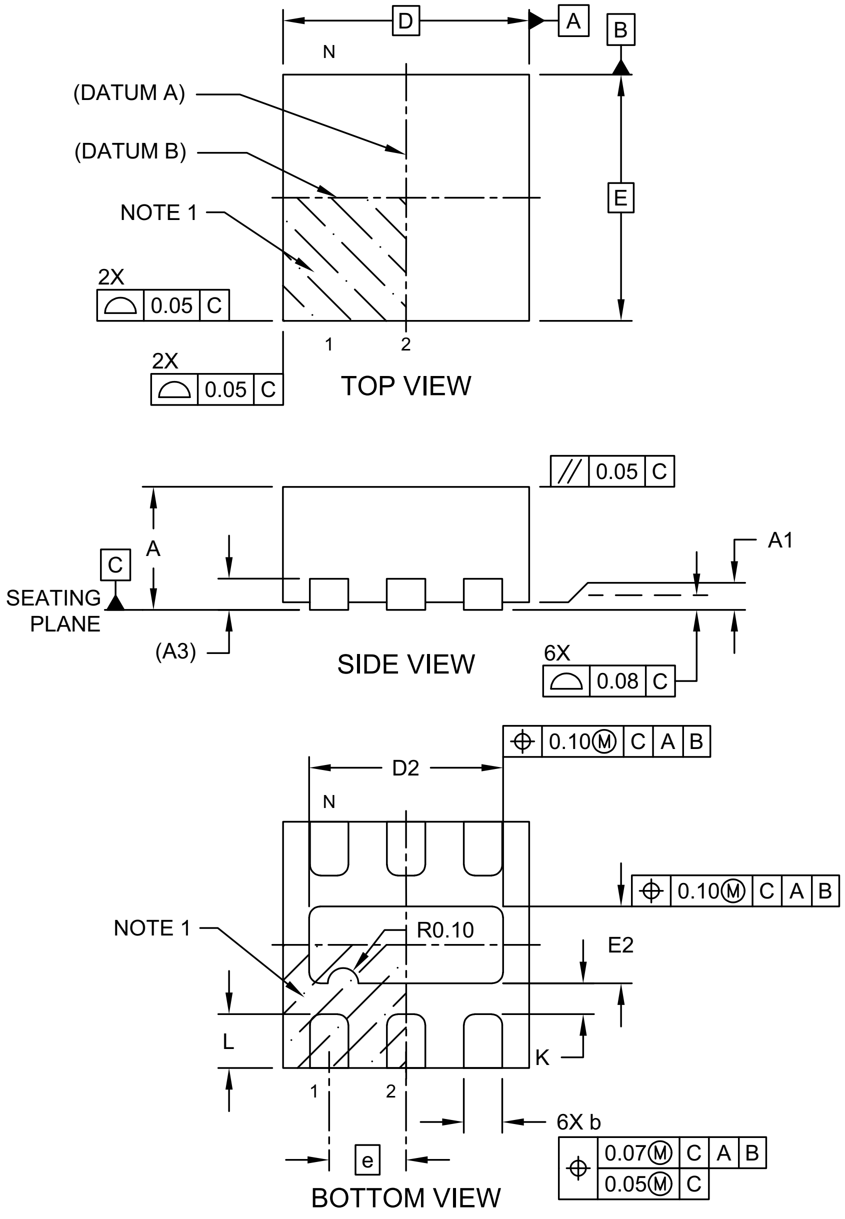
1. Dimensioning and tolerancing per ASME Y14.5M
   BSC: Basic Dimension. Theoretically exact value shown without tolerances.

Microchip Technology Drawing C04-3154 Rev A

6-Lead 1.6 mm x 1.6 mm WDFN Package Outline and Recommended Land Pattern

6-Lead Very, Very Thin Dual Flat, No Lead Package (K3A) - 1.6x1.6x0.8 mm Body [WDFN] With 1.26x0.5 mm Exposed Pad; Micrel Legacy Package Code DFN1616-6LD-PL-1

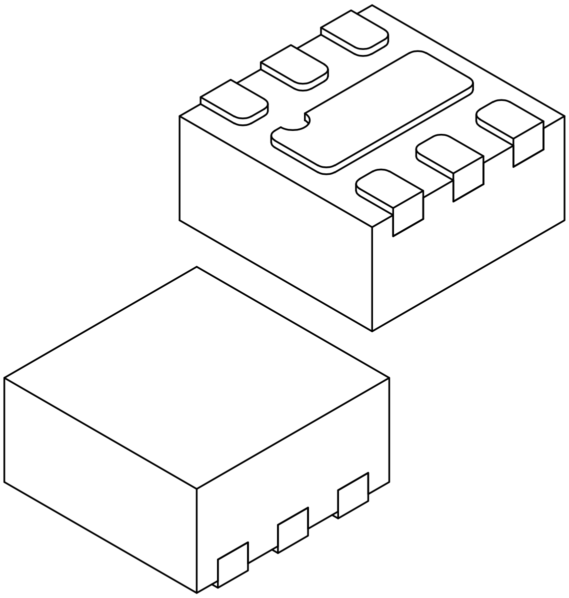
Note:	For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



Microchip Technology Drawing C04-1015 Rev A Sheet 1 of 2

6-Lead Very, Very Thin Dual Flat, No Lead Package (K3A) - 1.6x1.6x0.8 mm Body [WDFN] With 1.26x0.5 mm Exposed Pad; Micrel Legacy Package Code DFN1616-6LD-PL-1

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Number of Terminals	N		6	
Pitch	e		0.50 BSC	
Overall Height	A	0.70	0.75	0.80
Standoff	A1	0.00	0.02	0.05
Terminal Thickness	A3		0.203 REF	
Overall Length	D		1.60 BSC	
Exposed Pad Length	D2	1.21	1.26	1.31
Overall Width	E		1.60 BSC	
Exposed Pad Width	E2	0.45	0.50	0.55
Terminal Width	b	0.20	0.25	0.30
Terminal Length	L	0.30	0.35	0.40
Terminal-to-Exposed-Pad	K	0.20	–	–

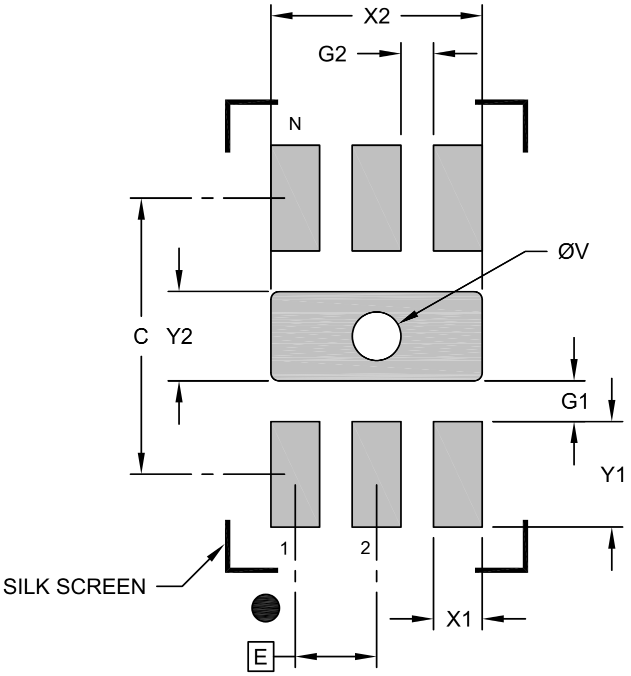
Notes:

1. Pin 1 visual index feature may vary, but must be located within the hatched area.
2. Package is saw singulated
3. Dimensioning and tolerancing per ASME Y14.5M
   BSC: Basic Dimension. Theoretically exact value shown without tolerances.
   REF: Reference Dimension, usually without tolerance, for information purposes only.

Microchip Technology Drawing C04-1015 Rev A Sheet 2 of 2

6-Lead Very, Very Thin Dual Flat, No Lead Package (K3A) - 1.6x1.6x0.8 mm Body [WDFN] With 1.26x0.5 mm Exposed Pad; Micrel Legacy Package Code DFN1616-6LD-PL-1

Note:	For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



RECOMMENDED LAND PATTERN

Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Contact Pitch	E		0.50 BSC	
Center Pad Width	X2			1.30
Center Pad Length	Y2			0.30
Contact Pad Spacing	C		1.70	
Contact Pad Width (X6)	X1			0.30
Contact Pad Length (X6)	Y1			1.30
Contact Pad to Center Pad (X6)	G1	0.25		
Contact Pad to Contact Pad (X4)	G2	0.20		
Thermal Via Diameter	V		0.30	

Notes:

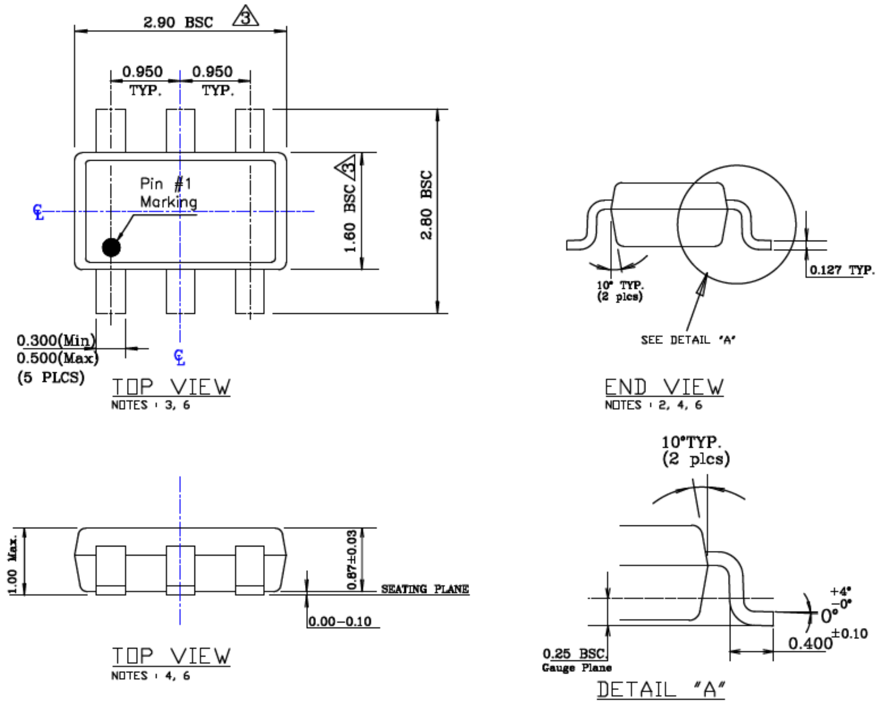
1. Dimensioning and tolerancing per ASME Y14.5M
   BSC: Basic Dimension. Theoretically exact value shown without tolerances.
2. For best soldering results, thermal vias, if used, should be filled or tented to avoid solder loss during reflow process

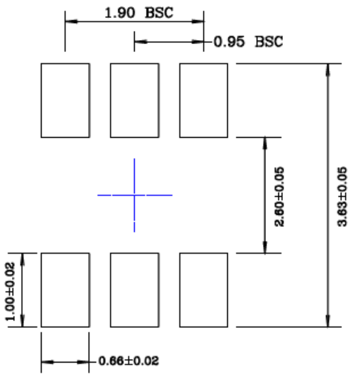
Microchip Technology Drawing C04-3015 Rev A

6-Lead Thin SOT-23 Package Outline and Recommended Land Pattern

TITLE
6 LEAD TSOT PACKAGE OUTLINE & RECOMMENDED LAND PATTERN

DRAWING #	TSOT-6LD-PL-1	**UNIT**	MM





RECOMMENDED LAND PATTERN

NOTE:

1. Dimensions and tolerances are as per ANSI Y14.5M, 1994.
2. Die is facing up for mold. Die is facing down for trim/form, ie. reverse trim/form.

△3 Dimensions are exclusive of mold flash and gate burr.

4. The footlength measuring is based on the gauge plane method.
5. All specification comply to Jedec Spec MO193 Issue C.
6. All dimensions are in millimeters.

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging.

APPENDIX A: REVISION HISTORY

Revision A (May 2022)

- Converted Micrel document MIC5321 to Microchip data sheet DS20006678A.
- Minor text changes throughout.

NOTES:

PRODUCT IDENTIFICATION SYSTEM

To order or obtain information, e.g., on pricing or delivery, contact your local Microchip representative or sales office.

Part Number	-XX	X	XX	-XX
Device	Output Voltages	Temp. Range	Package	Media Type

Device: MIC5321: High-Performance, Dual 150 mA µCap Ultra-Low Dropout Regulator

Output Voltages:

GF = 1.8V/1.5V (UDFN & TSOT options only)
GG = 1.8V/1.8V (UDFN & TSOT options only)
GW = 1.8V/1.6V (UDFN & TSOT options only)
JG = 2.5V/1.8V (UDFN & TSOT options only)
JJ = 2.5V/2.5V (UDFN & TSOT options only)
KD = 2.6V/1.85V (UDFN & TSOT options only)
KG = 2.6V/1.8V (UDFN & TSOT options only)
LL = 2.7V/2.7V (UDFN & TSOT options only)
MF = 2.8V/1.5V (All package options)
MG = 2.8V/1.8V (All package options)
MK = 2.8V/2.6V (UDFN & TSOT options only)
MM = 2.8V/2.8V (All package options)
ND = 2.85V/1.85V (UDFN & TSOT options only)
NK = 2.85V/2.6V (UDFN & TSOT options only)
NN = 2.85V/2.85V (UDFN & TSOT options only)
OF = 2.9V/1.5V (UDFN & TSOT options only)
OG = 2.9V/1.8V (UDFN & TSOT options only)
OO = 2.9V/2.9V (UDFN & TSOT options only)
PG = 3.0V/1.8V (UDFN & TSOT options only)
PJ = 3.0V/2.5V (UDFN & TSOT options only)
PK = 3.0V/2.6V (UDFN & TSOT options only)
PM = 3.0V/2.8V (UDFN & TSOT options only)
PN = 3.0V/2.85V (UDFN & TSOT options only)
PP = 3.0V/3.0V (All package options)
SF = 3.3V/1.5V (UDFN & TSOT options only)
SG = 3.3V/1.8V (UDFN & TSOT options only)
SJ = 3.3V/2.5V (UDFN & TSOT options only)
SK = 3.3V/2.6V (UDFN & TSOT options only)
SL = 3.3V/2.7V (UDFN & TSOT options only)
SM = 3.3V/2.8V (UDFN & TSOT options only)
SN = 3.3V/2.85V (UDFN & TSOT options only)
SO = 3.3V/2.9V (UDFN & TSOT options only)
SP = 3.3V/3.0V (UDFN & TSOT options only)
SR = 3.3V/3.2V (UDFN & TSOT options only)
SS = 3.3V/3.3V (UDFN & TSOT options only)

Temperature Range: Y = –40°C to +125°C

Package:

D6 = 6-Lead Thin SOT-23
ML = 6-Lead 1.6 mm x 1.6 mm WDFN
MT = 6-Lead 1.6 mm x 1.6 mm UDFN

Media Type:

TR = 3,000/Reel (TSOT-23 option only)
TR = 5,000/Reel (UDFN & WDFN options only)

Examples:

a) MIC5321-GGYMT-TR:	MIC5321, 1.8V/1.8V Output Voltages, –40°C to +125°C Temp. Range, 6-Lead UDFN, 5,000/Reel
b) MIC5321-KGYD6-TR:	MIC5321, 2.6V/1.8V Output Voltages, –40°C to +125°C Temp. Range, 6-Lead TSOT-23, 3,000/Reel
c) MIC5321-MMYML-TR:	MIC5321, 2.8V/2.8V Output Voltages, –40°C to +125°C Temp. Range, 6-Lead WDFN, 5,000/Reel
d) MIC5321-OFYMT-TR:	MIC5321, 2.9V/1.5V Output Voltages, –40°C to +125°C Temp. Range, 6-Lead UDFN, 5,000/Reel
e) MIC5321-SKYD6-TR:	MIC5321, 3.3V/2.6V Output Voltages, –40°C to +125°C Temp. Range, 6-Lead TSOT-23, 3,000/Reel
f) MIC5321-PPYML-TR:	MIC5321, 3.0V/3.0V Output Voltages, –40°C to +125°C Temp. Range, 6-Lead WDFN, 5,000/Reel

Note 1: Tape and Reel identifier only appears in the catalog part number description. This identifier is used for ordering purposes and is not printed on the device package. Check with your Microchip Sales Office for package availability with the Tape and Reel option.

NOTES:

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