PIC18F6393/6493/8393/8493
Data Sheet

64/80-Pin High Performance, Flash Microcontrollers with LCD Driver, 12-Bit ADC and nanoWatt Technology

Preliminary

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PIC18F6393/6493/8393/8493

64/80-Pin High-Performance, Flash Microcontrollers with LCD Driver, 12-Bit ADC and nanoWatt Technology

LCD Driver Module Features:

- Direct Driving of LCD Panel
- Up to 192 Pixels: Software Selectable
- Programmable LCD Timing module:
  - Multiple LCD timing sources available
  - Up to four commons: Static, 1/2, 1/3 or 1/4 multiplex
  - Static, 1/2 or 1/3 bias configuration
- Can Drive LCD Panel while in Sleep mode for Low-Power Operation

Power-Managed Modes:

- Run: CPU On, Peripherals On
- Idle: CPU Off, Peripherals On
- Sleep: CPU Off, Peripherals Off
- Run mode Current Down to 14 μA Typical
- Idle mode Currents Down to 5.8 μA Typical
- Sleep mode Currents Down to 0.1 μA Typical
- Timer1 Oscillator: 1.8 μA, 32 kHz, 2V
- Watchdog Timer: 2.1 μA Typical
- Two-Speed Oscillator Start-up

Flexible Oscillator Structure:

- Four Crystal modes:
  - LP: Up to 200 kHz
  - XT: Up to 4 MHz
  - HS: Up to 40 MHz
  - HSPLL: 4-10 MHz (16-40 MHz internal)
- 4x Phase Lock Loop (available for crystal and internal oscillators)
- Two External RC modes, Up to 4 MHz
- Two External Clock modes, Up to 40 MHz
- Internal Oscillator Block:
  - Eight selectable frequencies, from 31 kHz to 8 MHz
  - Provides a complete range of clock speeds from 31 kHz to 32 MHz when used with PLL
  - User-tunable to compensate for frequency drift
- Secondary Oscillator Using Timer1 at 32 kHz
- Fail-Safe Clock Monitor:
  - Allows for safe shutdown of device if primary or secondary clock fails

Peripheral Highlights:

- 12-Bit, Up to 12-Channel Analog-to-Digital (A/D) Converter module:
  - Auto-acquisition capability
  - Conversion available during Sleep
- High-Current Sink/Source 25 mA/25 mA
- Four External Interrupts
- Four Input Change Interrupts
- Four 8-Bit/16-Bit Timer/Counter modules
- Real-Time Clock (RTC) Software module:
  - Configurable 24-hour clock, calendar, automatic 100-year or 12,800-year, day-of-week calculator
  - Uses Timer1
- Up to Two Capture/Compare/PWM (CCP) modules
- Master Synchronous Serial Port (MSSP) module Supporting Three-Wire SPI (all four modes) and I²C™ Master and Slave modes
- Addressable USART module:
  - Supports RS-485 and RS-232
- Enhanced Addressable USART module:
  - Supports RS-485, RS-232 and LIN 1.2
  - Auto-wake-up on Start bit
  - Auto-Baud Detect
- Dual Analog Comparators with Input Multiplexing

Special Microcontroller Features:

- C Compiler Optimized Architecture:
  - Optional extended instruction set designed to optimize re-entrant code
- 1000 Erase/Write Cycle Flash Program Memory Typical
- Flash Retention: 100 Years Typical
- Priority Levels for Interrupts
- 8 x 8 Single-Cycle Hardware Multiplier
- Extended Watchdog Timer (WDT):
  - Programmable period from 4 ms to 132s
  - 2% stability over V_{DD} and temperature
- In-Circuit Serial Programming™ (ICSP™) via Two Pins
- In-Circuit Debug (ICD) via Two Pins
- Wide Operating Voltage Range: 2.0V to 5.5V

> **Note:** This document is supplemented by the *"PIC18F6390/6490/8390/8490 Data Sheet"* (DS39629). See **Section 1.0 "Device Overview"**.

PIC18F6393/6493/8393/8493

| Device | Program Memory | | Data Memory | I/O | LCD (pixel) | 12-Bit A/D (channels) | CCP (PWM) | MSSP | | EUSART/AUSART | Comparators | Timers 8/16-Bit |
	Flash (bytes)	# Single-Word Instructions	SRAM (bytes)					SPI	Master I²C™			
PIC18F6393	8K	4096	768	50	128	12	2	Y	Y	1/1	2	1/3
PIC18F6493	16K	8192	768	50	128	12	2	Y	Y	1/1	2	1/3
PIC18F8393	8K	4096	768	66	192	12	2	Y	Y	1/1	2	1/3
PIC18F8493	16K	8192	768	66	192	12	2	Y	Y	1/1	2	1/3

Pin Diagrams

64-Pin TQFP

PIC18F6393
PIC18F6493

Top pins (64–49):
- 64 LCDBIAS3
- 63 COM0
- 62 RE4/COM1
- 61 RE5/COM2
- 60 RE6/COM3
- 59 RE7/CCP2(1)/SEG31
- 58 RD0/SEG0
- 57 VDD
- 56 VSS
- 55 RD1/SEG1
- 54 RD2/SEG2
- 53 RD3/SEG3
- 52 RD4/SEG4
- 51 RD5/SEG5
- 50 RD6/SEG6
- 49 RD7/SEG7

Left pins (1–16):
- 1 LCDBIAS2
- 2 LCDBIAS1
- 3 RG0/SEG30
- 4 RG1/TX2/CK2/SEG29
- 5 RG2/RX2/DT2/SEG28
- 6 RG3/SEG27
- 7 MCLR/VPP/RG5
- 8 RG4/SEG26
- 9 VSS
- 10 VDD
- 11 RF7/SS/SEG25
- 12 RF6/AN11/SEG24
- 13 RF5/AN10/CVREF/SEG23
- 14 RF4/AN9/SEG22
- 15 RF3/AN8/SEG21
- 16 RF2/AN7/C1OUT/SEG20

Right pins (48–33):
- 48 RB0/INT0
- 47 RB1/INT1/SEG8
- 46 RB2/INT2/SEG9
- 45 RB3/INT3/SEG10
- 44 RB4/KBI0/SEG11
- 43 RB5/KBI1
- 42 RB6/KBI2/PGC
- 41 VSS
- 40 OSC2/CLKO/RA6
- 39 OSC1/CLKI/RA7
- 38 VDD
- 37 RB7/KBI3/PGD
- 36 RC5/SDO/SEG12
- 35 RC4/SDI/SDA
- 34 RC3/SCK/SCL
- 33 RC2/CCP1/SEG13

Bottom pins (17–32):
- 17 RF1/AN6/C2OUT/SEG19
- 18 RF0/AN5/SEG18
- 19 AVDD
- 20 AVSS
- 21 RA3/AN3/VREF+/SEG17
- 22 RA2/AN2/VREF-/SEG16
- 23 RA1/AN1
- 24 RA0/AN0
- 25 VSS
- 26 VDD
- 27 RA5/AN4/HLVDIN/SEG15
- 28 RA4/T0CKI/SEG14
- 29 RC1/T1OSI/CCP2(1)
- 30 RC0/T1OSO/T13CKI
- 31 RC6/TX1/CK1
- 32 RC7/RX1/DT1

Note 1: RE7 is the alternate pin for CCP2 multiplexing.

Pin Diagrams (Continued)

80-Pin TQFP

Top pins (80 → 61):
RH1/SEG46, RH0/SEG47, LCDBIAS3, COM0, RE4/COM1, RE5/COM2, RE6/COM3, RE7/CCP2[1]/SEG31, RD0/SEG0, VDD, VSS, RD1/SEG1, RD2/SEG2, RD3/SEG3, RD4/SEG4, RD5/SEG5, RD6/SEG6, RD7/SEG7, RJ0/SEG32, RJ1/SEG33

Left pins (1 → 20):
1 RH2/SEG45
2 RH3/SEG44
3 LCDBIAS2
4 LCDBIAS1
5 RG0/SEG30
6 RG1/TX2/CK2/SEG29
7 RG2/RX2/DT2/SEG28
8 RG3/SEG27
9 MCLR/VPP/RG5
10 RG4/SEG26
11 VSS
12 VDD
13 RF7/SS/SEG25
14 RF6/AN11/SEG24
15 RF5/AN10/CVREF/SEG23
16 RF4/AN9/SEG22
17 RF3/AN8/SEG21
18 RF2/AN7/C1OUT/SEG20
19 RH7/SEG43
20 RH6/SEG42

PIC18F8393
PIC18F8493

Right pins (60 → 41):
60 RJ2/SEG34
59 RJ3/SEG35
58 RB0/INT0
57 RB1/INT1/SEG8
56 RB2/INT2/SEG9
55 RB3/INT3/SEG10
54 RB4/KBI0/SEG11
53 RB5/KBI1
52 RB6/KBI2/PGC
51 VSS
50 OSC2/CLKO/RA6
49 OSC1/CLKI/RA7
48 VDD
47 RB7/KBI3/PGD
46 RC5/SDO/SEG12
45 RC4/SDI/SDA
44 RC3/SCK/SCL
43 RC2/CCP1/SEG13
42 RJ7/SEG36
41 RJ6/SEG37

Bottom pins (21 → 40):
21 RH5/SEG41
22 RH4/SEG40
23 RF1/AN6/C2OUT/SEG19
24 RF0/AN5/SEG18
25 AVDD
26 AVSS
27 RA3/AN3/VREF+/SEG17
28 RA2/AN2/VREF-/SEG16
29 RA1/AN1
30 RA0/AN0
31 VSS
32 VDD
33 RA5/AN4/HLVDIN/SEG15
34 RA4/T0CKI/SEG14
35 RC1/T1OSI/CCP2[1]
36 RC0/T1OSO/T13CKI
37 RC6/TX1/CK1
38 RC7/RX1/DT1
39 RJ4/SEG39
40 RJ5/SEG38

Note 1: RE7 is the alternate pin for CCP2 multiplexing.

PIC18F6393/6493/8393/8493

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NOTES:

Preliminary

1.0 DEVICE OVERVIEW

This document contains device-specific information for the following devices:

- PIC18F6393
- PIC18F8393
- PIC18F6493
- PIC18F8493

> **Note:** This data sheet documents only the devices' features and specifications that are in addition to the features and specifications of the PIC18F6390/6490/8390/8490 devices. For information on the features and specifications shared by the PIC18F6393/6493/8393/8493 and PIC18F6390/6490/8390/8490 devices, see the *"PIC18F6390/6490/8390/8490 Data Sheet"* (DS39629).

This family offers the advantages of all PIC18 microcontrollers – namely, high computational performance at an economical price. In addition to these features, the PIC18F6393/6493/8393/8493 family introduces design enhancements that make these microcontrollers a logical choice for many high-performance, power-sensitive applications.

1.1 Special Features

- **12-Bit A/D Converter:** This module incorporates programmable acquisition time, allowing for a channel to be selected and a conversion to be initiated without waiting for a sampling period and thus, reduces code overhead.

1.2 Details on Individual Family Members

Devices in the PIC18F6393/6493/8393/8493 family are available in 64-pin (PIC18F6X93) and 80-pin (PIC18F8X93) packages. Block diagrams for the two groups are shown in Figure 1-1 and Figure 1-2, respectively.

The devices are differentiated from each other in the following ways:

- I/O Ports:
  - 64-pin devices – 7 bidirectional ports
  - 80-pin devices – 9 bidirectional ports
- LCD Pixels:
  - 64-pin devices – 128 (32 SEGs x 4 COMs) pixels can be driven
  - 80-pin devices – 192 (48 SEGs x 4 COMs) pixels can be driven
- Flash Program Memory:
  - PIC18FX393 devices – 8 Kbytes
  - PIC18FX493 devices – 16 Kbytes

All other features for devices in this family are identical. These are summarized in Table 1-1.

The pinouts for all devices are listed in Table 1-2 and Table 1-3.

Like all Microchip PIC18 devices, members of the PIC18F6393/6493/8393/8493 family are available as both standard and low-voltage devices. Standard devices with Flash memory, designated with an "F" in the part number (such as PIC18F6393), accommodate an operating V_{DD} range of 4.2V to 5.5V. Low-voltage parts, designated by "LF" (such as PIC18LF6490), function over an extended V_{DD} range of 2.0V to 5.5V.
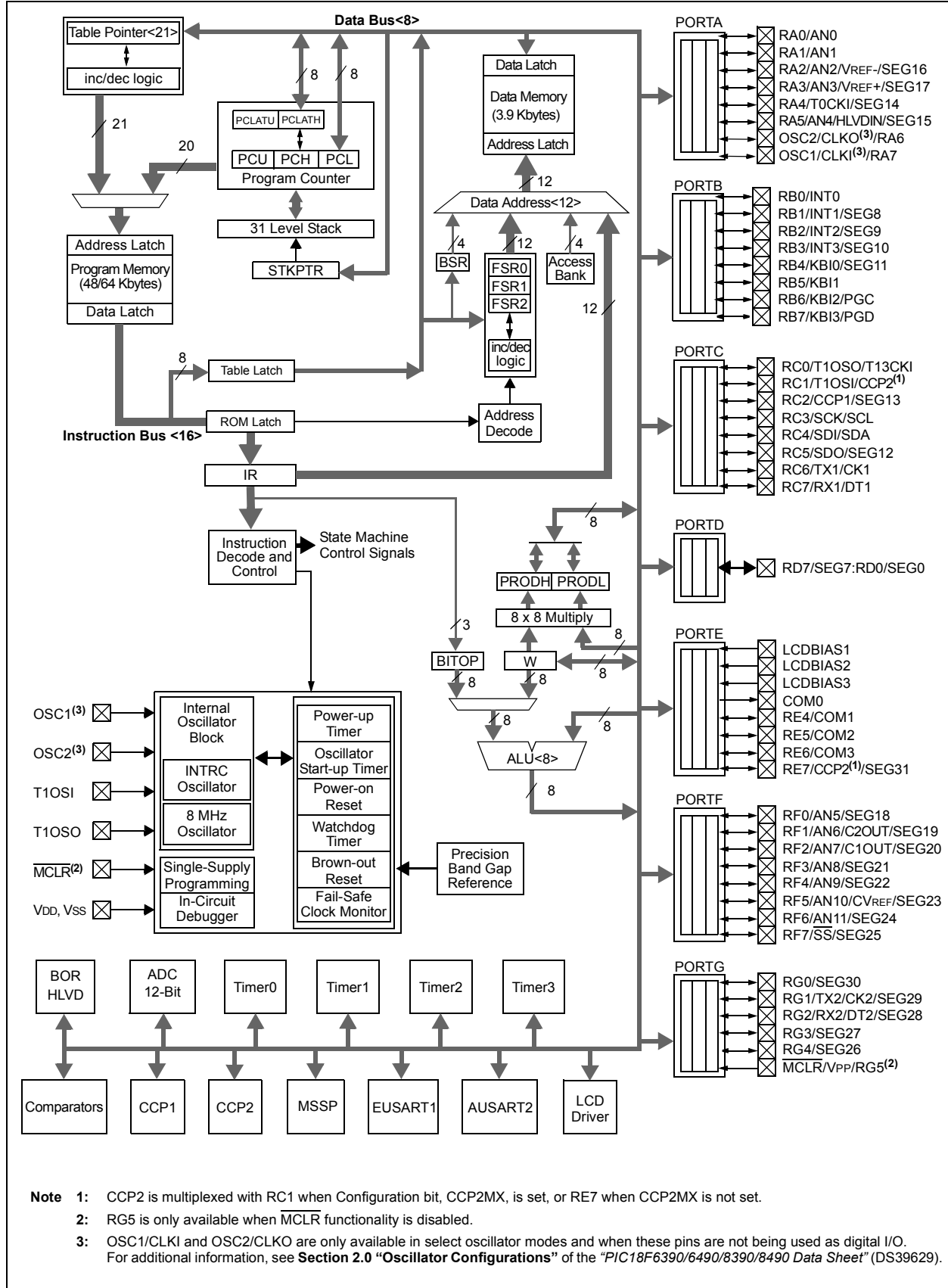
PIC18F6393/6493/8393/8493

TABLE 1-1: DEVICE FEATURES

Features	PIC18F6393	PIC18F6493	PIC18F8393	PIC18F8493
Operating Frequency	DC – 40 MHz	DC – 40 MHz	DC – 40 MHz	DC – 40 MHz
Program Memory (Bytes)	8K	16K	8K	16K
Program Memory (Instructions)	4096	8192	4096	8192
Data Memory (Bytes)	768	768	768	768
Interrupt Sources	22	22	22	22
I/O Ports	Ports A, B, C, D, E, F, G	Ports A, B, C, D, E, F, G	Ports A, B, C, D, E, F, G, H, J	Ports A, B, C, D, E, F, G, H, J
Number of Pixels the LCD Driver Can Drive	128 (32 SEGs x 4 COMs)	128 (32 SEGs x 4 COMs)	192 (48 SEGs x 4 COMs)	192 (48 SEGs x 4 COMs)
Timers	4	4	4	4
Capture/Compare/PWM Modules	2	2	2	2
Serial Communications	MSSP, AUSART, Enhanced USART	MSSP, AUSART, Enhanced USART	MSSP, AUSART, Enhanced USART	MSSP, AUSART, Enhanced USART
12-Bit Analog-to-Digital Module	12 Input Channels	12 Input Channels	12 Input Channels	12 Input Channels
Resets (and Delays)	POR, BOR, RESET Instruction, Stack Full, Stack Underflow (PWRT, OST), MCLR (optional), WDT	POR, BOR, RESET Instruction, Stack Full, Stack Underflow (PWRT, OST), MCLR (optional), WDT	POR, BOR, RESET Instruction, Stack Full, Stack Underflow (PWRT, OST), MCLR (optional), WDT	POR, BOR, RESET Instruction, Stack Full, Stack Underflow (PWRT, OST), MCLR (optional), WDT
Programmable Low-Voltage Detect	Yes	Yes	Yes	Yes
Programmable Brown-out Reset	Yes	Yes	Yes	Yes
Instruction Set	75 Instructions; 83 with Extended Instruction Set Enabled	75 Instructions; 83 with Extended Instruction Set Enabled	75 Instructions; 83 with Extended Instruction Set Enabled	75 Instructions; 83 with Extended Instruction Set Enabled
Packages	64-Pin TQFP	64-Pin TQFP	80-Pin TQFP	80-Pin TQFP

Preliminary

FIGURE 1-1: **PIC18F6X93 (64-PIN) BLOCK DIAGRAM**

PIC18F6393/6493/8393/8493

FIGURE 1-2: **PIC18F8X93 (80-PIN) BLOCK DIAGRAM**
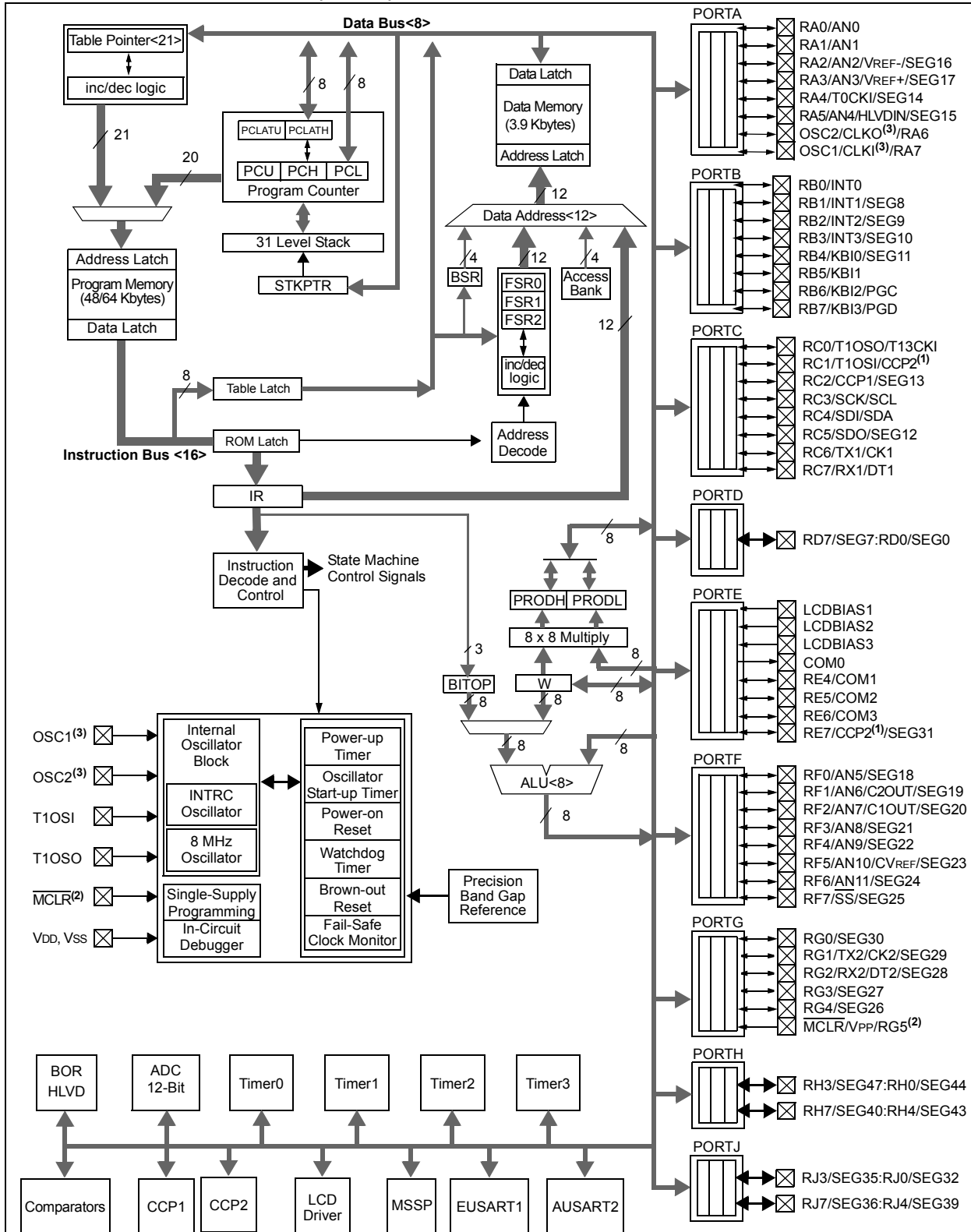
Note 1: CCP2 is multiplexed with RC1 when Configuration bit, CCP2MX, is set and RE7 when CCP2MX is not set.

2: RG5 is only available when $\overline{MCLR}$ functionality is disabled.

3: OSC1/CLKI and OSC2/CLKO are only available in select oscillator modes and when these pins are not being used as digital I/O. For additional information, see **Section 2.0 "Oscillator Configurations"** of the *"PIC18F6390/6490/8390/8490 Data Sheet"* (DS39629).

Preliminary

TABLE 1-2:   PIC18F6X93 PINOUT I/O DESCRIPTIONS

Pin Name	Pin Number	Pin Type	Buffer Type	Description
	TQFP			
MCLR/VPP/RG5	7			Master Clear (input) or programming voltage (input).
MCLR		I	ST	Master Clear (Reset) input. This pin is an active-low Reset to the device.
VPP		P		Programming voltage input.
RG5		I	ST	Digital input.
OSC1/CLKI/RA7	39			Oscillator crystal or external clock input.
OSC1		I	ST	Oscillator crystal input or external clock source input. ST buffer when configured in RC mode; CMOS otherwise.
CLKI		I	CMOS	External clock source input. Always associated with pin function OSC1. (See related OSC1/CLKI, OSC2/CLKO pins.)
RA7		I/O	TTL	General purpose I/O pin.
OSC2/CLKO/RA6	40			Oscillator crystal or clock output.
OSC2		O	—	Oscillator crystal output. Connects to crystal or resonator in Crystal Oscillator mode.
CLKO		O	—	In RC mode, OSC2 pin outputs CLKO, which has 1/4 the frequency of OSC1 and denotes the instruction cycle rate.
RA6		I/O	TTL	General purpose I/O pin.

Legend: TTL = TTL compatible input   CMOS = CMOS compatible input or output
            ST   = Schmitt Trigger input with CMOS levels   Analog = Analog input
            I   = Input   O   = Output
            P   = Power   OD   = Open-Drain (no P diode to VDD)

Note 1: Default assignment for CCP2 when Configuration bit, CCP2MX, is set.
2: Alternate assignment for CCP2 when Configuration bit, CCP2MX, is cleared.

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TABLE 1-2: PIC18F6X93 PINOUT I/O DESCRIPTIONS (CONTINUED)

Pin Name	Pin Number TQFP	Pin Type	Buffer Type	Description
				PORTA is a bidirectional I/O port.
RA0/AN0	24			
RA0		I/O	TTL	Digital I/O.
AN0		I	Analog	Analog input 0.
RA1/AN1	23			
RA1		I/O	TTL	Digital I/O.
AN1		I	Analog	Analog input 1.
RA2/AN2/V$_{REF}$-/SEG16	22			
RA2		I/O	TTL	Digital I/O.
AN2		I	Analog	Analog input 2.
V$_{REF}$-		I	Analog	A/D reference voltage (Low) input.
SEG16		O	Analog	SEG16 output for LCD.
RA3/AN3/V$_{REF}$+/SEG17	21			
RA3		I/O	TTL	Digital I/O.
AN3		I	Analog	Analog input 3.
V$_{REF}$+		I	Analog	A/D reference voltage (High) input.
SEG17		O	Analog	SEG17 output for LCD.
RA4/T0CKI/SEG14	28			
RA4		I/O	ST/OD	Digital I/O. Open-drain when configured as output.
T0CKI		I	ST	Timer0 external clock input.
SEG14		O	Analog	SEG14 output for LCD.
RA5/AN4/HLVDIN/SEG15	27			
RA5		I/O	TTL	Digital I/O.
AN4		I	Analog	Analog input 4.
HLVDIN		I	Analog	Low-Voltage Detect input.
SEG15		O	Analog	SEG15 output for LCD.
RA6				See the OSC2/CLKO/RA6 pin.
RA7				See the OSC1/CLKI/RA7 pin.

Legend: TTL = TTL compatible input   CMOS = CMOS compatible input or output
ST = Schmitt Trigger input with CMOS levels   Analog = Analog input
I = Input   O = Output
P = Power   OD = Open-Drain (no P diode to V$_{DD}$)

Note 1: Default assignment for CCP2 when Configuration bit, CCP2MX, is set.

    2: Alternate assignment for CCP2 when Configuration bit, CCP2MX, is cleared.

TABLE 1-2: PIC18F6X93 PINOUT I/O DESCRIPTIONS (CONTINUED)

Pin Name	Pin Number TQFP	Pin Type	Buffer Type	Description
				PORTB is a bidirectional I/O port. PORTB can be software programmed for internal weak pull-ups on all inputs.
RB0/INT0	48			
RB0		I/O	TTL	Digital I/O.
INT0		I	ST	External interrupt 0.
RB1/INT1/SEG8	47			
RB1		I/O	TTL	Digital I/O.
INT1		I	ST	External interrupt 1.
SEG8		O	Analog	SEG8 output for LCD.
RB2/INT2/SEG9	46			
RB2		I/O	TTL	Digital I/O.
INT2		I	ST	External interrupt 2.
SEG9		O	Analog	SEG9 output for LCD.
RB3/INT3/SEG10	45			
RB3		I/O	TTL	Digital I/O.
INT3		I	ST	External interrupt 3.
SEG10		O	Analog	SEG10 output for LCD.
RB4/KBI0/SEG11	44			
RB4		I/O	TTL	Digital I/O.
KBI0		I	TTL	Interrupt-on-change pin.
SEG11		O	Analog	SEG11 output for LCD.
RB5/KBI1	43			
RB5		I/O	TTL	Digital I/O.
KBI1		I	TTL	Interrupt-on-change pin.
RB6/KBI2/PGC	42			
RB6		I/O	TTL	Digital I/O.
KBI2		I	TTL	Interrupt-on-change pin.
PGC		I/O	ST	In-Circuit Debugger and ICSP™ programming clock pin.
RB7/KBI3/PGD	37			
RB7		I/O	TTL	Digital I/O.
KBI3		I	TTL	Interrupt-on-change pin.
PGD		I/O	ST	In-Circuit Debugger and ICSP programming data pin.

Legend: TTL = TTL compatible input CMOS = CMOS compatible input or output
ST = Schmitt Trigger input with CMOS levels Analog = Analog input
I = Input O = Output
P = Power OD = Open-Drain (no P diode to V$_{DD}$)

Note 1: Default assignment for CCP2 when Configuration bit, CCP2MX, is set.

2: Alternate assignment for CCP2 when Configuration bit, CCP2MX, is cleared.

PIC18F6393/6493/8393/8493

TABLE 1-2: **PIC18F6X93 PINOUT I/O DESCRIPTIONS (CONTINUED)**

Pin Name	Pin Number TQFP	Pin Type	Buffer Type	Description
				PORTC is a bidirectional I/O port.
RC0/T1OSO/T13CKI	30			
RC0		I/O	ST	Digital I/O.
T1OSO		O	—	Timer1 oscillator output.
T13CKI		I	ST	Timer1/Timer3 external clock input.
RC1/T1OSI/CCP2	29			
RC1		I/O	ST	Digital I/O.
T1OSI		I	CMOS	Timer1 oscillator input.
CCP2[1]		I/O	ST	Capture 2 input/Compare 2 output/PWM2 output.
RC2/CCP1/SEG13	33			
RC2		I/O	ST	Digital I/O.
CCP1		I/O	ST	Capture 1 input/Compare 1 output/PWM1 output.
SEG13		O	Analog	SEG13 output for LCD.
RC3/SCK/SCL	34			
RC3		I/O	ST	Digital I/O.
SCK		I/O	ST	Synchronous serial clock input/output for SPI mode.
SCL		I/O	ST	Synchronous serial clock input/output for I^{2}C™ mode.
RC4/SDI/SDA	35			
RC4		I/O	ST	Digital I/O.
SDI		I	ST	SPI data in.
SDA		I/O	ST	I^{2}C data I/O.
RC5/SDO/SEG12	36			
RC5		I/O	ST	Digital I/O.
SDO		O	—	SPI data out.
SEG12		O	Analog	SEG12 output for LCD.
RC6/TX1/CK1	31			
RC6		I/O	ST	Digital I/O.
TX1		O	—	EUSART1 asynchronous transmit.
CK1		I/O	ST	EUSART1 synchronous clock (see related RX1/DT1).
RC7/RX1/DT1	32			
RC7		I/O	ST	Digital I/O.
RX1		I	ST	EUSART1 asynchronous receive.
DT1		I/O	ST	EUSART1 synchronous data (see related TX1/CK1).

Legend: TTL = TTL compatible input   CMOS = CMOS compatible input or output
         ST = Schmitt Trigger input with CMOS levels   Analog = Analog input
         I = Input   O = Output
         P = Power   OD = Open-Drain (no P diode to V$_{DD}$)

Note 1: Default assignment for CCP2 when Configuration bit, CCP2MX, is set.

     2: Alternate assignment for CCP2 when Configuration bit, CCP2MX, is cleared.

TABLE 1-2: **PIC18F6X93 PINOUT I/O DESCRIPTIONS (CONTINUED)**

Pin Name	Pin Number TQFP	Pin Type	Buffer Type	Description
RD0/SEG0 RD0 SEG0	58	 I/O O	 ST Analog	PORTD is a bidirectional I/O port. Digital I/O. SEG0 output for LCD.
RD1/SEG1 RD1 SEG1	55	 I/O O	 ST Analog	 Digital I/O. SEG1 output for LCD.
RD2/SEG2 RD2 SEG2	54	 I/O O	 ST Analog	 Digital I/O. SEG2 output for LCD.
RD3/SEG3 RD3 SEG3	53	 I/O O	 ST Analog	 Digital I/O. SEG3 output for LCD.
RD4/SEG4 RD4 SEG4	52	 I/O O	 ST Analog	 Digital I/O. SEG4 output for LCD.
RD5/SEG5 RD5 SEG5	51	 I/O O	 ST Analog	 Digital I/O. SEG5 output for LCD.
RD6/SEG6 RD6 SEG6	50	 I/O O	 ST Analog	 Digital I/O. SEG6 output for LCD.
RD7/SEG7 RD7 SEG7	49	 I/O O	 ST Analog	 Digital I/O. SEG7 output for LCD.

Legend: TTL = TTL compatible input   CMOS = CMOS compatible input or output
         ST = Schmitt Trigger input with CMOS levels   Analog = Analog input
         I = Input   O = Output
         P = Power   OD = Open-Drain (no P diode to V_{DD})

Note 1: Default assignment for CCP2 when Configuration bit, CCP2MX, is set.
     2: Alternate assignment for CCP2 when Configuration bit, CCP2MX, is cleared.

TABLE 1-2: **PIC18F6X93 PINOUT I/O DESCRIPTIONS (CONTINUED)**

Pin Name	Pin Number TQFP	Pin Type	Buffer Type	Description
				PORTE is a bidirectional I/O port.
LCDBIAS1	2			
LCDBIAS1		I	Analog	BIAS1 input for LCD.
LCDBIAS2	1			
LCDBIAS2		I	Analog	BIAS2 input for LCD.
LCDBIAS3	64			
LCDBIAS3		I	Analog	BIAS3 input for LCD.
COM0	63			
COM0		O	Analog	COM0 output for LCD.
RE4/COM1	62			
RE4		I/O	ST	Digital I/O.
COM1		O	Analog	COM1 output for LCD.
RE5/COM2	61			
RE5		I/O	ST	Digital I/O.
COM2		O	Analog	COM2 output for LCD.
RE6/COM3	60			
RE6		I/O	ST	Digital I/O.
COM3		O	Analog	COM3 output for LCD.
RE7/CCP2/SEG31	59			
RE7		I/O	ST	Digital I/O.
CCP2[2]		I/O	ST	Capture 2 input/Compare 2 output/PWM2 output.
SEG31		O	Analog	SEG31 output for LCD.

Legend: TTL = TTL compatible input CMOS = CMOS compatible input or output
ST = Schmitt Trigger input with CMOS levels Analog = Analog input
I = Input O = Output
P = Power OD = Open-Drain (no P diode to V_{DD})

Note 1: Default assignment for CCP2 when Configuration bit, CCP2MX, is set.

   2: Alternate assignment for CCP2 when Configuration bit, CCP2MX, is cleared.

TABLE 1-2: **PIC18F6X93 PINOUT I/O DESCRIPTIONS (CONTINUED)**

Pin Name	Pin Number TQFP	Pin Type	Buffer Type	Description
				PORTF is a bidirectional I/O port.
RF0/AN5/SEG18	18			
RF0		I/O	ST	Digital I/O.
AN5		I	Analog	Analog input 5.
SEG18		O	Analog	SEG18 output for LCD.
RF1/AN6/C2OUT/SEG19	17			
RF1		I/O	ST	Digital I/O.
AN6		I	Analog	Analog input 6.
C2OUT		O	—	Comparator 2 output.
SEG19		O	Analog	SEG19 output for LCD.
RF2/AN7/C1OUT/SEG20	16			
RF2		I/O	ST	Digital I/O.
AN7		I	Analog	Analog input 7.
C1OUT		O	—	Comparator 1 output.
SEG20		O	Analog	SEG20 output for LCD.
RF3/AN8/SEG21	15			
RF3		I/O	ST	Digital I/O.
AN8		I	Analog	Analog input 8.
SEG21		O	Analog	SEG21 output for LCD.
RF4/AN9/SEG22	14			
RF4		I/O	ST	Digital I/O.
AN9		I	Analog	Analog input 9.
SEG22		O	Analog	SEG22 output for LCD.
RF5/AN10/CV$_{REF}$/SEG23	13			
RF5		I/O	ST	Digital I/O.
AN10		I	Analog	Analog input 10.
CV$_{REF}$		O	Analog	Comparator reference voltage output.
SEG23		O	Analog	SEG23 output for LCD.
RF6/AN11/SEG24	12			
RF6		I/O	ST	Digital I/O.
AN11		I	Analog	Analog input 11.
SEG24		O	Analog	SEG24 output for LCD.
RF7/$\overline{SS}$/SEG25	11			
RF7		I/O	ST	Digital I/O.
$\overline{SS}$		I	TTL	SPI™ slave select input.
SEG25		O	Analog	SEG25 output for LCD.

Legend: TTL = TTL compatible input   CMOS = CMOS compatible input or output
ST = Schmitt Trigger input with CMOS levels   Analog = Analog input
I = Input   O = Output
P = Power   OD = Open-Drain (no P diode to V$_{DD}$)

Note 1: Default assignment for CCP2 when Configuration bit, CCP2MX, is set.
    2: Alternate assignment for CCP2 when Configuration bit, CCP2MX, is cleared.

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TABLE 1-2: **PIC18F6X93 PINOUT I/O DESCRIPTIONS (CONTINUED)**

Pin Name	Pin Number TQFP	Pin Type	Buffer Type	Description
RG0/SEG30	3			PORTG is a bidirectional I/O port.
RG0		I/O	ST	Digital I/O.
SEG30		O	Analog	SEG30 output for LCD.
RG1/TX2/CK2/SEG29	4			
RG1		I/O	ST	Digital I/O.
TX2		O	—	AUSART2 asynchronous transmit.
CK2		I/O	ST	AUSART2 synchronous clock (see related RX2/DT2).
SEG29		O	Analog	SEG29 output for LCD.
RG2/RX2/DT2/SEG28	5			
RG2		I/O	ST	Digital I/O.
RX2		I	ST	AUSART2 asynchronous receive.
DT2		I/O	ST	AUSART2 synchronous data (see related TX2/CK2).
SEG28		O	Analog	SEG28 output for LCD.
RG3/SEG27	6			
RG3		I/O	ST	Digital I/O.
SEG27		O	Analog	SEG27 output for LCD.
RG4/SEG26	8			
RG4		I/O	ST	Digital I/O.
SEG26		O	Analog	SEG26 output for LCD.
RG5				See $\overline{\text{MCLR}}$/Vpp/RG5 pin.
Vss	9, 25, 41, 56	P	—	Ground reference for logic and I/O pins.
VDD	10, 26, 38, 57	P	—	Positive supply for logic and I/O pins.
AVss	20	P	—	Ground reference for analog modules.
AVDD	19	P	—	Positive supply for analog modules.

Legend: TTL = TTL compatible input   CMOS = CMOS compatible input or output
ST = Schmitt Trigger input with CMOS levels   Analog = Analog input
I = Input   O = Output
P = Power   OD = Open-Drain (no P diode to VDD)

Note 1: Default assignment for CCP2 when Configuration bit, CCP2MX, is set.

    2: Alternate assignment for CCP2 when Configuration bit, CCP2MX, is cleared.

TABLE 1-3: **PIC18F8X93 PINOUT I/O DESCRIPTIONS**

Pin Name	Pin Number	Pin	Buffer	Description
	TQFP	Type	Type	
MCLR/VPP/RG5	9			Master Clear (input) or programming voltage (input).
MCLR		I	ST	Master Clear (Reset) input. This pin is an active-low Reset to the device.
VPP		P		Programming voltage input.
RG5		I	ST	Digital input.
OSC1/CLKI/RA7	49			Oscillator crystal or external clock input.
OSC1		I	ST	Oscillator crystal input or external clock source input. ST buffer when configured in RC mode; CMOS otherwise.
CLKI		I	CMOS	External clock source input. Always associated with pin function OSC1. (See related OSC1/CLKI, OSC2/CLKO pins.)
RA7		I/O	TTL	General purpose I/O pin.
OSC2/CLKO/RA6	50			Oscillator crystal or clock output.
OSC2		O	—	Oscillator crystal output. Connects to crystal or resonator in Crystal Oscillator mode.
CLKO		O	—	In RC mode, OSC2 pin outputs CLKO, which has 1/4 the frequency of OSC1 and denotes the instruction cycle rate.
RA6		I/O	TTL	General purpose I/O pin.

Legend: TTL = TTL compatible input   CMOS = CMOS compatible input or output
ST = Schmitt Trigger input with CMOS levels   Analog = Analog input
I = Input   O = Output
P = Power   OD = Open-Drain (no P diode to VDD)

Note 1: Default assignment for CCP2 when Configuration bit, CCP2MX, is set.

    2: Alternate assignment for CCP2 when Configuration bit, CCP2MX, is cleared.

TABLE 1-3: **PIC18F8X93 PINOUT I/O DESCRIPTIONS (CONTINUED)**

Pin Name	Pin Number TQFP	Pin Type	Buffer Type	Description
				PORTA is a bidirectional I/O port.
RA0/AN0	30			
RA0		I/O	TTL	Digital I/O.
AN0		I	Analog	Analog input 0.
RA1/AN1	29			
RA1		I/O	TTL	Digital I/O.
AN1		I	Analog	Analog input 1.
RA2/AN2/V_{REF}-/SEG16	28			
RA2		I/O	TTL	Digital I/O.
AN2		I	Analog	Analog input 2.
V_{REF}-		I	Analog	A/D reference voltage (Low) input.
SEG16		O	Analog	SEG16 output for LCD.
RA3/AN3/V_{REF}+/SEG17	27			
RA3		I/O	TTL	Digital I/O.
AN3		I	Analog	Analog input 3.
V_{REF}+		I	Analog	A/D reference voltage (High) input.
SEG17		O	Analog	SEG17 output for LCD.
RA4/T0CKI/SEG14	34			
RA4		I/O	ST/OD	Digital I/O. Open-drain when configured as output.
T0CKI		I	ST	Timer0 external clock input.
SEG14		O	Analog	SEG14 output for LCD.
RA5/AN4/HLVDIN/SEG15	33			
RA5		I/O	TTL	Digital I/O.
AN4		I	Analog	Analog input 4.
HLVDIN		I	Analog	Low-Voltage Detect input.
SEG15		O	Analog	SEG15 output for LCD.
RA6				See the OSC2/CLKO/RA6 pin.
RA7				See the OSC1/CLKI/RA7 pin.

Legend: TTL = TTL compatible input   CMOS = CMOS compatible input or output
ST = Schmitt Trigger input with CMOS levels   Analog = Analog input
I = Input   O = Output
P = Power   OD = Open-Drain (no P diode to V_{DD})

Note 1: Default assignment for CCP2 when Configuration bit, CCP2MX, is set.

    2: Alternate assignment for CCP2 when Configuration bit, CCP2MX, is cleared.

TABLE 1-3: PIC18F8X93 PINOUT I/O DESCRIPTIONS (CONTINUED)

Pin Name	Pin Number TQFP	Pin Type	Buffer Type	Description
				PORTB is a bidirectional I/O port. PORTB can be software programmed for internal weak pull-ups on all inputs.
RB0/INT0	58			
RB0		I/O	TTL	Digital I/O.
INT0		I	ST	External interrupt 0.
RB1/INT1/SEG8	57			
RB1		I/O	TTL	Digital I/O.
INT1		I	ST	External interrupt 1.
SEG8		O	Analog	SEG8 output for LCD.
RB2/INT2/SEG9	56			
RB2		I/O	TTL	Digital I/O.
INT2		I	ST	External interrupt 2.
SEG9		O	Analog	SEG9 output for LCD.
RB3/INT3/SEG10	55			
RB3		I/O	TTL	Digital I/O.
INT3		I	ST	External interrupt 3.
SEG10		O	Analog	SEG10 output for LCD.
RB4/KBI0/SEG11	54			
RB4		I/O	TTL	Digital I/O.
KBI0		I	TTL	Interrupt-on-change pin.
SEG11		O	Analog	SEG11 output for LCD.
RB5/KBI1	53			
RB5		I/O	TTL	Digital I/O.
KBI1		I	TTL	Interrupt-on-change pin.
RB6/KBI2/PGC	52			
RB6		I/O	TTL	Digital I/O.
KBI2		I	TTL	Interrupt-on-change pin.
PGC		I/O	ST	In-Circuit Debugger and ICSP™ programming clock pin.
RB7/KBI3/PGD	47			
RB7		I/O	TTL	Digital I/O.
KBI3		I	TTL	Interrupt-on-change pin.
PGD		I/O	ST	In-Circuit Debugger and ICSP programming data pin.

Legend: TTL = TTL compatible input CMOS = CMOS compatible input or output
ST = Schmitt Trigger input with CMOS levels Analog = Analog input
I = Input O = Output
P = Power OD = Open-Drain (no P diode to VDD)

Note 1: Default assignment for CCP2 when Configuration bit, CCP2MX, is set.
2: Alternate assignment for CCP2 when Configuration bit, CCP2MX, is cleared.

TABLE 1-3: PIC18F8X93 PINOUT I/O DESCRIPTIONS (CONTINUED)

Pin Name	Pin Number TQFP	Pin Type	Buffer Type	Description
				PORTC is a bidirectional I/O port.
RC0/T1OSO/T13CKI	36			
RC0		I/O	ST	Digital I/O.
T1OSO		O	—	Timer1 oscillator output.
T13CKI		I	ST	Timer1/Timer3 external clock input.
RC1/T1OSI/CCP2	35			
RC1		I/O	ST	Digital I/O.
T1OSI		I	CMOS	Timer1 oscillator input.
CCP2[1]		I/O	ST	Capture 2 input/Compare 2 output/PWM2 output.
RC2/CCP1/SEG13	43			
RC2		I/O	ST	Digital I/O.
CCP1		I/O	ST	Capture 1 input/Compare 1 output/PWM1 output.
SEG13		O	Analog	SEG13 output for LCD.
RC3/SCK/SCL	44			
RC3		I/O	ST	Digital I/O.
SCK		I/O	ST	Synchronous serial clock input/output for SPI mode.
SCL		I/O	ST	Synchronous serial clock input/output for I^{2}C™ mode.
RC4/SDI/SDA	45			
RC4		I/O	ST	Digital I/O.
SDI		I	ST	SPI data in.
SDA		I/O	ST	I^{2}C data I/O.
RC5/SDO/SEG12	46			
RC5		I/O	ST	Digital I/O.
SDO		O	—	SPI data out.
SEG12		O	Analog	SEG12 output for LCD.
RC6/TX1/CK1	37			
RC6		I/O	ST	Digital I/O.
TX1		O	—	EUSART1 asynchronous transmit.
CK1		I/O	ST	EUSART1 synchronous clock (see related RX1/DT1).
RC7/RX1/DT1	38			
RC7		I/O	ST	Digital I/O.
RX1		I	ST	EUSART1 asynchronous receive.
DT1		I/O	ST	EUSART1 synchronous data (see related TX1/CK1).

Legend: TTL = TTL compatible input   CMOS = CMOS compatible input or output
         ST = Schmitt Trigger input with CMOS levels   Analog = Analog input
         I = Input   O = Output
         P = Power   OD = Open-Drain (no P diode to V$_{DD}$)

Note 1: Default assignment for CCP2 when Configuration bit, CCP2MX, is set.

     2: Alternate assignment for CCP2 when Configuration bit, CCP2MX, is cleared.

TABLE 1-3: **PIC18F8X93 PINOUT I/O DESCRIPTIONS (CONTINUED)**

Pin Name	Pin Number TQFP	Pin Type	Buffer Type	Description
				PORTD is a bidirectional I/O port.
RD0/SEG0	72			
RD0		I/O	ST	Digital I/O.
SEG0		O	Analog	SEG0 output for LCD.
RD1/SEG1	69			
RD1		I/O	ST	Digital I/O.
SEG1		O	Analog	SEG1 output for LCD.
RD2/SEG2	68			
RD2		I/O	ST	Digital I/O.
SEG2		O	Analog	SEG2 output for LCD.
RD3/SEG3	67			
RD3		I/O	ST	Digital I/O.
SEG3		O	Analog	SEG3 output for LCD.
RD4/SEG4	66			
RD4		I/O	ST	Digital I/O.
SEG4		O	Analog	SEG4 output for LCD.
RD5/SEG5	65			
RD5		I/O	ST	Digital I/O.
SEG5		O	Analog	SEG5 output for LCD.
RD6/SEG6	64			
RD6		I/O	ST	Digital I/O.
SEG6		O	Analog	SEG6 output for LCD.
RD7/SEG7	63			
RD7		I/O	ST	Digital I/O.
SEG7		O	Analog	SEG7 output for LCD.

Legend: TTL = TTL compatible input   CMOS = CMOS compatible input or output
ST = Schmitt Trigger input with CMOS levels   Analog = Analog input
I = Input   O = Output
P = Power   OD = Open-Drain (no P diode to V$_{DD}$)

Note 1: Default assignment for CCP2 when Configuration bit, CCP2MX, is set.
2: Alternate assignment for CCP2 when Configuration bit, CCP2MX, is cleared.

TABLE 1-3: **PIC18F8X93 PINOUT I/O DESCRIPTIONS (CONTINUED)**

Pin Name	Pin Number TQFP	Pin Type	Buffer Type	Description
				PORTE is a bidirectional I/O port.
LCDBIAS1	4			
LCDBIAS1		I	Analog	BIAS1 input for LCD.
LCDBIAS2	3			
LCDBIAS2		I	Analog	BIAS2 input for LCD.
LCDBIAS3	78			
LCDBIAS3		I	Analog	BIAS3 input for LCD.
COM0	77			
COM0		O	Analog	COM0 output for LCD.
RE4/COM1	76			
RE4		I/O	ST	Digital I/O.
COM1		O	Analog	COM1 output for LCD.
RE5/COM2	75			
RE5		I/O	ST	Digital I/O.
COM2		O	Analog	COM2 output for LCD.
RE6/COM3	74			
RE6		I/O	ST	Digital I/O.
COM3		O	Analog	COM3 output for LCD.
RE7/CCP2/SEG31	73			
RE7		I/O	ST	Digital I/O.
CCP2[2]		I/O	ST	Capture 2 input/Compare 2 output/PWM2 output.
SEG31		O	Analog	SEG31 output for LCD.

Legend: TTL = TTL compatible input CMOS = CMOS compatible input or output
ST = Schmitt Trigger input with CMOS levels Analog = Analog input
I = Input O = Output
P = Power OD = Open-Drain (no P diode to V_{DD})

Note 1: Default assignment for CCP2 when Configuration bit, CCP2MX, is set.

2: Alternate assignment for CCP2 when Configuration bit, CCP2MX, is cleared.

TABLE 1-3: **PIC18F8X93 PINOUT I/O DESCRIPTIONS (CONTINUED)**

Pin Name	Pin Number TQFP	Pin Type	Buffer Type	Description
				PORTF is a bidirectional I/O port.
RF0/AN5/SEG18	24			
RF0		I/O	ST	Digital I/O.
AN5		I	Analog	Analog input 5.
SEG18		O	Analog	SEG18 output for LCD.
RF1/AN6/C2OUT/SEG19	23			
RF1		I/O	ST	Digital I/O.
AN6		I	Analog	Analog input 6.
C2OUT		O	—	Comparator 2 output.
SEG19		O	Analog	SEG19 output for LCD.
RF2/AN7/C1OUT/SEG20	18			
RF2		I/O	ST	Digital I/O.
AN7		I	Analog	Analog input 7.
C1OUT		O	—	Comparator 1 output.
SEG20		O	Analog	SEG20 output for LCD.
RF3/AN8/SEG21	17			
RF3		I/O	ST	Digital I/O.
AN8		I	Analog	Analog input 8.
SEG21		O	Analog	SEG21 output for LCD.
RF4/AN9/SEG22	16			
RF4		I/O	ST	Digital I/O.
AN9		I	Analog	Analog input 9.
SEG22		O	Analog	SEG22 output for LCD.
RF5/AN10/CV$_{REF}$/SEG23	15			
RF5		I/O	ST	Digital I/O.
AN10		I	Analog	Analog input 10.
CV$_{REF}$		O	Analog	Comparator reference voltage output.
SEG23		O	Analog	SEG23 output for LCD.
RF6/AN11/SEG24	14			
RF6		I/O	ST	Digital I/O.
AN11		I	Analog	Analog input 11.
SEG24		O	Analog	SEG24 output for LCD.
RF7/$\overline{SS}$/SEG25	13			
RF7		I/O	ST	Digital I/O.
$\overline{SS}$		I	TTL	SPI slave select input.
SEG25		O	Analog	SEG25 output for LCD.

Legend: TTL = TTL compatible input   CMOS = CMOS compatible input or output
         ST = Schmitt Trigger input with CMOS levels   Analog = Analog input
         I = Input   O = Output
         P = Power   OD = Open-Drain (no P diode to V$_{DD}$)

Note 1: Default assignment for CCP2 when Configuration bit, CCP2MX, is set.

      2: Alternate assignment for CCP2 when Configuration bit, CCP2MX, is cleared.

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TABLE 1-3: PIC18F8X93 PINOUT I/O DESCRIPTIONS (CONTINUED)

Pin Name	Pin Number TQFP	Pin Type	Buffer Type	Description
				PORTG is a bidirectional I/O port.
RG0/SEG30	5			
RG0		I/O	ST	Digital I/O.
SEG30		O	Analog	SEG30 output for LCD.
RG1/TX2/CK2/SEG29	6			
RG1		I/O	ST	Digital I/O.
TX2		O	—	AUSART2 asynchronous transmit.
CK2		I/O	ST	AUSART2 synchronous clock (see related RX2/DT2).
SEG29		O	Analog	SEG29 output for LCD.
RG2/RX2/DT2/SEG28	7			
RG2		I/O	ST	Digital I/O.
RX2		I	ST	AUSART2 asynchronous receive.
DT2		I/O	ST	AUSART2 synchronous data (see related TX2/CK2).
SEG28		O	Analog	SEG28 output for LCD.
RG3/SEG27	8			
RG3		I/O	ST	Digital I/O.
SEG27		O	Analog	SEG27 output for LCD.
RG4/SEG26	10			
RG4		I/O	ST	Digital I/O.
SEG26		O	Analog	SEG26 output for LCD.
RG5				See $\overline{\text{MCLR}}$/VPP/RG5 pin.

Legend: TTL = TTL compatible input   CMOS = CMOS compatible input or output
ST = Schmitt Trigger input with CMOS levels   Analog = Analog input
I = Input   O = Output
P = Power   OD = Open-Drain (no P diode to VDD)

Note 1: Default assignment for CCP2 when Configuration bit, CCP2MX, is set.

2: Alternate assignment for CCP2 when Configuration bit, CCP2MX, is cleared.

TABLE 1-3: **PIC18F8X93 PINOUT I/O DESCRIPTIONS (CONTINUED)**

Pin Name	Pin Number TQFP	Pin Type	Buffer Type	Description
				PORTH is a bidirectional I/O port.
RH0/SEG47	79			
RH0		I/O	ST	Digital I/O.
SEG47		O	Analog	SEG47 output for LCD.
RH1/SEG46	80			
RH1		I/O	ST	Digital I/O.
SEG46		O	Analog	SEG46 output for LCD.
RH2/SEG45	1			
RH2		I/O	ST	Digital I/O.
SEG45		O	Analog	SEG45 output for LCD.
RH3/SEG44	2			
RH3		I/O	ST	Digital I/O.
SEG44		O	Analog	SEG44 output for LCD.
RH4/SEG40	22			
RH4		I/O	ST	Digital I/O.
SEG40		O	Analog	SEG40 output for LCD.
RH5/SEG41	21			
RH5		I/O	ST	Digital I/O.
SEG41		O	Analog	SEG41 output for LCD.
RH6/SEG42	20			
RH6		I/O	ST	Digital I/O.
SEG42		O	Analog	SEG42 output for LCD.
RH7/SEG43	19			
RH7		I/O	ST	Digital I/O.
SEG43		O	Analog	SEG43 output for LCD.

Legend: TTL = TTL compatible input   CMOS = CMOS compatible input or output
ST = Schmitt Trigger input with CMOS levels   Analog = Analog input
I = Input   O = Output
P = Power   OD = Open-Drain (no P diode to V_{DD})

Note 1: Default assignment for CCP2 when Configuration bit, CCP2MX, is set.
    2: Alternate assignment for CCP2 when Configuration bit, CCP2MX, is cleared.

TABLE 1-3:   PIC18F8X93 PINOUT I/O DESCRIPTIONS (CONTINUED)

Pin Name	Pin Number TQFP	Pin Type	Buffer Type	Description
				PORTJ is a bidirectional I/O port.
RJ0/SEG32	62			
RJ0		I/O	ST	Digital I/O.
SEG32		O	Analog	SEG32 output for LCD.
RJ1/SEG33	61			
RJ1		I/O	ST	Digital I/O.
SEG33		O	Analog	SEG33 output for LCD.
RJ2/SEG34	60			
RJ2		I/O	ST	Digital I/O.
SEG34		O	Analog	SEG34 output for LCD.
RJ3/SEG35	59			
RJ3		I/O	ST	Digital I/O.
SEG35		O	Analog	SEG35 output for LCD.
RJ4/SEG39	39			
RJ4		I/O	ST	Digital I/O.
SEG39		O	Analog	SEG39 output for LCD.
RJ5/SEG38	40			
RJ5		I/O	ST	Digital I/O
SEG38		O	Analog	SEG38 output for LCD.
RJ6/SEG37	41			
RJ6		I/O	ST	Digital I/O.
SEG37		O	Analog	SEG37 output for LCD.
RJ7/SEG36	42			
RJ7		I/O	ST	Digital I/O.
SEG36		O	Analog	SEG36 output for LCD.
Vss	11, 31, 51, 70	P	—	Ground reference for logic and I/O pins.
Vdd	12, 32, 48, 71	P	—	Positive supply for logic and I/O pins.
AVss	26	P	—	Ground reference for analog modules.
AVdd	25	P	—	Positive supply for analog modules.

Legend: TTL = TTL compatible input   CMOS = CMOS compatible input or output
ST = Schmitt Trigger input with CMOS levels   Analog = Analog input
I = Input   O = Output
P = Power   OD = Open-Drain (no P diode to VDD)

Note 1: Default assignment for CCP2 when Configuration bit, CCP2MX, is set.
      2: Alternate assignment for CCP2 when Configuration bit, CCP2MX, is cleared.

2.0 12-BIT ANALOG-TO-DIGITAL CONVERTER (A/D) MODULE

The Analog-to-Digital (A/D) Converter module converts an analog input signal to a 12-bit digital number. The module has 12 inputs for both PIC18F6393/6493 (64-pin) and PIC18F8393/8493 (80-pin) devices.

The module has five registers:

- A/D Result High Register (ADRESH)
- A/D Result Low Register (ADRESL)
- A/D Control Register 0 (ADCON0)
- A/D Control Register 1 (ADCON1)
- A/D Control Register 2 (ADCON2)

The ADCON0 register, shown in Register 2-1, controls the operation of the A/D module. The ADCON1 register, shown in Register 2-2, configures the functions of the port pins. The ADCON2 register, shown in Register 2-3, configures the A/D clock source, programmed acquisition time and justification.

REGISTER 2-1: ADCON0: A/D CONTROL REGISTER 0

U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
—	—	CHS3	CHS2	CHS1	CHS0	GO/DONE	ADON
bit 7							bit 0

Legend:		
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 7-6 **Unimplemented:** Read as '0'

bit 5-2 **CHS3:CHS0:** Analog Channel Select bits
0000 = Channel 0 (AN0)
0001 = Channel 1 (AN1)
0010 = Channel 2 (AN2)
0011 = Channel 3 (AN3)
0100 = Channel 4 (AN4)
0101 = Channel 5 (AN5)
0110 = Channel 6 (AN6)
0111 = Channel 7 (AN7)
1000 = Channel 8 (AN8)
1001 = Channel 9 (AN9)
1010 = Channel 10 (AN10)
1011 = Channel 11 (AN11)
1100 = Unimplemented[1]
1101 = Unimplemented[1]
1110 = Unimplemented[1]
1111 = Unimplemented[1]

bit 1 **GO/DONE:** A/D Conversion Status bit
When ADON = 1:
1 = A/D conversion in progress
0 = A/D Idle

bit 0 **ADON:** A/D On bit
1 = A/D Converter module is enabled
0 = A/D Converter module is disabled

Note 1: Performing a conversion on unimplemented channels will return a floating input measurement.

REGISTER 2-2: ADCON1: A/D CONTROL REGISTER 1

U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0

REGISTER 2-2: **ADCON1: A/D CONTROL REGISTER 1 (CONTINUED)**

—	—	VCFG1	VCFG0	PCFG3	PCFG2	PCFG1	PCFG0
bit 7							bit 0

Legend:		
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 7-6   **Unimplemented:** Read as '0'

bit 5-4   **VCFG1:VCFG0:** Voltage Reference Configuration bits

	A/D VREF+	A/D VREF-
00	AVDD	AVSS
01	External VREF+	AVSS
10	AVDD	External VREF-
11	External VREF+	External VREF-

bit 3-0   **PCFG3:PCFG0:** A/D Port Configuration Control bits

PCFG<3:0>	AN11	AN10	AN9	AN8	AN7	AN6	AN5	AN4	AN3	AN2	AN1	AN0
0000	A	A	A	A	A	A	A	A	A	A	A	A
0001	A	A	A	A	A	A	A	A	A	A	A	A
0010	A	A	A	A	A	A	A	A	A	A	A	A
0011	A	A	A	A	A	A	A	A	A	A	A	A
0100	D	A	A	A	A	A	A	A	A	A	A	A
0101	D	D	A	A	A	A	A	A	A	A	A	A
0110	D	D	D	A	A	A	A	A	A	A	A	A
0111	D	D	D	D	A	A	A	A	A	A	A	A
1000	D	D	D	D	D	A	A	A	A	A	A	A
1001	D	D	D	D	D	D	A	A	A	A	A	A
1010	D	D	D	D	D	D	D	A	A	A	A	A
1011	D	D	D	D	D	D	D	D	A	A	A	A
1100	D	D	D	D	D	D	D	D	D	A	A	A
1101	D	D	D	D	D	D	D	D	D	D	A	A
1110	D	D	D	D	D	D	D	D	D	D	D	A
1111	D	D	D	D	D	D	D	D	D	D	D	D

A = Analog input   D = Digital I/O

REGISTER 2-3: **ADCON2: A/D CONTROL REGISTER 2**

R/W-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
ADFM	—	ACQT2	ACQT1	ACQT0	ADCS2	ADCS1	ADCS0
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 7   **ADFM:** A/D Result Format Select bit

          1 = Right justified
          0 = Left justified

bit 6   **Unimplemented:** Read as '0'

bit 5-3   **ACQT2:ACQT0:** A/D Acquisition Time Select bits

          111 = 20 T_{AD}
          110 = 16 T_{AD}
          101 = 12 T_{AD}
          100 = 8 T_{AD}
          011 = 6 T_{AD}
          010 = 4 T_{AD}
          001 = 2 T_{AD}
          000 = 0 T_{AD}[1]

bit 2-0   **ADCS2:ADCS0:** A/D Conversion Clock Select bits

          111 = F$_{RC}$ (clock derived from A/D RC oscillator)[1]
          110 = F$_{OSC}$/64
          101 = F$_{OSC}$/16
          100 = F$_{OSC}$/4
          011 = F$_{RC}$ (clock derived from A/D RC oscillator)[1]
          010 = F$_{OSC}$/32
          001 = F$_{OSC}$/8
          000 = F$_{OSC}$/2

Note 1: If the A/D F$_{RC}$ clock source is selected, a delay of one T$_{CY}$ (instruction cycle) is added before the A/D clock starts. This allows the SLEEP instruction to be executed before starting a conversion.

The analog reference voltage is software selectable to either the device's positive and negative supply voltage (V_{DD} and V_{SS}), or the voltage level on the RA3/AN3/V_{REF}+/SEG17 and RA2/AN2/V_{REF}-/SEG16 pins.

The A/D Converter has a unique feature of being able to operate while the device is in Sleep mode. To operate in Sleep, the A/D conversion clock must be derived from the A/D's internal RC oscillator.

The output of the sample and hold is the input into the converter, which generates the result via successive approximation.

A device Reset forces all registers to their Reset state. This forces the A/D module to be turned off and any conversion in progress is aborted.

Each port pin associated with the A/D Converter can be configured as an analog input or a digital I/O. The ADRESH and ADRESL registers contain the result of the A/D conversion. When the A/D conversion is complete, the result is loaded into the ADRESH:ADRESL register pair, the GO/DONE bit (ADCON0<1>) is cleared and the A/D Interrupt Flag bit, ADIF, is set. The block diagram of the A/D module is shown in Figure 2-1.

FIGURE 2-1: **A/D BLOCK DIAGRAM**

Note 1: I/O pins have diode protection to V_{DD} and V_{SS}.
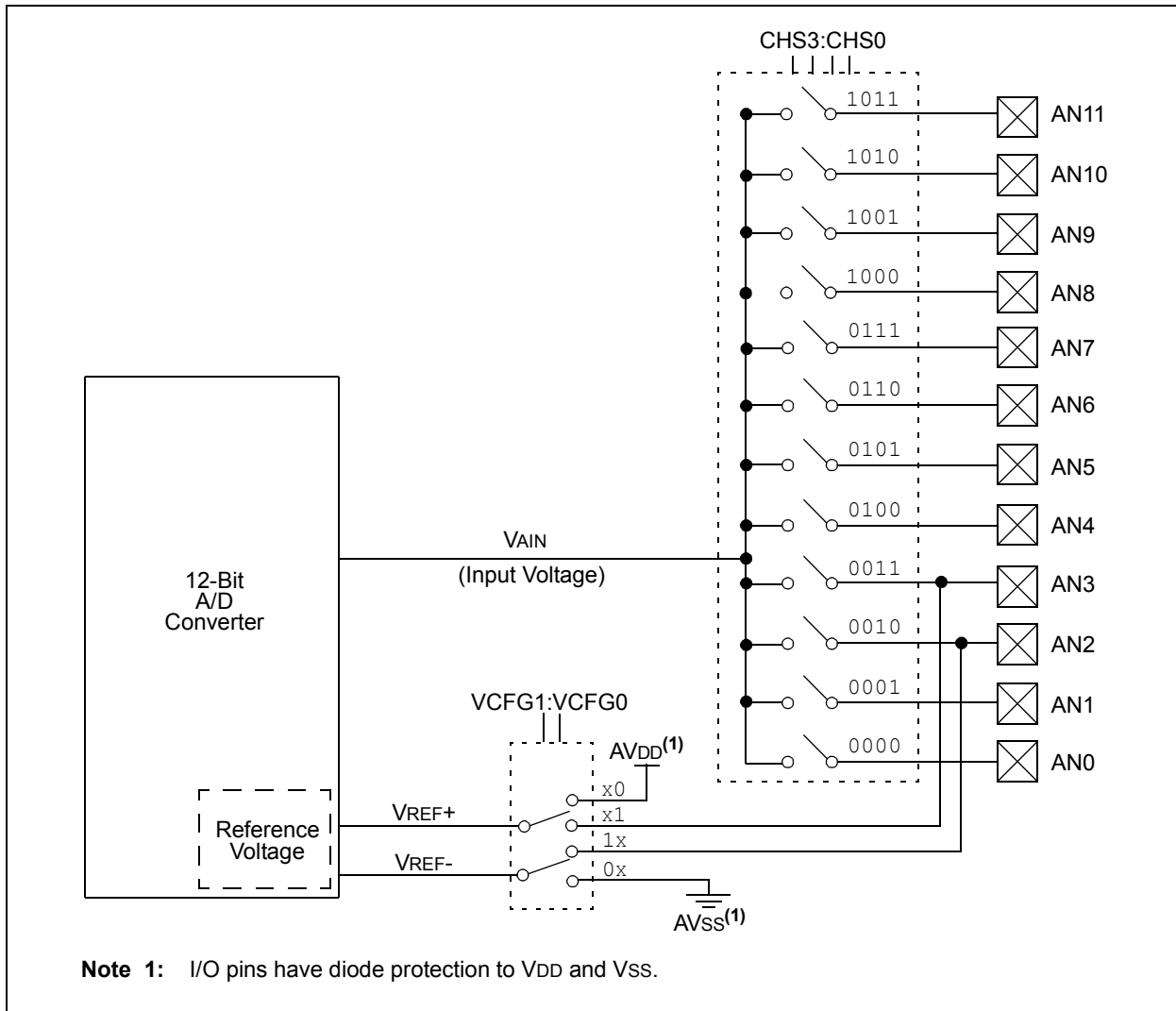
The value in the ADRESH:ADRESL registers is unknown following Power-on and Brown-out Resets and is not affected by any other Reset.

After the A/D module has been configured as desired, the selected channel must be acquired before the conversion is started. The analog input channels must have their corresponding TRIS bits selected as an input. To determine acquisition time, see **Section 2.1 "A/D Acquisition Requirements"**. After this acquisition time has elapsed, the A/D conversion can be started. An acquisition time can be programmed to occur between setting the GO/DONE bit and the actual start of the conversion.

The following steps should be followed to perform an A/D conversion:

1. Configure the A/D module:
   - Configure analog pins, voltage reference and digital I/O (ADCON1)
   - Select A/D input channel (ADCON0)
   - Select A/D acquisition time (ADCON2)
   - Select A/D conversion clock (ADCON2)
   - Turn on A/D module (ADCON0)
2. Configure A/D interrupt (if desired):
   - Clear ADIF bit
   - Set ADIE bit
   - Set GIE bit
3. Wait the required acquisition time (if required).
4. Start conversion:
   - Set GO/DONE bit (ADCON0<1>)

5. Wait for A/D conversion to complete by either:
   - Polling for the GO/DONE bit to be cleared

   OR

   - Waiting for the A/D interrupt
6. Read A/D Result registers (ADRESH:ADRESL); clear bit, ADIF, if required.
7. For the next conversion, go to step 1 or step 2, as required. The A/D conversion time per bit is defined as T$_{AD}$. A minimum wait of 2 T$_{AD}$ is required before the next acquisition starts.

FIGURE 2-2:   **A/D TRANSFER FUNCTION**
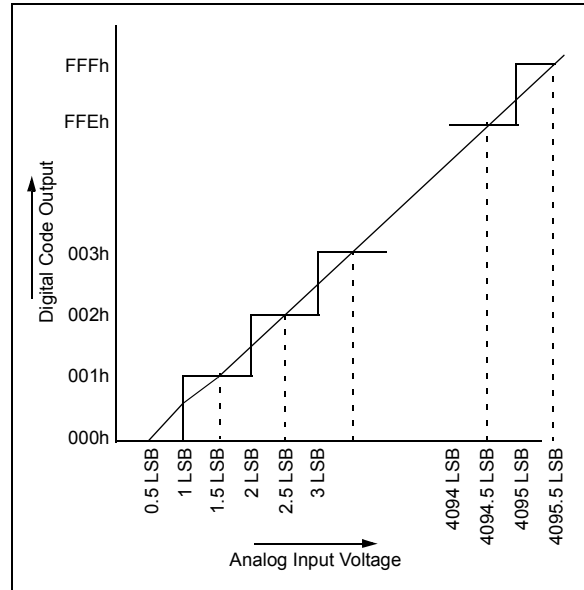
FIGURE 2-3:   **ANALOG INPUT MODEL**
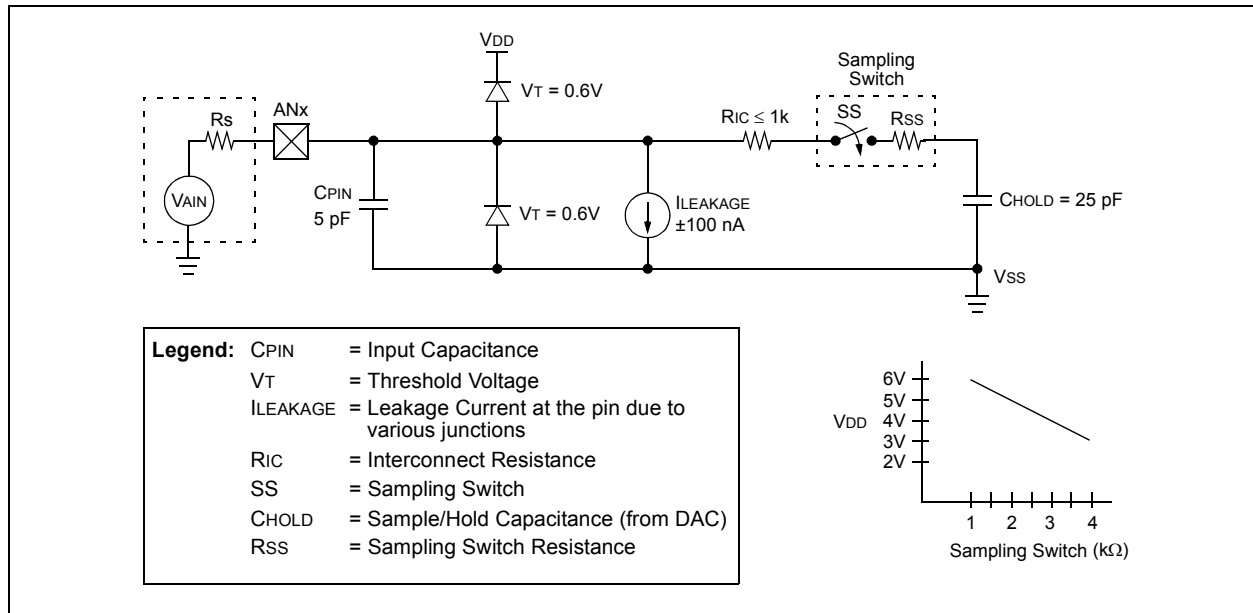
2.1 A/D Acquisition Requirements

For the A/D Converter to meet its specified accuracy, the charge holding capacitor (CHOLD) must be allowed to fully charge to the input channel voltage level. The analog input model is shown in Figure 2-3. The source impedance (RS) and the internal sampling switch (RSS) impedance directly affect the time required to charge the capacitor, CHOLD. The sampling switch (RSS) impedance varies over the device voltage (VDD). The source impedance affects the offset voltage at the analog input (due to pin leakage current). **The maximum recommended impedance for analog sources is 2.5 kΩ**. After the analog input channel is selected (changed), the channel must be sampled for at least the minimum acquisition time before starting a conversion.

Note:	When the conversion is started, the holding capacitor is disconnected from the input pin.

To calculate the minimum acquisition time, Equation 2-1 may be used. This equation assumes that 1/2 LSb error is used (4096 steps for the 12-bit A/D). The 1/2 LSb error is the maximum error allowed for the A/D to meet its specified resolution.

Equation 2-3 shows the calculation of the minimum required acquisition time, TACQ. This calculation is based on the following application system assumptions:

CHOLD	=	25 pF
Rs	=	2.5 kΩ
Conversion Error	$\leq$	1/2 LSb
VDD	=	3V $\rightarrow$ Rss = 4 kΩ
Temperature	=	85°C (system max.)

EQUATION 2-1: ACQUISITION TIME

$$\text{TACQ} = \text{Amplifier Settling Time + Holding Capacitor Charging Time + Temperature Coefficient}$$
$$= \text{TAMP + TC + TCOFF}$$

EQUATION 2-2: A/D MINIMUM CHARGING TIME

$$\text{VHOLD} = (\text{VREF} - (\text{VREF}/4096)) \bullet (1 - e^{(-\text{TC}/\text{CHOLD}(\text{RIC} + \text{RSS} + \text{RS}))})$$
or
$$\text{TC} = -(\text{CHOLD})(\text{RIC} + \text{RSS} + \text{RS}) \ln(1/4096)$$

EQUATION 2-3: CALCULATING THE MINIMUM REQUIRED ACQUISITION TIME

TACQ	=	TAMP + TC + TCOFF
TAMP	=	0.2 μs
TCOFF	=	(Temp – 25°C)(0.02 μs/°C)
		(85°C – 25°C)(0.02 μs/°C)
		1.2 μs

Temperature coefficient is only required for temperatures > 25°C. Below 25°C, TCOFF = 0 μs.

TC	=	-(CHOLD)(RIC + RSS + RS) ln(1/4096) μs
		-(25 pF) (1 kΩ + 4 kΩ + 2.5 kΩ) ln(0.0002441) μs
		1.56 μs
TACQ	=	0.2 μs + 1.56 μs + 1.2 μs
		2.96 μs

2.2 Selecting and Configuring Acquisition Time

The ADCON2 register allows the user to select an acquisition time that occurs each time the GO/$\overline{\text{DONE}}$ bit is set. It also gives users the option to use an automatically determined acquisition time.

Acquisition time may be set with the ACQT2:ACQT0 bits (ADCON2<5:3>), which provide a range of 2 to 20 T$_{AD}$. When the GO/$\overline{\text{DONE}}$ bit is set, the A/D module continues to sample the input for the selected acquisition time, then automatically begins a conversion. Since the acquisition time is programmed, there may be no need to wait for an acquisition time between selecting a channel and setting the GO/$\overline{\text{DONE}}$ bit.

Manual acquisition is selected when ACQT2:ACQT0 = `000`. When the GO/$\overline{\text{DONE}}$ bit is set, sampling is stopped and a conversion begins. The user is responsible for ensuring the required acquisition time has passed between selecting the desired input channel and setting the GO/$\overline{\text{DONE}}$ bit. This option is also the default Reset state of the ACQT2:ACQT0 bits and is compatible with devices that do not offer programmable acquisition times.

In either case, when the conversion is completed, the GO/$\overline{\text{DONE}}$ bit is cleared, the ADIF flag is set and the A/D begins sampling the currently selected channel again. If an acquisition time is programmed, there is nothing to indicate if the acquisition time has ended or if the conversion has begun.

2.3 Selecting the A/D Conversion Clock

The A/D conversion time per bit is defined as T$_{AD}$. The A/D conversion requires 13 T$_{AD}$ per 12-bit conversion. The source of the A/D conversion clock is software selectable. There are seven possible options for T$_{AD}$:

- 2 T$_{OSC}$
- 4 T$_{OSC}$
- 8 T$_{OSC}$
- 16 T$_{OSC}$
- 32 T$_{OSC}$
- 64 T$_{OSC}$
- Internal RC Oscillator

For correct A/D conversions, the A/D conversion clock (T$_{AD}$) must be as short as possible, but greater than the minimum T$_{AD}$. (See parameter 130 for more information.)

Table 2-1 shows the resultant T$_{AD}$ times derived from the device operating frequencies and the A/D clock source selected.

TABLE 2-1: T$_{AD}$ vs. DEVICE OPERATING FREQUENCIES

A/D Clock Source (T$_{AD}$)		Assumes T$_{AD}$ Min. = 0.8 μs
Operation	ADCS2:ADCS0	Maximum F$_{OSC}$
2 T$_{OSC}$	`000`	2.50 MHz
4 T$_{OSC}$	`100`	5.00 MHz
8 T$_{OSC}$	`001`	10.00 MHz
16 T$_{OSC}$	`101`	20.00 MHz
32 T$_{OSC}$	`010`	40.00 MHz
64 T$_{OSC}$	`110`	40.00 MHz
RC[1]	`x11`	1.00 MHz[2]

Note 1: The RC source has a typical T$_{AD}$ time of 2.5 μs.

2: For device frequencies above 1 MHz, the device must be in Sleep for the entire conversion or a F$_{OSC}$ divider should be used instead; otherwise, the A/D accuracy specification may not be met.

2.4 Operation in Power-Managed Modes

The selection of the automatic acquisition time and A/D conversion clock is determined in part by the clock source and frequency while in a power-managed mode.

If the A/D is expected to operate while the device is in a power-managed mode, the ADCS2:ADCS0 bits in ADCON2 should be updated in accordance with the clock source to be used. The ACQT2:ACQT0 bits do not need to be adjusted as the ADCS2:ADCS0 bits adjust the T_{AD} time for the new clock speed. After entering the mode, an A/D acquisition or conversion may be started. Once started, the device should continue to be clocked by the same clock source until the conversion has been completed.

If desired, the device may be placed into the corresponding Idle mode during the conversion. If the device clock frequency is less than 1 MHz, the A/D RC clock source should be selected.

Operation in Sleep mode requires the A/D FRC clock to be selected. If the ACQT2:ACQT0 bits are set to '`000`' and a conversion is started, the conversion will be delayed one instruction cycle to allow execution of the `SLEEP` instruction and entry to Sleep mode. The IDLEN bit (OSCCON<7>) must have already been cleared prior to starting the conversion.

2.5 Configuring Analog Port Pins

The ADCON1, TRISA, TRISF and TRISH registers all configure the A/D port pins. The port pins needed as analog inputs must have their corresponding TRIS bits set (input). If the TRIS bit is cleared (output), the digital output level (V_{OH} or V_{OL}) will be converted.

The A/D operation is independent of the state of the CHS3:CHS0 bits and the TRIS bits.

Note 1:	When reading the PORT register, all pins configured as analog input channels will read as cleared (a low level). Analog conversion on pins configured as digital pins can be performed. The voltage on the pin will be accurately converted.
2:	Analog levels on any pin defined as a digital input may cause the digital input buffer to consume current out of the device's specification limits.

2.6 A/D Conversions

Figure 2-4 shows the operation of the A/D Converter after the GO/$\overline{\text{DONE}}$ bit has been set and the ACQT2:ACQT0 bits are cleared. A conversion is started after the following instruction to allow entry into Sleep mode before the conversion begins.

Figure 2-5 shows the operation of the A/D Converter after the GO/$\overline{\text{DONE}}$ bit has been set, the ACQT2:ACQT0 bits are set to '010' and a 4 TAD acquisition time has been selected before the conversion starts.

Clearing the GO/$\overline{\text{DONE}}$ bit during a conversion will abort the current conversion. The A/D Result register pair will *not* be updated with the partially completed A/D conversion sample. This means the ADRESH:ADRESL registers will continue to contain the value of the last completed conversion (or the last value written to the ADRESH:ADRESL registers).

After the A/D conversion is completed or aborted, a 2 TAD wait is required before the next acquisition can be started. After this wait, acquisition on the selected channel is automatically started.

> **Note:** The GO/$\overline{\text{DONE}}$ bit should **NOT** be set in the same instruction that turns on the A/D. Code should wait at least 2 μs after enabling the A/D before beginning an acquisition and conversion cycle.

2.7 Discharge

The discharge phase is used to initialize the value of the holding capacitor. The array is discharged before every sample. This feature helps to optimize the unity gain amplifier, as the circuit always needs to charge the capacitor array, rather than charge/discharge based on previous-measure values.

FIGURE 2-4: A/D CONVERSION TAD CYCLES (ACQT<2:0> = 000, TACQ = 0)
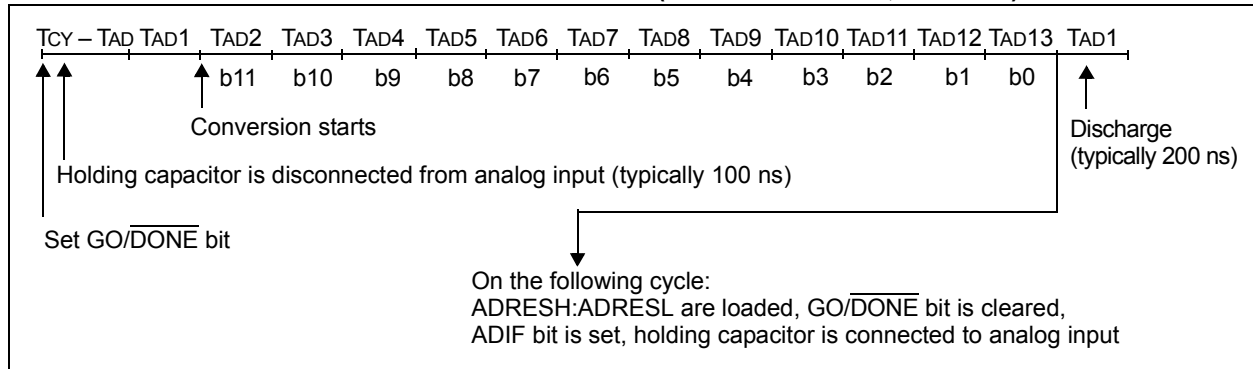
FIGURE 2-5: A/D CONVERSION TAD CYCLES (ACQT<2:0> = 010, TACQ = 4 TAD)
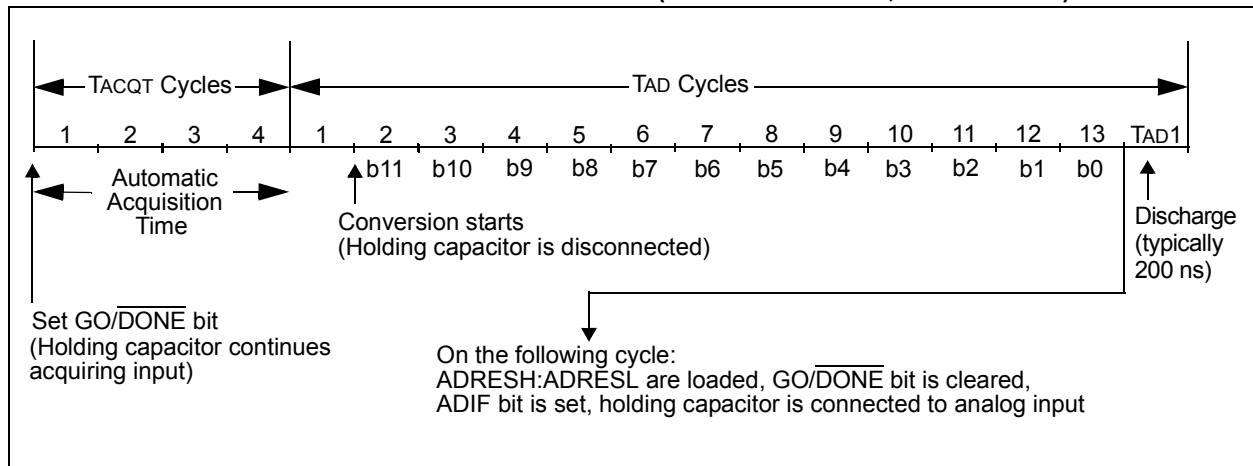
2.8 Use of the ECCP2 Trigger

An A/D conversion can be started by the Special Event Trigger of the ECCP2 module. This requires that the CCP2M3:CCP2M0 bits (CCP2CON<3:0>) be programmed as '1011' and that the A/D module is enabled (ADON bit is set). When the trigger occurs, the GO/$\overline{\text{DONE}}$ bit will be set, starting the A/D acquisition and conversion, and the Timer1 (or Timer3) counter will be reset to zero. Timer1 (or Timer3) is reset to automatically repeat the A/D acquisition period with minimal software overhead (moving ADRESH:ADRESL to the desired location). The appropriate analog input channel must be selected and the minimum acquisition period is either timed by the user, or an appropriate T_{ACQ} time selected before the Special Event Trigger sets the GO/$\overline{\text{DONE}}$ bit (starts a conversion).

If the A/D module is not enabled (ADON is cleared), the Special Event Trigger will be ignored by the A/D module but will still reset the Timer1 (or Timer3) counter.

TABLE 2-2: REGISTERS ASSOCIATED WITH A/D OPERATION

Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Reset Values
INTCON	GIE/GIEH	PEIE/GIEL	TMR0IE	INT0IE	RBIE	TMR0IF	INT0IF	RBIF	(3)
PIR1	—	ADIF	RC1IF	TX1IF	SSP1IF	CCP1IF	TMR2IF	TMR1IF	(3)
PIE1	—	ADIE	RC1IE	TX1IE	SSP1IE	CCP1IE	TMR2IE	TMR1IE	(3)
IPR1	—	ADIP	RC1IP	TX1IP	SSP1IP	CCP1IP	TMR2IP	TMR1IP	(3)
PIR2	OSCFIF	CMIF	—	—	BCL1IF	HLVDIF	TMR3IF	CCP2IF	(3)
PIE2	OSCFIE	CMIE	—	—	BCL1IE	HLVDIE	TMR3IE	CCP2IE	(3)
IPR2	OSCFIP	CMIP	—	—	BCL1IP	HLVDIP	TMR3IP	CCP2IP	(3)
ADRESH	A/D Result Register High Byte								(3)
ADRESL	A/D Result Register Low Byte								(3)
ADCON0	—	—	CHS3	CHS2	CHS1	CHS0	GO/$\overline{\text{DONE}}$	ADON	(3)
ADCON1	—	—	VCFG1	VCFG0	PCFG3	PCFG2	PCFG1	PCFG0	(3)
ADCON2	ADFM	—	ACQT2	ACQT1	ACQT0	ADCS2	ADCS1	ADCS0	(3)
TRISA	TRISA7[1]	TRISA6[1]	TRISA5	TRISA4	TRISA3	TRISA2	TRISA1	TRISA0	(3)
TRISF	TRISF7	TRISF6	TRISF5	TRISF4	TRISF3	TRISF2	TRISF1	TRISF0	(3)
TRISH[2]	TRISH7	TRISH6	TRISH5	TRISH4	TRISH3	TRISH2	TRISH1	TRISH0	(3)

Legend: — = unimplemented, read as '0'. Shaded cells are not used for A/D conversion.

Note 1: PORTA<7:6> and their direction bits are individually configured as port pins based on various primary oscillator modes. When disabled, these bits read as '0'.

2: These registers are not implemented on 64-pin devices.

3: For these Reset values, see the *"PIC18F6390/6490/8390/8490 Data Sheet"* (DS39629).

3.0 SPECIAL FEATURES OF THE CPU

Note:	For additional details on the Configuration bits, refer to **Section 23.1 "Configuration Bits" in** the *"PIC18F6390/6490/8390/8490 Data Sheet"* (DS39629). Device ID information presented in this section is for the PIC18F6393/6493/8393/8493 devices only.

PIC18F6393/6493/8393/8493 devices include several features intended to maximize reliability and minimize cost through elimination of external components. These include:

• Device ID Registers

3.1 Device ID Registers

The Device ID registers are "read-only" registers. They identify the device type and revision to device programmers and can be read by firmware using table reads.

TABLE 3-1: DEVICE IDs

File Name		Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Default/ Unprogrammed Value
3FFFFEh	DEVID1	DEV2	DEV1	DEV0	REV4	REV3	REV2	REV1	REV0	xxxx xxxx[1]
3FFFFFh	DEVID2	DEV10	DEV9	DEV8	DEV7	DEV6	DEV5	DEV4	DEV3	xxxx xxxx[1]

Legend: x = unknown

Note 1: See Register 3-1 and Register 3-2 for DEVID values. DEVID registers are read-only and cannot be programmed by the user.

PIC18F6393/6493/8393/8493

REGISTER 3-1: DEVID1: DEVICE ID REGISTER 1 FOR PIC18F6393/6493/8393/8493 DEVICES

R	R	R	R	R	R	R	R
DEV2	DEV1	DEV0	REV4	REV3	REV2	REV1	REV0
bit 7							bit 0

Legend:		
R = Read-only bit	P = Programmable bit	U = Unimplemented bit, read as '0'
-n = Value when device is unprogrammed		u = Unchanged from programmed state

bit 7-5   **DEV2:DEV0:** Device ID bits
                       See Register 3-2 for a complete listing.

bit 4-0   **REV4:REV0:** Revision ID bits
                       These bits are used to indicate the device revision.

REGISTER 3-2: DEVID2: DEVICE ID REGISTER 2 FOR PIC18F6393/6493/8393/8493 DEVICES

R	R	R	R	R	R	R	R
DEV10	DEV9	DEV8	DEV7	DEV6	DEV5	DEV4	DEV3
bit 7							bit 0

Legend:		
R = Read-only bit	P = Programmable bit	U = Unimplemented bit, read as '0'
-n = Value when device is unprogrammed		u = Unchanged from programmed state

bit 7-0   **DEV10:DEV3:** Device ID bits

Device	DEV10:DEV3 (DEVID2<7:0>)	DEV2:DEV0 (DEVID1<7:5>)
PIC18F6393	0001 1010	000
PIC18F6493	0000 1110	000
PIC18F8393	0001 1010	001
PIC18F8493	0000 1110	001

Preliminary

4.0   ELECTRICAL CHARACTERISTICS

Note: Other than some basic data, this section documents only the PIC18F6393/6493/8393/8493 devices' specifications that differ from those of the PIC18F6390/6490/8390/8490 devices. For detailed information on the electrical specifications shared by the PIC18F6393/6493/8393/8493 and PIC18F6390/6490/8390/8490 devices, see the *"PIC18F6390/6490/8390/8490 Data Sheet"* (DS39629).

Absolute Maximum Ratings[†]

Ambient temperature under bias..-40°C to +125°C

Storage temperature .... -65°C to +150°C

Voltage on any pin with respect to Vss (except VDD and $\overline{\text{MCLR}}$) .... -0.3V to (VDD + 0.3V)

Voltage on VDD with respect to Vss .... -0.3V to +7.5V

Voltage on $\overline{\text{MCLR}}$ with respect to Vss **(Note 2)** .... 0V to +13.25V

Total power dissipation **(Note 1)** 1.0W

Maximum current out of Vss pin ....300 mA

Maximum current into VDD pin ....250 mA

Input clamp current, IIK (VI < 0 or VI > VDD)...±20 mA

Output clamp current, IOK (VO < 0 or VO > VDD) ....±20 mA

Maximum output current sunk by any I/O pin..25 mA

Maximum output current sourced by any I/O pin ....25 mA

Maximum current sunk by all ports ....200 mA

Maximum current sourced by all ports ....200 mA

Note 1: Power dissipation is calculated as follows:
$$P_{DIS} = V_{DD} \times \{I_{DD} - \sum I_{OH}\} + \sum \{(V_{DD} - V_{OH}) \times I_{OH}\} + \sum (V_{OL} \times I_{OL})$$

2: Voltage spikes below Vss at the $\overline{\text{MCLR}}$/VPP/RG5 pin, inducing currents greater than 80 mA, may cause latch-up. Thus, a series resistor of 50-100Ω should be used when applying a "low" level to the $\overline{\text{MCLR}}$/VPP/RG5 pin, rather than pulling this pin directly to Vss.

† NOTICE: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at those or any other conditions above those indicated in the operation listings of this specification is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.

FIGURE 4-1: **PIC18F6393/6493/8393/8493 VOLTAGE-FREQUENCY GRAPH (INDUSTRIAL)**
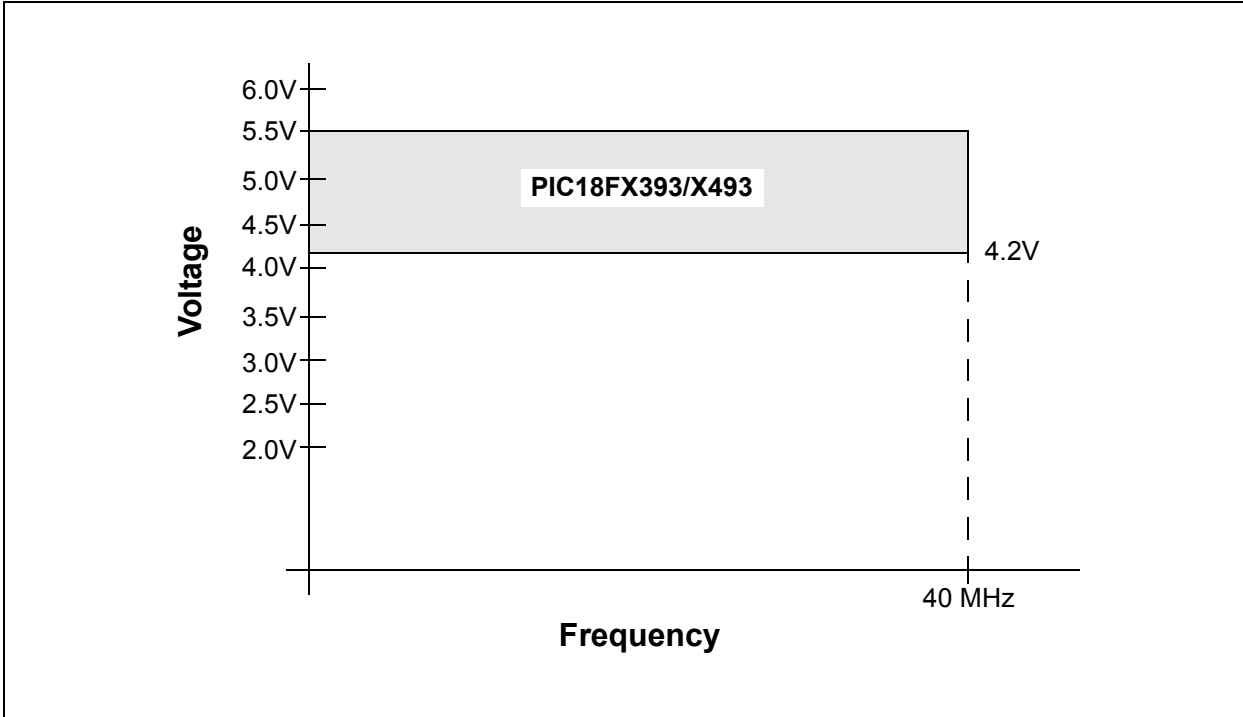
FIGURE 4-2: **PIC18LF6393/6493/8393/8493 VOLTAGE-FREQUENCY GRAPH (INDUSTRIAL)**

F_{MAX} = (16.36 MHz/V) ($V_{DDAPPMIN}$ – 2.0V) + 4 MHz

Note: $V_{DDAPPMIN}$ is the minimum voltage of the PIC® device in the application.
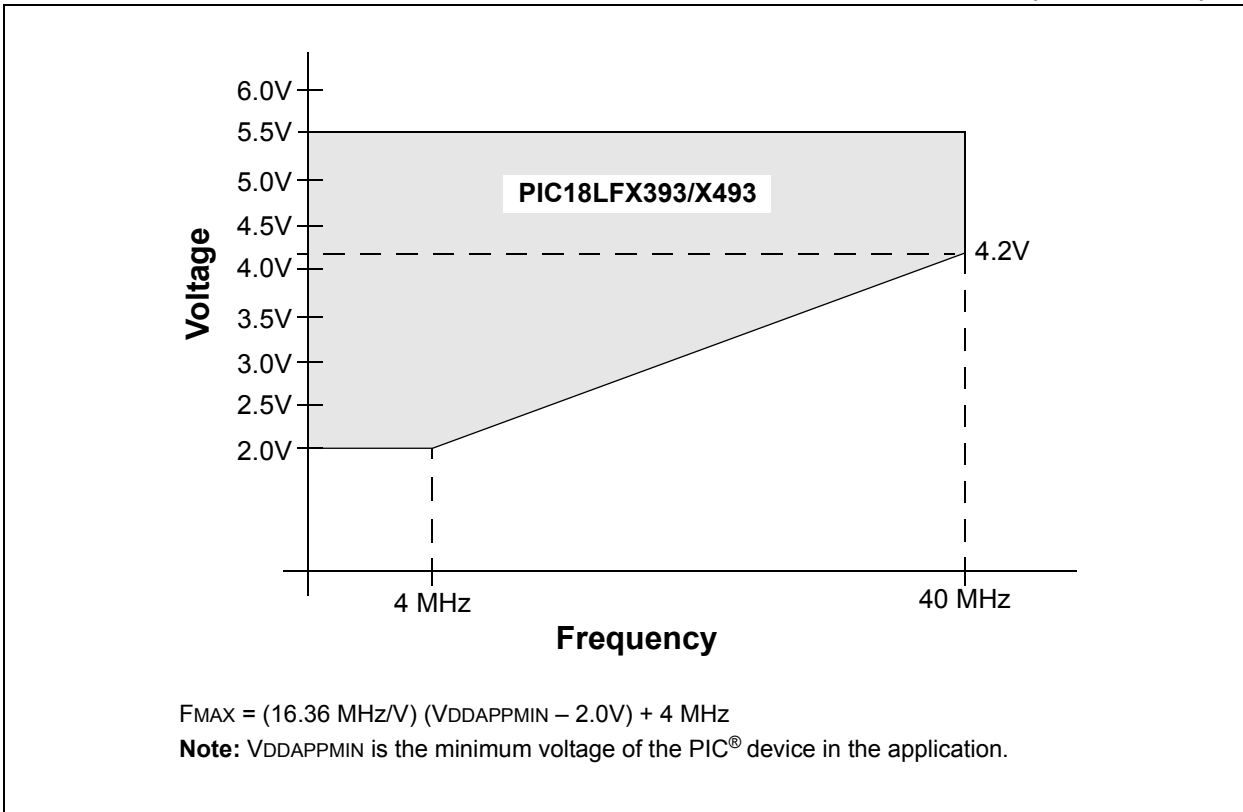
TABLE 4-1: **A/D CONVERTER CHARACTERISTICS: PIC18F6393/6493/8393/8493 (INDUSTRIAL)**

Param No.	Sym	Characteristic	Min	Typ	Max	Units	Conditions	
A01	N$_R$	Resolution	—	—	12	bit		ΔVREF ≥ 3.0V
A03	E$_{IL}$	Integral Linearity Error	—	<±1	±2.0	LSB	VDD = 3.0V	ΔVREF ≥ 3.0V
			—	—	±2.0	LSB	VDD = 5.0V	
A04	E$_{DL}$	Differential Linearity Error	—	<±1	+1.5/-1.0	LSB	VDD = 3.0V	ΔVREF ≥ 3.0V
			—	—	+1.5/-1.0	LSB	VDD = 5.0V	
A06	E$_{OFF}$	Offset Error	—	<±1	±5	LSB	VDD = 3.0V	ΔVREF ≥ 3.0V
			—	—	±3	LSB	VDD = 5.0V	
A07	E$_{GN}$	Gain Error	—	<±1	±2.00	LSB	VDD = 3.0V	ΔVREF ≥ 3.0V
			—	—	±2.00	LSB	VDD = 5.0V	
A10	—	Monotonicity	Guaranteed[1]			—		VSS ≤ VAIN ≤ VREF
A20	ΔVREF	Reference Voltage Range (VREFH – VREFL)	3	—	VDD – VSS	V		For 12-bit resolution
A21	VREFH	Reference Voltage High	VSS + 3.0V	—	VDD + 0.3V	V		For 12-bit resolution
A22	VREFL	Reference Voltage Low	VSS – 0.3V	—	VDD – 3.0V	V		For 12-bit resolution
A25	VAIN	Analog Input Voltage	VREFL	—	VREFH	V		
A30	Z$_{AIN}$	Recommended Impedance of Analog Voltage Source	—	—	2.5	kΩ		
A50	IREF	VREF Input Current[2]	—	—	5	μA		During VAIN acquisition. During A/D conversion cycle.
			—	—	150	μA		

Note 1: The A/D conversion result never decreases with an increase in the input voltage and has no missing codes.

2: VREFH current is from the RA3/AN3/VREF+/SEG17 pin or VDD, whichever is selected as the VREFH source. VREFL current is from the RA2/AN2/VREF-/SEG16 pin or VSS, whichever is selected as the VREFL source.

FIGURE 4-3: A/D CONVERSION TIMING

Note 1: If the A/D clock source is selected as RC, a time of T_{CY} is added before the A/D clock starts. This allows the `SLEEP` instruction to be executed.

2: This is a minimal RC delay (typically 100 ns), which also disconnects the holding capacitor from the analog input.
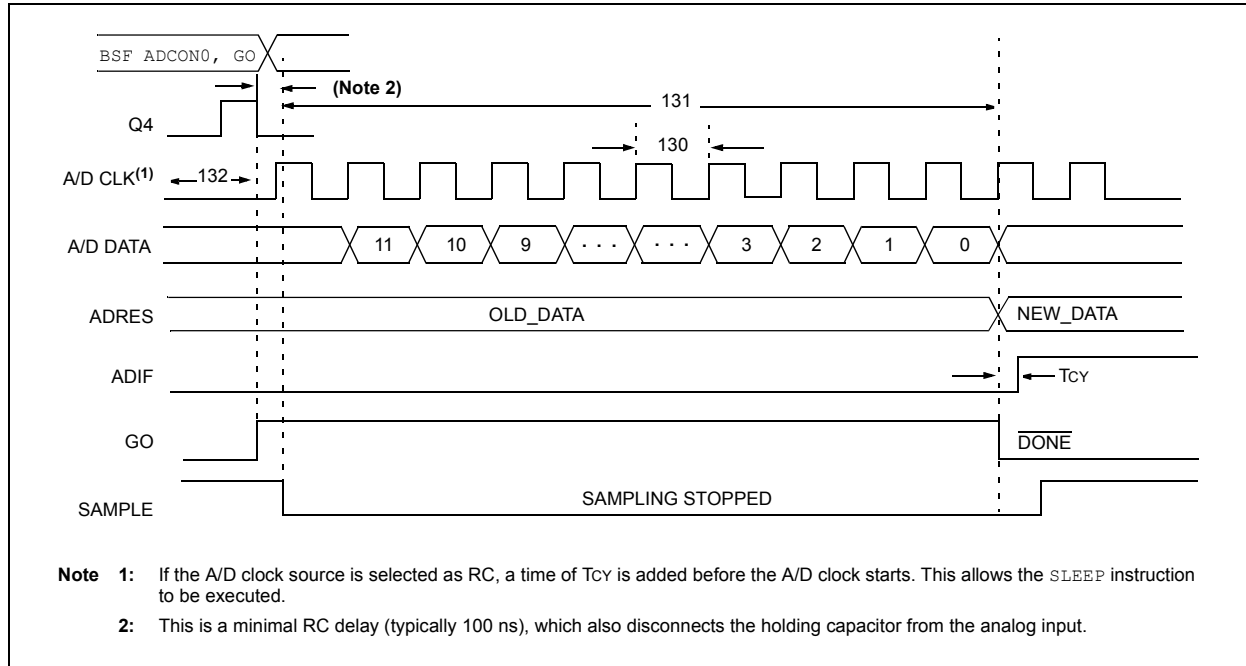
TABLE 4-2: A/D CONVERSION REQUIREMENTS

Param No.	Symbol	Characteristic		Min	Max	Units	Conditions
130	T_{AD}	A/D Clock Period	PIC18**F**XXXX	0.8	12.5[1]	µs	T_{OSC} based, $V_{REF} \geq 3.0V$
			PIC18**LF**XXXX	1.4	25.0[1]	µs	V_{DD} = 3.0V; T_{OSC} based, V_{REF} full range
			PIC18**F**XXXX	—	1	µs	A/D RC mode
			PIC18**LF**XXXX	—	3	µs	V_{DD} = 3.0V; A/D RC mode
131	T_{CNV}	Conversion Time (not including acquisition time)[2]		13	14	T_{AD}	
132	T_{ACQ}	Acquisition Time[3]		1.4	—	µs	
135	T_{SWC}	Switching Time from Convert → Sample		—	**(Note 4)**		
137	T_{DIS}	Discharge Time		0.2	—	µs	

Note 1: The time of the A/D clock period is dependent on the device frequency and the T_{AD} clock divider.

2: ADRES registers may be read on the following T_{CY} cycle.

3: The time for the holding capacitor to acquire the "New" input voltage when the voltage changes full scale after the conversion (V_{DD} to V_{SS} or V_{SS} to V_{DD}). The source impedance (R_S) on the input channels is 50Ω.

4: On the following cycle of the device clock.

5.0 PACKAGING INFORMATION

For packaging information, see the *"PIC18F6390/6490/ 8390/8490 Data Sheet"* (DS39629).

NOTES:

APPENDIX A: REVISION HISTORY

Revision A (September 2007)

Original data sheet for the PIC18F6393/6493/8393/8493 devices.

APPENDIX B: DEVICE DIFFERENCES

The differences between the devices listed in this data sheet are shown in Table B-1.

TABLE B-1: DEVICE DIFFERENCES

Features	PIC18F6393	PIC18F6493	PIC18F8393	PIC18F8493
Number of Pixels the LCD Driver Can Drive	128 (4 x 32)	128 (4 x 32)	192 (4 x 48)	192 (4 x 48)
I/O Ports	Ports A, B, C, D, E, F, G	Ports A, B, C, D, E, F, G	Ports A, B, C, D, E, F, G, H, J	Ports A, B, C, D, E, F, G, H, J
Flash Program Memory	8 Kbytes	16 Kbytes	8 Kbytes	16 Kbytes
Packages	64-Pin TQFP	64-Pin TQFP	80-Pin TQFP	80-Pin TQFP

APPENDIX C: CONVERSION CONSIDERATIONS

This appendix discusses the considerations for converting from previous versions of a device to the ones listed in this data sheet. Typically, these changes are due to the differences in the process technology used. An example of this type of conversion is from a PIC16C74A to a PIC16C74B.

Not Applicable

APPENDIX D: MIGRATION FROM BASELINE TO ENHANCED DEVICES

This section discusses how to migrate from a Baseline device (i.e., PIC16C5X) to an Enhanced MCU device (i.e., PIC18FXXX).

The following are the list of modifications over the PIC16C5X microcontroller family:

Not Currently Available

APPENDIX E: MIGRATION FROM MID-RANGE TO ENHANCED DEVICES

A detailed discussion of the differences between the mid-range MCU devices (i.e., PIC16CXXX) and the enhanced devices (i.e., PIC18FXXX) is provided in *AN716, "Migrating Designs from PIC16C74A/74B to PIC18C442"*. The changes discussed, while device-specific, are generally applicable to all mid-range to enhanced device migrations.

This Application Note is available as Literature Number DS00716.

APPENDIX F: MIGRATION FROM HIGH-END TO ENHANCED DEVICES

A detailed discussion of the migration pathway and differences between the high-end MCU devices (i.e., PIC17CXXX) and the enhanced devices (i.e., PIC18FXXX) is provided in *AN726, "PIC17CXXX to PIC18CXXX Migration"*. This Application Note is available as Literature Number DS00726.

NOTES:

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PIC18F6393/6493/8393/8493

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To order or obtain information, e.g., on pricing or delivery, refer to the factory or the listed sales office.

PART NO.	**X**	**/XX**	**XXX**
Device	**Temperature Range**	**Package**	**Pattern**

Device[1], [2]   PIC18F6393, PIC18F6493, PIC18F8393, PIC18F8493 –
        V_{DD} range: 4.2V to 5.5V
        PIC18LF6393, PIC18LF6493, PIC18LF8393, PIC18LF8493 –
        V_{DD} range: 2.0V to 5.5V

Temperature Range   I   = -40°C to +85°C   (Industrial)
                           E = -40°C to +125°C   (Extended)

Package   PT   =   TQFP (Thin Quad Flatpack)

Pattern   QTP, SQTP, Code or Special Requirements
                           (blank otherwise)

Examples:

a)   PIC18LF6393-I/PT 301 = Industrial temp., TQFP package, Extended V_{DD} limits, QTP pattern #301.

b)   PIC18LF6393-I/PT = Industrial temp., TQFP package, Extended V_{DD} limits.

c)   PIC18F6393-E/PT = Extended temp., TQFP package, normal V_{DD} limits.

Note 1:   F = Standard Voltage Range
                    LF = Wide Voltage Range
     2:   T = in tape and reel TQFP packages only.

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