

# 2N3027-2N3032

### SILICON CONTROLLED RECTIFIER

#### **FEATURES**

- Available as "HR" (high reliability) screened per MIL-PRF-19500, JANTX level. Add "HR" suffix to base part number.
- Available as non-RoHS (Sn/Pb plating), standard, and as RoHS by adding "-PBF" suffix.

#### **MAXIMUM RATINGS**

Characteristic	Symbol	2N3027 2N3030	2N3028 2N3031	2N3029 2N3032		
Repetitive peak off-state voltage	V <sub>DRM</sub>	30V	60V	100V		
Repetitive peak reverse voltage	$V_{RRM}$	30V	60V	100V		
DC on-state current 100°C case 75°C ambient	lτ	500mA 250mA				
Repetitive peak on-state current	I <sub>TRM</sub>	30A				
Surge (non-repetitive) on-state current 50ms 8ms	Ітѕм	5A 8A				
Peak gate current	I <sub>GM</sub>	250mA				
Average gate current	I <sub>G(AV)</sub>	25mA				
Reverse gate voltage	$V_{GR}$	5V				
Reverse gate current	I <sub>GR</sub>	3mA				
Storage temperature range	T <sub>stg</sub>	-65°C to +200°C				
Operating temperature range	T,	-65°C to +150°C				

Blocking voltage ratings apply over the operating temperature range, provided the gate is connected to the cathode through an appropriate resistor, or adequate gate bias is used.

#### ELECTRICAL CHARACTERISTIC (@ 25°C unless otherwise noted) (2N3027-2N3029)

Parameter	Symbol	Min.	Тур.	Max.	Unit	Test Condition
25°C tests					•	
Off state current	I <sub>DRM</sub>	-	0.002	0.100	μА	$R_{GK} = 1K\Omega$ , $V_{DRM} = rating$
Reverse current	I <sub>RRM</sub>	-	0.002	0.100	μΑ	$R_{GK} = 1K\Omega$ , $V_{RRM} = rating$
Reverse gate voltage	$V_{GR}$	5	8	-	V	I <sub>GR</sub> = 0.1mA
Gate trigger current	I <sub>GT</sub>	-5	8	200	μΑ	$R_{GS} = 10K\Omega$ , $V_D = 5V$
Gate trigger voltage	$V_{GT}$	0.400	0.550	0.800	V	$R_{GS} = 100\Omega, V_D = 5V$
On-state voltage	V <sub>T</sub>	0.800	1.200	1.500	V	I <sub>T</sub> = 1A (pulse test)
Holding current	lμ	0.300	0.700	5.000	mA	$R_{GK} = 1K\Omega, V_D = 5V$
Off-state voltage – critical rate of rise	dv/dt	30 15 10	60 30 25	- - -	V/µs	$R_{GK} = 1K\Omega, V_D = 30V (2N3027)$ $R_{GK} = 1K\Omega, V_D = 60V (2N3028)$ $R_{GK} = 1K\Omega, V_D = 100V (2N3029)$
Gate trigger-on pulse width	t <sub>pg(on)</sub>	-	0.070	0.200	μs	$I_G = 10$ mA, $I_T = 1$ A, $V_D = 30$ V
Delay time	t <sub>d</sub>	-	0.080	-	μs	$I_G = 10$ mA, $I_T = 1$ A, $V_D = 30$ V
Rise time	tr	-	0.040	-	μs	I <sub>G</sub> = 10mA, I <sub>T</sub> = 1A, V <sub>D</sub> = 30V
Circuit commutated turn-off time	tg	-	0.700	2.000	μs	$I_T = 1A$ , $I_R = 1A$ , $R_{GK} = 1K\Omega$



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### SILICON CONTROLLED RECTIFIER

Parameter	Symbol	Min.	Тур.	Max.	Unit	Test Condition
150°C Tests						
High temperature off-state current	I <sub>DRM</sub>	-	2	20	μΑ	$R_{GK} = 1K\Omega$ , $V_{DRM} = rating$
High temperature reverse current	I <sub>RRM</sub>	-	20	50	μΑ	$R_{GK} = 1K\Omega$ , $V_{RRM} = rating$
High temperature gate trigger voltage	V <sub>GT</sub>	0.100	0.150	0.600	٧	$R_{GS} = 100\Omega, V_D = 5V$
High temperature holding current	lμ	0.050	0.200	1.000	mA	$R_{GK} = 1K\Omega$ , $V_D = 5V$
-65°C Tests						
Low temperature gate trigger voltage	V <sub>GT</sub>	0.600	0.750	1.100	٧	$R_{GS} = 100\Omega$ , $V_D = 5V$
Low temperature gate trigger current	I <sub>GT</sub>	0	150	1.200	mA	$R_{GS} = 10K\Omega$ , $V_D = 5V$
Low temperature holding current	lμ	0.500	3.500	10	mA	$R_{GK} = 1K\Omega$ , $V_D = 5V$

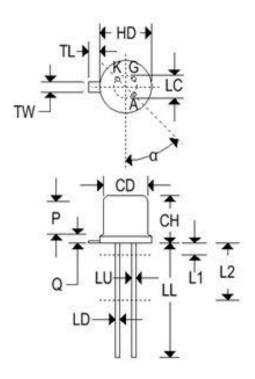
#### **ELECTRICAL CHARACTERISTIC** (@ 25°C unless otherwise noted) (2N3030-2N3032)

25°C tests	icas otherw	, , , , , , , , , , , , , , , , , , ,		•		
Off state current	I <sub>DRM</sub>	-	0.002	0.100	μΑ	$R_{GK} = 1K\Omega$ , $V_{DRM} = rating$
Reverse current	I <sub>RRM</sub>	-	0.002	0.100	μΑ	$R_{GK} = 1K\Omega$ , $V_{RRM} = rating$
Reverse gate voltage	$V_{GR}$	5	8	-	V	I <sub>GR</sub> = 0.1mA
Gate trigger current	I <sub>GT</sub>	-5		20	μΑ	$R_{GS} = 10K\Omega$ , $V_D = 5V$
Gate trigger voltage	$V_{GT}$	0.440		0.600	V	$R_{GS} = 100\Omega, V_D = 5V$
On-state voltage	V <sub>T</sub>	0.800	1.200	1.500	V	I <sub>T</sub> = 1A (pulse test)
Holding current	lн	0.300	1.000	4.000	mA	$R_{GK} = 1K\Omega$ , $V_D = 5V$
		30	60	-		$R_{GK} = 1K\Omega$ , $V_D = 30V$ (2N3030)
Off-state voltage – critical rate of rise	dv/dt	15	30	-	V/µs	$R_{GK} = 1K\Omega$ , $V_D = 60V$ (2N3031)
		10	25	-		$R_{GK} = 1K\Omega$ , $V_D = 100V$ (2N3032)
Gate trigger-on pulse width	t <sub>pg(on)</sub>	-	0.050	0.100	μs	$I_G = 10$ mA, $I_T = 1$ A, $V_D = 30$ V
Delay time	t <sub>d</sub>	-	0.100	-	μs	$I_G = 10$ mA, $I_T = 1$ A, $V_D = 30$ V
Rise time	t <sub>r</sub>	-	0.050	-	μs	$I_G = 10$ mA, $I_T = 1$ A, $V_D = 30$ V
Circuit commutated turn-off time	tg	-	0.700	2.000	μs	$I_T = 1A$ , $I_R = 1A$ , $R_{GK} = 1K$
150°C Tests						
High temperature off-state current	I <sub>DRM</sub>	-	2	20	μΑ	$R_{GK} = 1K\Omega$ , $V_{DRM} = rating$
High temperature reverse current	I <sub>RRM</sub>	-	20	50	μΑ	$R_{GK} = 1K\Omega$ , $V_{RRM} = rating$
High temperature gate trigger voltage	V <sub>GT</sub>	0.100	0.150	0.400	V	$R_{GS} = 100\Omega$ , $V_D = 5V$
High temperature holding current	lμ	0.050	0.300	2.000	mA	$R_{GK} = 1K$ , $V_D = 5V$
-65°C Tests						
Low temperature gate trigger voltage	V <sub>GT</sub>	0.440	0.800	0.950	V	$R_{GS} = 100\Omega$ , $V_D = 5V$
Low temperature gate trigger current	I <sub>GT</sub>	0	0.400	0.500	mA	$R_{GS} = 10K\Omega$ , $V_D = 5V$
Low temperature holding current	lμ	0.500	5.000	8	mA	$R_{GK} = 1K\Omega$ , $V_D = 5V$



#### **MECHANICAL CHARACTERISTICS**

Case	TO-18
Marking	Alpha-numeric
Pin out	See below



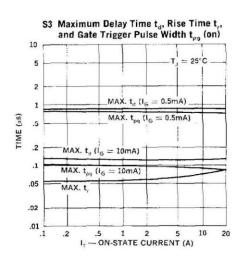
# 2N3027-2N3032

### SILICON CONTROLLED RECTIFIER

	TO-18								
Dim	Inc	hes	Millimeters						
	Min	Max	Min	Max					
CD	0.178	0.195	4.520	4.950					
СН	0.170	0.210	4.320	5.330					
HD	0.209	0.230	5.310	5.840					
LC	0.10	0 TP	2.540 TP						
LD	0.016	0.021	0.410	0.530					
LL	0.500	0.750	12.700	19.050					
LU	0.016	0.019	0.410	0.480					
Lı	55:	0.050	12	1.270					
L2	0.250	¥ .	6.350	1941					
Р	0.100	35	2.540	3328					
Q		0.040		1.020					
TL	0.028	0.048	0.710	1.220					
TW	0.036	0.046	0.910	1.170					
α	45	TP	45°TP						

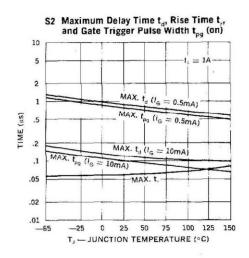


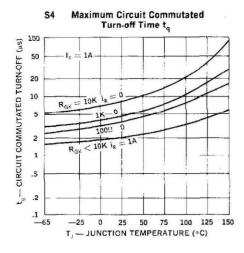
### S1 Maximum Delay Time $t_d$ , Rise Time $t_r$ , and Gate Trigger Pulse Width $t_{pg}$ (on) $I_{\rm F}=1A$ TIME (us) .02 .01 .01 .02 .05 .1 .2 .5 - PULSE GATE CURRENT (mA)

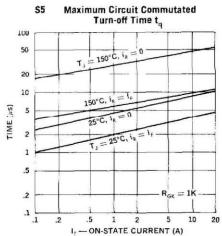


# 2N3027-2N3032

### SILICON CONTROLLED RECTIFIER



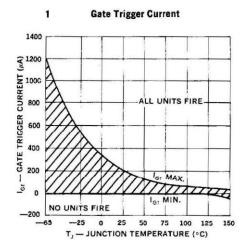




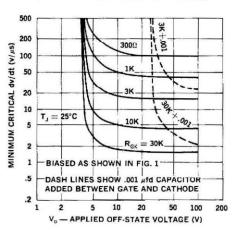


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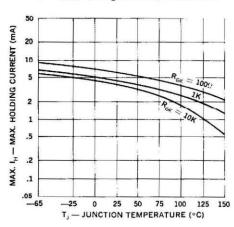
### SILICON CONTROLLED RECTIFIER



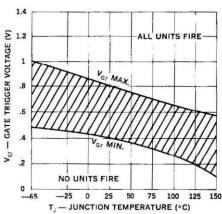
#### 3 Min. Critical dv/dt (25°C - R Bias)



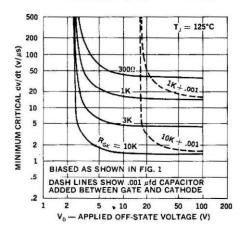
#### 5 Max. Holding Current (Resistor Bias)



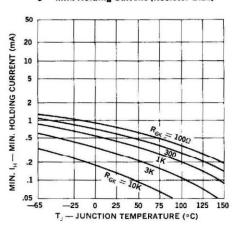
### 2 Gate Trigger Voltage



#### 4 Min. Critical dv/dt (125°C - R Bias)



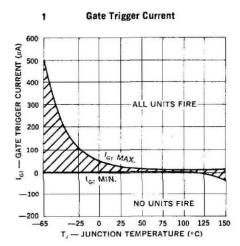
#### 6 Min. Holding Current (Resistor Bias)



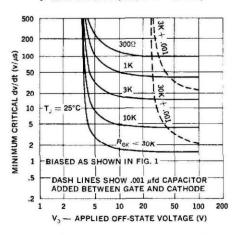


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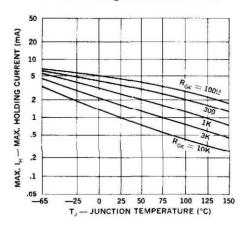
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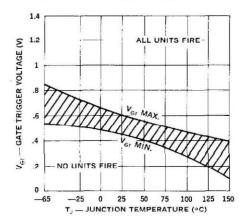
#### 3 Min. Critical dv/dt (25°C - R Bias)



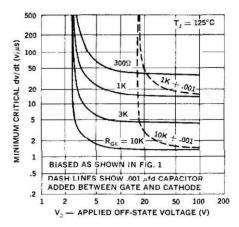
#### 5 Max. Holding Current (Resistor Bias)



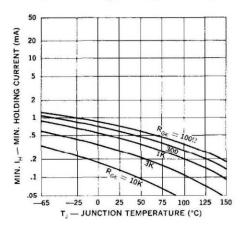
#### 2 Gate Trigger Voltage



#### 4 Min. Critical dv/dt (125°C - R Bias)



#### 6 Min. Holding Current (Resistor Bias)

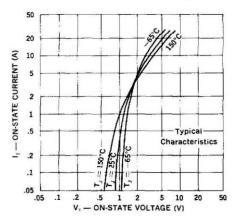




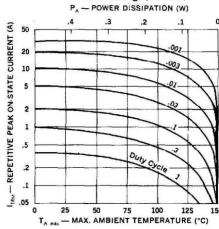
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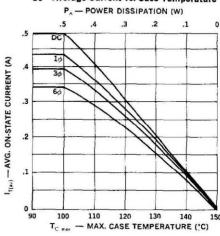




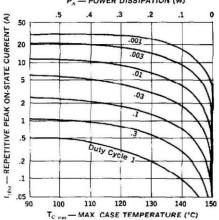
#### C3 Peak Current vs. Ambient Temperature TO-18 Ratings (see note)



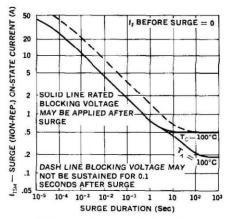
#### C5 Average Current vs. Case Temperature



### Pak Current vs. Case Temperature Pa — POWER DISSIPATION (W)



#### C4 Surge Current vs. Time



### C6 Average Current vs. Ambient Temperature TO-18 Ratings (see note)

