

# SN54BCT652, SN74BCT652 OCTAL BUS TRANSCEIVERS AND REGISTERS WITH 3-STATE OUTPUTS

SCBS038A – AUGUST 1989 – REVISED NOVEMBER 1993

- State-of-the-Art BiCMOS Design Significantly Reduces  $I_{CCZ}$
- ESD Protection Exceeds 2000 V Per MIL-STD-883C, Method 3015; Exceeds 200 V Using Machine Model ( $C = 200$  pF,  $R = 0$ )
- Independent Registers and Enables for A and B Buses
- Multiplexed Real-Time and Stored Data
- Power-Up High-Impedance Mode
- Package Options Include Plastic Small-Outline (DW) Packages, Ceramic Chip Carriers (FK) and Flatpacks (W), and Standard Plastic and Ceramic 300-mil DIPs (JT, NT)

## description

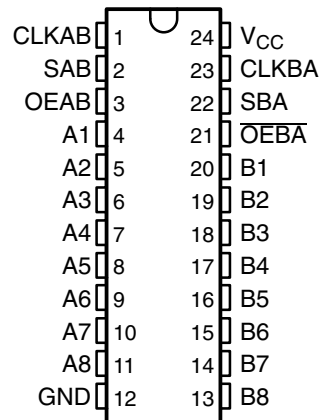
These devices consist of bus transceiver circuits, D-type flip-flops, and control circuitry arranged for multiplexed transmission of data directly from the data bus or from the internal storage registers.

Output-enable (OEAB and  $\overline{OEBA}$ ) inputs are provided to control the transceiver functions. Select-control (SAB and SBA) inputs are provided to select whether real-time or stored data is transferred. The circuitry used for select control eliminates the typical decoding glitch that occurs in a multiplexer during the transition between stored and real-time data. A low input selects real-time data, and a high input selects stored data. Figure 1 illustrates the four fundamental bus-management functions that can be performed with the 'BCT652.

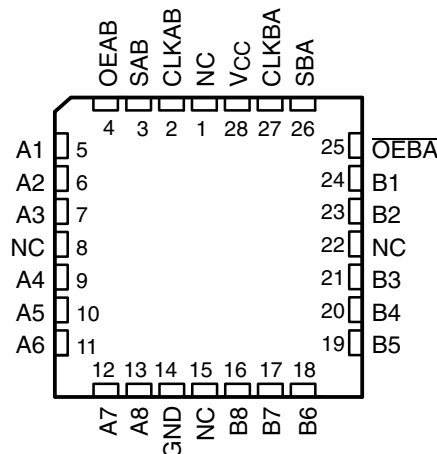
Data on the A or B data bus, or both, can be stored in the internal D-type flip-flops by low-to-high transitions at the appropriate clock (CLKAB or CLKBA) inputs regardless of the select- or enable-control pins. When SAB and SBA are in the real-time transfer mode, it is possible to store data without using the internal D-type flip-flops by simultaneously enabling OEAB and  $\overline{OEBA}$ . In this configuration each output reinforces its input. Therefore, when all other data sources to the two sets of bus lines are at high impedance, each set of bus lines remain at its last state.

The SN54BCT652 is characterized for operation over the full military temperature range of  $-55^{\circ}\text{C}$  to  $125^{\circ}\text{C}$ . The SN74BCT652 is characterized for operation from  $0^{\circ}\text{C}$  to  $70^{\circ}\text{C}$ .

SN54BCT652 . . . JT OR W PACKAGE  
SN74BCT652 . . . DW OR NT PACKAGE  
(TOP VIEW)



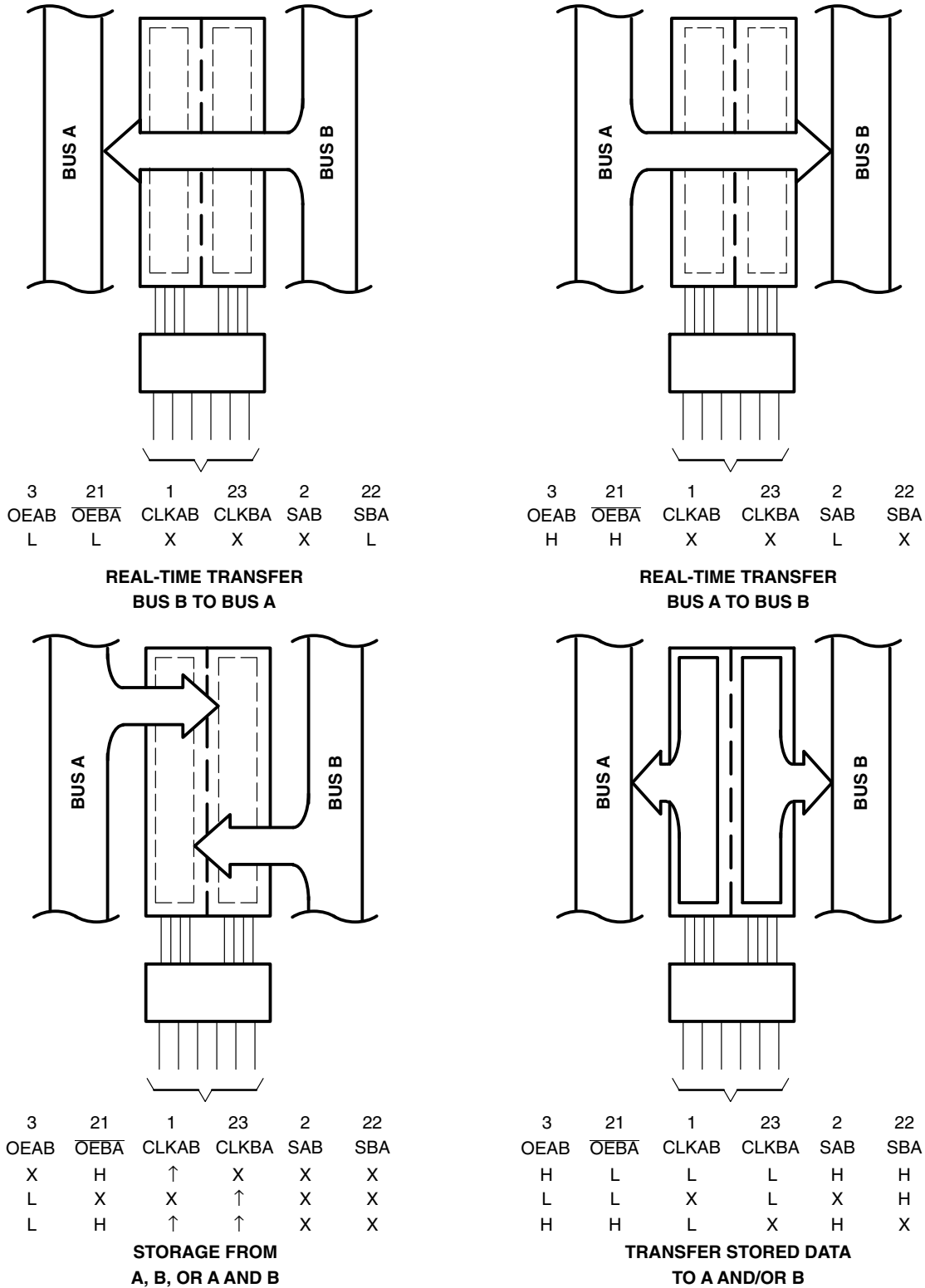
SN54BCT652 . . . FK PACKAGE  
(TOP VIEW)



NC – No internal connection

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**Figure 1. Bus-Management Functions**

Pin numbers shown are for the DW, JT, NT, and W packages.

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FUNCTION TABLE

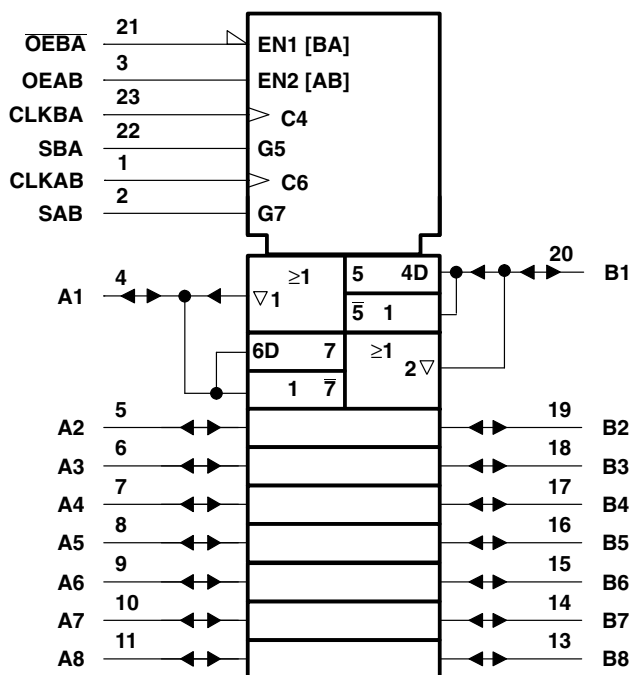
INPUTS						DATA I/O†		OPERATION OR FUNCTION
OEAB	OEBA	CLKAB	CLKBA	SAB	SBA	A1 THRU A8	B1 THRU B8	
L	H	H or L	H or L	X	X	Input	Input	Isolation
L	H	↑	↑	X	X	Input	Input	Store A and B data
X	H	↑	H or L	X	X	Input	Unspecified‡	Store A, hold B
H	H	↑	↑	X‡	X	Input	Output	Store A in both registers
L	X	H or L	↑	X	X	Unspecified‡	Input	Hold A, store B
L	L	↑	↑	X	X‡	Output	Input	Store B in both registers
L	L	X	X	X	L	Output	Input	Real-time B data to A bus
L	L	X	H or L	X	H	Output	Input	Stored B data to A bus
H	H	X	X	L	X	Input	Output	Real-time A data to B bus
H	H	H or L	X	H	X	Input	Output	Stored A data to B bus
H	L	H or L	H or L	H	H	Output	Output	Stored A data to B bus and stored B data to A bus

† The data output functions may be enabled or disabled by a variety of level combinations at the OEAB or OEBA inputs. Data input functions are always enabled; i.e., data at the bus pins is stored on every low-to-high transition on the clock inputs.

‡ Select control = L; clocks can occur simultaneously.

Select control = H; clocks must be staggered in order to load both registers.

## logic symbol§



§ This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12. Pin numbers shown are for the DW, JT, NT, and W packages.



# SN54BCT652, SN74BCT652 OCTAL BUS TRANSCEIVERS AND REGISTERS WITH 3-STATE OUTPUTS

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## recommended operating conditions

		SN54BCT652			SN74BCT652			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
$V_{CC}$	Supply voltage	4.5	5	5.5	4.5	5	5.5	V
$V_{IH}$	High-level input voltage	2			2			V
$V_{IL}$	Low-level input voltage			0.8			0.8	V
$I_{IK}$	Input clamp current			-18			-18	mA
$I_{OH}$	High-level output current			-12			-15	mA
$I_{OL}$	Low-level output current			48			64	mA
$T_A$	Operating free-air temperature	-55		125	0		70	°C

## electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS		SN54BCT652			SN74BCT652			UNIT
				MIN	TYP†	MAX	MIN	TYP†	MAX	
$V_{IK}$		$V_{CC} = 4.5\text{ V}$ ,	$I_I = -18\text{ mA}$			-1.2			-1.2	V
$V_{OH}$		$V_{CC} = 4.5\text{ V}$	$I_{OH} = -3\text{ mA}$	2.4	3.3		2.4	3.3		V
			$I_{OH} = -12\text{ mA}$	2	3.2					
			$I_{OH} = -15\text{ mA}$				2	3.1		
$V_{OL}$		$V_{CC} = 4.5\text{ V}$	$I_{OL} = 48\text{ mA}$	0.38	0.55					V
			$I_{OL} = 64\text{ mA}$				0.42	0.55		
$I_I$	A or B port	$V_{CC} = 5.5\text{ V}$ ,	$V_I = 5.5\text{ V}$		1			1		mA
	Control inputs				1			1		
$I_{IH}^\ddagger$	A or B port	$V_{CC} = 5.5\text{ V}$ ,	$V_I = 2.7\text{ V}$		70			70		$\mu\text{A}$
	Control inputs				20			20		
$I_{IL}^\ddagger$	A or B port	$V_{CC} = 5.5\text{ V}$ ,	$V_I = 0.5\text{ V}$		-0.7			-0.7		mA
	Control inputs				-0.7			-0.7		
$I_{OS}^\S$		$V_{CC} = 5.5\text{ V}$ ,	$V_O = 0$	-100		-225	-100		-225	mA
$I_{CCL}$	A or B port	$V_{CC} = 5.5\text{ V}$ ,	$V_I = 0$		43	69		43	69	mA
$I_{CCH}$	A or B port	$V_{CC} = 5.5\text{ V}$ ,	$V_I = 4.5\text{ V}$		6	10		6	10	mA
$I_{CCZ}$	A or B port	$V_{CC} = 5.5\text{ V}$ ,	$V_I = 0$		10	17		10	17	mA
$C_i$	Control inputs	$V_{CC} = 5\text{ V}$ ,	$V_I = 2.5\text{ V}$ or $0.5\text{ V}$		6			6		pF
$C_{io}$	A or B port	$V_{CC} = 5\text{ V}$ ,	$V_O = 2.5\text{ V}$ or $0.5\text{ V}$		14			14		pF

† All typical values are at  $V_{CC} = 5\text{ V}$ ,  $T_A = 25^\circ\text{C}$ .

‡ For I/O ports, the parameters  $I_{IH}$  and  $I_{IL}$  include the off-state output current.

§ Not more than one output should be tested at a time, and the duration of the test should not exceed one second.

## timing requirements over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

		$V_{CC} = 5\text{ V}$ , $T_A = 25^\circ\text{C}$		SN54BCT652		SN74BCT652		UNIT
		MIN	MAX	MIN	MAX	MIN	MAX	
$f_{\text{clock}}$	Clock frequency	0	77	0	77	0	77	MHz
$t_w$	Pulse duration, CLK high or low	6.5		7		6.5		ns
$t_{su}$	Setup time, A or B before CLKAB $\uparrow$ or CLKBA $\uparrow$	5		6		5		ns
$t_h$	Hold time, A or B after CLKAB $\uparrow$ or CLKBA $\uparrow$	1		1		1		ns



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switching characteristics over recommended ranges of supply voltage and operating free-air temperature,  $C_L = 50$  pF (unless otherwise noted) (see Note 2)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	$V_{CC} = 5$ V, $T_A = 25^\circ$ C			SN54BCT652		SN74BCT652		UNIT
			MIN	TYP	MIN	MIN	MAX	MIN	MAX	
$f_{max}$			77			77		77		MHz
$t_{PLH}$	CLKBA	A	2.6	6.9	8.9	2.6	11.6	2.6	10.5	ns
$t_{PHL}$			2.8	6.8	8.8	2.8	10.7	2.8	9.9	
$t_{PLH}$	CLKAB	B	2.6	6.9	8.9	2.6	11.6	2.6	10.5	ns
$t_{PHL}$			2.8	6.8	8.8	2.8	10.7	2.8	9.9	
$t_{PLH}$	A	B	1.7	5.8	7.5	1.7	10.3	1.7	8.9	ns
$t_{PHL}$			2.4	6.5	8.2	2.4	11	2.4	9.8	
$t_{PLH}$	B	A	1.7	5.8	7.5	1.7	10.3	1.7	8.9	ns
$t_{PHL}$			2.4	6.5	8.2	2.4	11	2.4	9.8	
$t_{PLH}$	SBA† (with B high)	A	3.5	8.8	10.8	3.5	14.2	3.5	13.1	ns
$t_{PHL}$			2.4	5.9	7.7	2.4	9.1	2.4	8.5	
$t_{PLH}$	SBA† (with B low)	A	3	7.6	9.7	3	12.4	3	11.3	ns
$t_{PHL}$			3.8	8.3	10.4	3.8	12.9	3.8	12.5	
$t_{PLH}$	SAB† (with A high)	B	3.5	8.8	10.8	3.5	14.2	3.5	13.1	ns
$t_{PHL}$			2.4	5.9	7.7	2.4	9.1	2.4	8.5	
$t_{PLH}$	SAB† (with A low)	B	3	7.6	9.7	3	12.4	3	11.3	ns
$t_{PHL}$			3.8	8.3	10.4	3.8	12.9	3.8	12.5	
$t_{PZH}$	$\overline{OEBA}$	A	2.5	7.2	8.9	2.5	11.2	2.5	10.6	ns
$t_{PZL}$			3.2	8.1	10.1	3.2	12.6	3.2	12	
$t_{PHZ}$	$\overline{OEBA}$	A	2.8	6.7	8.6	2.8	10.9	2.8	10	ns
$t_{PLZ}$			2.4	6.3	8.4	2.4	10.5	2.4	9.5	
$t_{PZH}$	OEAB	B	1.5	5.4	7.1	1.5	9	1.5	8.1	ns
$t_{PZL}$			2.3	6.2	8.1	2.3	10.3	2.3	9.3	
$t_{PHZ}$	OEAB	B	3.5	8.2	10	3.5	12.2	3.5	11.6	ns
$t_{PLZ}$			2.8	7.2	9.5	2.8	12	2.8	11.3	

† These parameters are measured with the internal output state of the storage register opposite to that of the bus input.

NOTE 2: Load circuits and voltage waveforms are shown in Section 1.

**PACKAGING INFORMATION**

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
5962-9155301MKA	ACTIVE	CFP	W	24	1	TBD	A42	N / A for Pkg Type	-55 to 125	5962-9155301MK A SNJ54BCT652W	
SN74BCT652DW	ACTIVE	SOIC	DW	24	25	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	BCT652	
SN74BCT652NT	OBSOLETE	PDIP	NT	24		TBD	Call TI	Call TI	0 to 70		
SN74BCT652NTE4	OBSOLETE	PDIP	NT	24		TBD	Call TI	Call TI	0 to 70		
SNJ54BCT652W	ACTIVE	CFP	W	24	1	TBD	A42	N / A for Pkg Type	-55 to 125	5962-9155301MK A SNJ54BCT652W	

(1) The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBSOLETE:** TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

**TBD:** The Pb-Free/Green conversion plan has not been defined.

**Pb-Free (RoHS):** TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

**Pb-Free (RoHS Exempt):** This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

**Green (RoHS & no Sb/Br):** TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

<sup>(6)</sup> Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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- Catalog: [SN74BCT652](#)
- Military: [SN54BCT652](#)

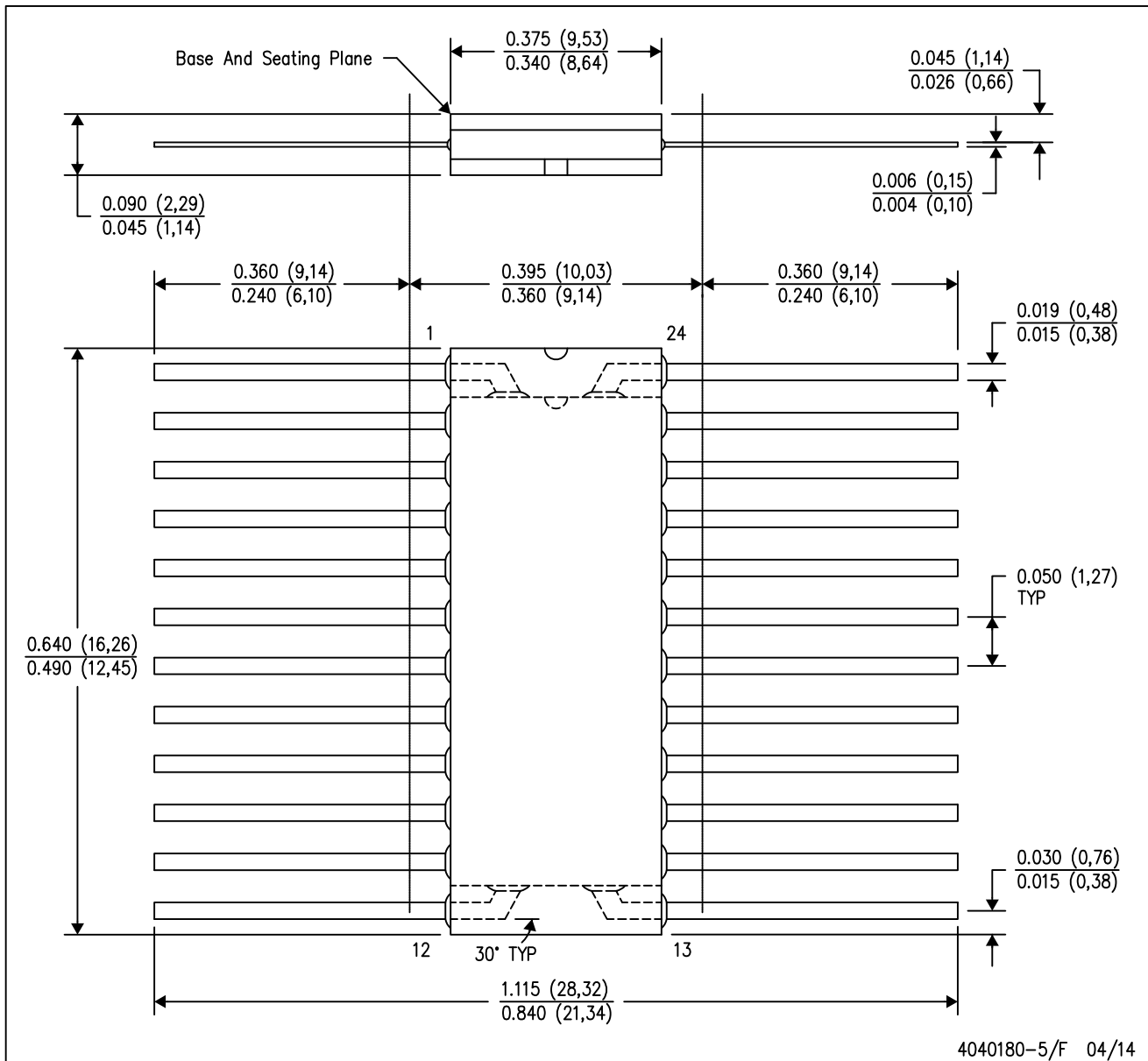
NOTE: Qualified Version Definitions:

- Catalog - TI's standard catalog product
- Military - QML certified for Military and Defense Applications



W (R-GDFP-F24)

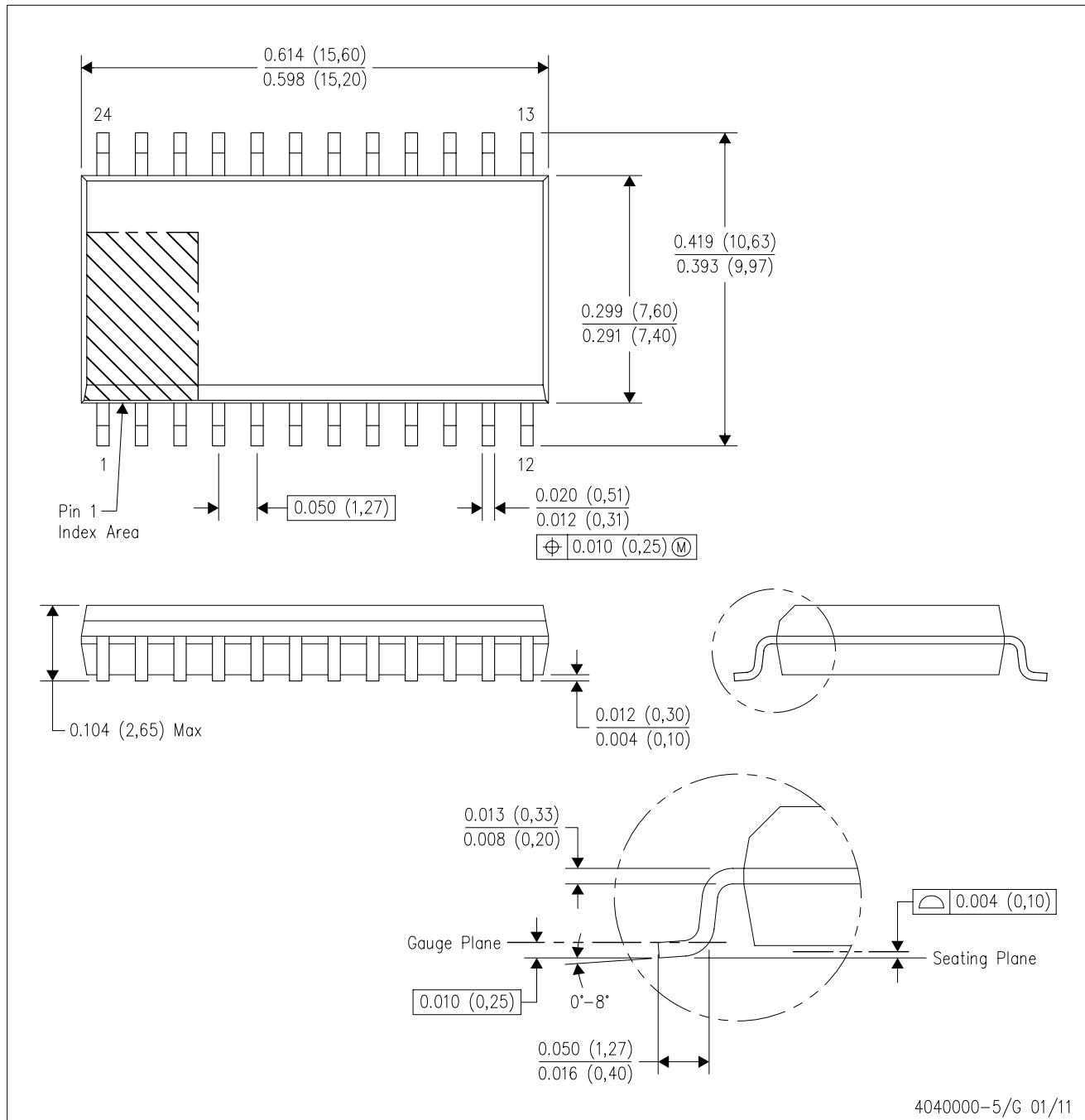
CERAMIC DUAL FLATPACK



- NOTES:
- A. All linear dimensions are in inches (millimeters).
  - B. This drawing is subject to change without notice.
  - C. This package can be hermetically sealed with a ceramic lid using glass frit.
  - D. Index point is provided on cap for terminal identification only.
  - E. Falls within Mil-Std 1835 GDFP2-F20

DW (R-PDSO-G24)

PLASTIC SMALL OUTLINE



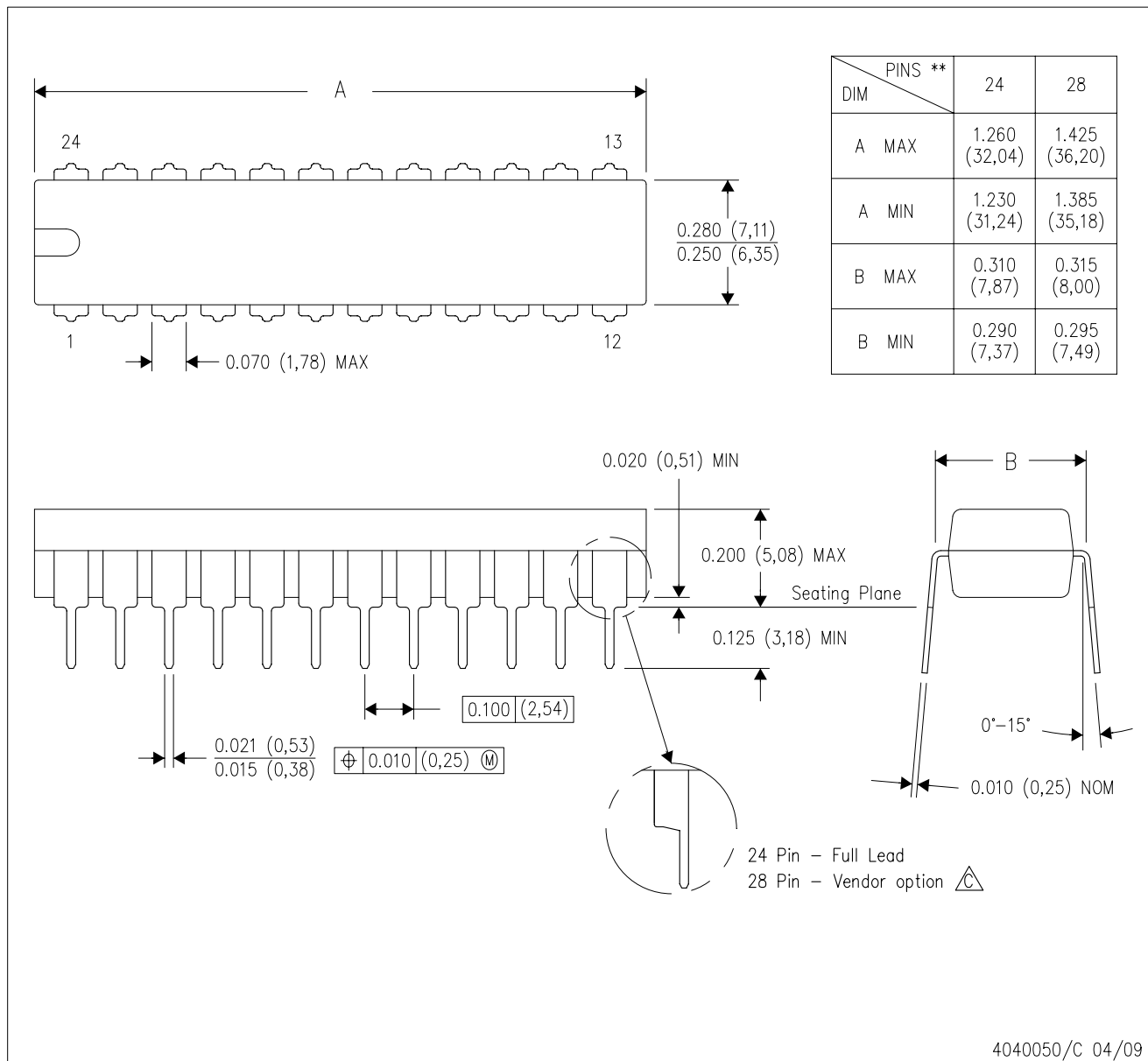
- NOTES:
- A. All linear dimensions are in inches (millimeters). Dimensioning and tolerancing per ASME Y14.5M-1994.
  - B. This drawing is subject to change without notice.
  - C. Body dimensions do not include mold flash or protrusion not to exceed 0.006 (0,15).
  - D. Falls within JEDEC MS-013 variation AD.


# MECHANICAL DATA

NT (R-PDIP-T\*\*)

PLASTIC DUAL-IN-LINE PACKAGE

24 PINS SHOWN



- NOTES:
- A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M-1994.
  - B. This drawing is subject to change without notice.
  -  The 28 pin end lead shoulder width is a vendor option, either half or full width.

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Medical	<a href="http://www.ti.com/medical">www.ti.com/medical</a>
Security	<a href="http://www.ti.com/security">www.ti.com/security</a>
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