## Rochester Electronics Manufactured Components

**Rochester** branded components are manufactured using either die/wafers purchased from the original suppliers or Rochester wafers recreated from the original IP. All recreations are done with the approval of the OCM.

**Parts** are tested using original factory test programs or Rochester developed test solutions to guarantee product meets or exceed the OCM data sheet.

## Quality Overview

- ISO-9001
- AS9120 certification
- Qualified Manufacturers List (QML) MIL-PRF-35835
    - Class Q Military
    - Class V Space Level
- Qualified Suppliers List of Distributors (QSLD)

    • Rochester is a critical supplier to DLA and meets all industry and DLA standards.

**Rochester Electronics, LLC is committed to** supplying products that satisfy customer expectations for quality and are equal to those originally supplied by industry manufacturers.

The original manufacturer's datasheet accompanying this document reflects the performance and specifications of the Rochester manufactured version of this device. Rochester Electronics guarantees the performance of its semiconductor products to the original OEM specifications. 'Typical' values are for reference purposes only. Certain minimum or maximum ratings may be based on product characterization, design, simulation, or sample testing.

# Am29818A

## Pipeline Register with SSR™ Diagnostics
### Higher Speed Version of Am29818

## DISTINCTIVE CHARACTERISTICS

- High-speed noninverting 8-bit parallel register for any data path or pipelining application
- WCS (Writable Control Store) pipeline register
  - Load WCS from serial register
  - Read WCS via serial scan
- Alternate sourced as SN54/74S818

- High-speed 8-bit "shadow register" with serial shift mode for Serial Shadow Register (SSR) Diagnostics
  - Controllability: serial scan in new machine state
  - Observability: serial scan out diagnostics routine results
- Speed comparable with that of 'AS374 register
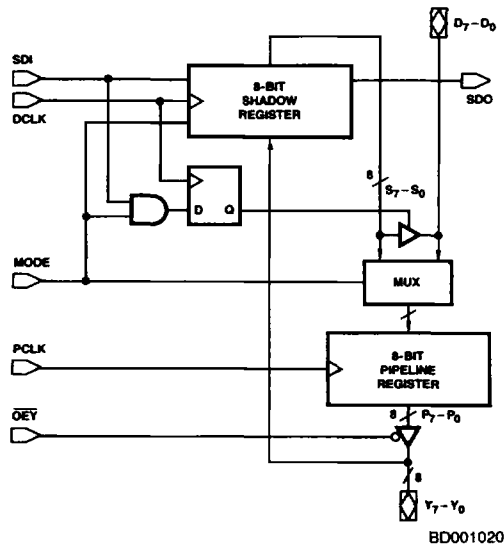
## GENERAL DESCRIPTION

The Am29818A is a high-speed, general-purpose pipeline register with an on-board shadow register for performing Serial Shadow Register (SSR) Diagnostics and/or Writable Control Store loading.

The D-to-Y path provides an 8-bit parallel data path pipeline register for *normal* system operation. The shadow register can load parallel data to or from the pipeline register and *can output data through the D input port (as in WCS loading).*
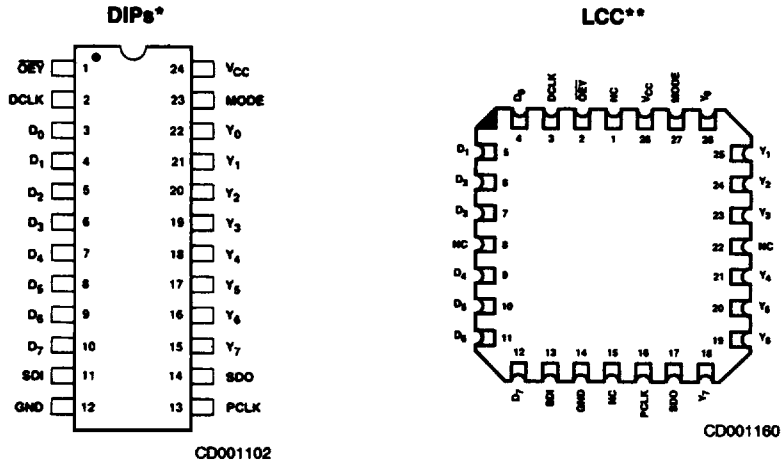
The 8-bit shadow register has multiplexer inputs that select parallel inputs from the Y-port or adjacent bits in the shadow register to operate as a shift register. In the serial shift mode, SDI is shifted into the '0' location of the Shadow register and the contents of '7' location appear at the SDO output. This register can then participate in a serial loop throughout the system where normal data, address, status and control registers are replaced with Am29818A Diagnostic Pipeline Registers. The loop can be used to scan in a complete test routine starting point (data, address, etc.). Then after a specified number of clock cycles, the data clocked out can be compared to the expected results. WCS loading can be accomplished using the same technique. An instruction word can be serially shifted into the shadow register and written into the WCS RAM by enabling the D output.

## BLOCK DIAGRAM



BD001020

| Publication # | Rev. | Amendment |
|---|---|---|
| 08611 | C | /0 |

Issue Date: **January 1988**

## CONNECTION DIAGRAMS
## Top View

### DIPs*

| | | | |
|---|---|---|---|
| OEY | 1 | 24 | Vcc |
| DCLK | 2 | 23 | MODE |
| D0 | 3 | 22 | Y0 |
| D1 | 4 | 21 | Y1 |
| D2 | 5 | 20 | Y2 |
| D3 | 6 | 19 | Y3 |
| D4 | 7 | 18 | Y4 |
| D5 | 8 | 17 | Y5 |
| D6 | 9 | 16 | Y6 |
| D7 | 10 | 15 | Y7 |
| SDI | 11 | 14 | SDO |
| GND | 12 | 13 | PCLK |

CD001102

### LCC**

CD001160

*Also available in 24-Pin Flatpack and Small Outline package; pinout identical to DIPs.
**Also available in 28-Pin PLCC; pinout identical to LCC.

## ORDERING INFORMATION

### Standard Products

AMD standard products are available in several packages and operating ranges. The order number (Valid Combination) is formed by a combination of: a. **Device Number**
b. **Speed Option** (if applicable)
c. **Package Type**
d. **Temperature Range**
e. **Optional Processing**

AM29818A    P    C    B

**e. OPTIONAL PROCESSING**
Blank = Standard processing
B = Burn-in

**d. TEMPERATURE RANGE**
C = Commercial (0 to +70°C)
E = Extended Commercial (−55 to +125°C)

**c. PACKAGE TYPE**
P = 24-Pin Slim Plastic DIP (PD3024)
D = 24-Pin Slim Ceramic DIP (CD3024)
S = 24-Pin Plastic Small Outline Package (SO 024)
J = 28-Pin Plastic Leaded Chip Carrier (PL 028)
L = 28-Pin Ceramic Leadless Chip Carrier (CL 028)

**b. SPEED OPTION**
Not Applicable

**a. DEVICE NUMBER/DESCRIPTION**
Am29818A
Pipeline Register with SSR Diagnostics
(Higher Speed Version of Am29818 & Am29818-1)

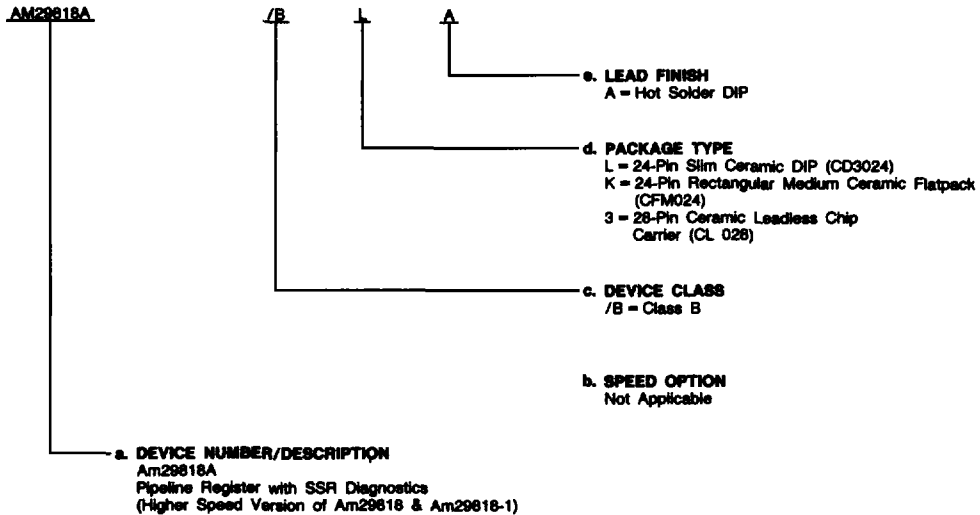| Valid Combinations | |
|---|---|
| AM29818A | PC, PCB, DC, DCB, DE, SC, JC, LC |

### Valid Combinations

Valid Combinations list configurations planned to be supported in volume for this device. Consult the local AMD sales office to confirm availability of specific valid combinations, to check on newly released combinations, and to obtain additional data on AMD's standard military grade products.

# ORDERING INFORMATION (Cont'd.)

## APL Products

AMD products for Aerospace and Defense applications are available in several packages and operating ranges. APL (Approved Products List) products are fully compliant with MIL-STD-883C requirements. The order number (Valid Combination) for APL products is formed by a combination of:

a. **Device Number**
b. **Speed Option** (if applicable)
c. **Device Class**
d. **Package Type**
e. **Lead Finish**

AM29818A          /B      L      A

**e. LEAD FINISH**
A = Hot Solder DIP

**d. PACKAGE TYPE**
L = 24-Pin Slim Ceramic DIP (CD3024)
K = 24-Pin Rectangular Medium Ceramic Flatpack (CFM024)
3 = 28-Pin Ceramic Leadless Chip Carrier (CL 028)

**c. DEVICE CLASS**
/B = Class B

**b. SPEED OPTION**
Not Applicable

**a. DEVICE NUMBER/DESCRIPTION**
Am29818A
Pipeline Register with SSR Diagnostics
(Higher Speed Version of Am29818 & Am29818-1)

| Valid Combinations | |
|---|---|
| AM29818A | /BLA, /BKA, /B3A |

### Valid Combinations

Valid Combinations list configurations planned to be supported in volume for this device. Consult the local AMD sales office to confirm availability of specific valid combinations or to check for newly released valid combinations.

### Group A Tests

Group A tests consist of Subgroups
1, 2, 3, 7, 8, 9, 10, 11.

# PIN DESCRIPTION

**$D_0 - D_7$  Parallel Data Inputs (Input/Output)**
Parallel data input to the pipeline register or parallel data output from the shadow register (see Function Table for control modes).

**DCLK  Diagnostics Clock (Input)**
Diagnostics/WCS clock for loading shadow register (serial or parallel modes — see Function Table).

**MODE  Mode Control (Input)**
Control input for pipeline register multiplexer and shadow register control (see Function Table).

**$\overline{OEY}$  Y-Port Output Enable (Input; Active LOW)**
Active-LOW output enable for Y-port.

**PCLK  Pipeline Register Clock (Input)**
Pipeline register clock input loads D-port or shadow register contents on LOW-to-HIGH transition.

**SDI  Serial Data Input (Input)**
Input to shadow register (see Function Table).

**SDO  Serial Data Output (Output)**
Output from shadow register.

**$Y_0 - Y_7$  Parallel Data Outputs (Input/Output)**
Data outputs from the pipeline register and parallel inputs to the shadow register.

## FUNCTIONAL DESCRIPTION

Data transfers into the shadow register occur on the LOW-to-HIGH transition of DCLK. MODE and SDI determines what data source will be loaded. The pipeline register is loaded on the LOW-to-HIGH transition of PCLK. MODE selects whether the data source is the data input or the shadow register output. Because of the independence of the clock inputs data can be shifted in the shadow register via DCLK and loaded into the pipeline register from the data input via PCLK simultaneously. As long as no set-up or hold times are violated, this simultaneous operation is legal.

| Inputs | | | | Outputs | | | |
|---|---|---|---|---|---|---|---|
| SDI | MODE | DCLK | PCLK | SDO | Shadow Register | Pipeline Register | Operation |
| X | L | ↑ | X | $S_7$ | $S_i \leftarrow S_{i-1}$<br>$S_0 \leftarrow SDI$ | NA | Serial Shift; $D_7 - D_0$ Disabled |
| X | L | X | ↑ | $S_7$ | NA | $P_i \leftarrow D_i$ | Normal Load Pipeline Register |
| L | H | ↑ | X | SDI | $S_i \leftarrow Y_i$ | NA | Load Shadow Register from Y; $D_7 - D_0$ Disabled |
| X | H | X | ↑ | SDI | NA | $P_i \leftarrow S_i$ | Load Pipeline Register from Shadow Register |
| H | H | ↑ | X | SDI | Hold* | NA | Hold Shadow Register; $D_7 - D_0$ Enabled* |

*Although not shown, Hold is implemented by gating DCLK internally.
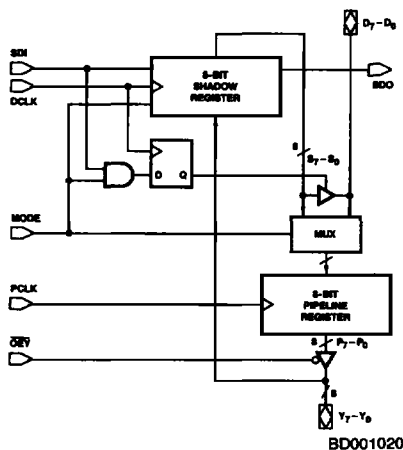
**FUNCTION TABLE DEFINITIONS**

**INPUTS**

H = HIGH
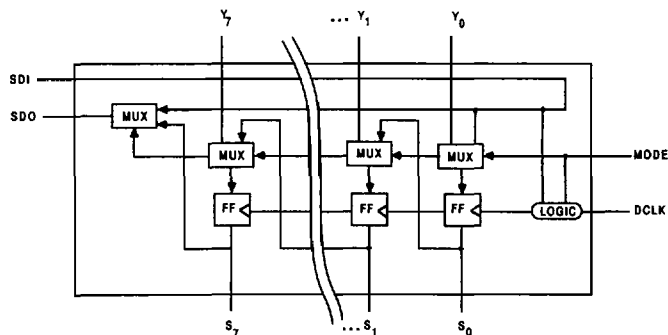L = LOW
X = Don't Care
↑ = LOW-to-HIGH transition

**OUTPUTS**

$S_7 - S_0$ = Shadow Register outputs
$P_7 - P_0$ = Pipeline Register outputs
$D_7 - D_0$ = Data I/O port
$Y_7 - Y_0$ = Y I/O port
NA = Not applicable output is not a function of the specified input combinations.

## BLOCK DIAGRAM



BD001020

## SHADOW REGISTER



BD006770

# An Introduction to Serial Shadow Register (SSR) Diagnostics

## Diagnostics

A diagnostics capability provides the necessary functionality as well as a systematic method for detecting and pin-pointing hardware-related failures in a system. This capability must be able to both *observe* intermediate test points and *control* intermediate signals - address, data, control and status - to exercise all portions of the system under test. These two capabilities – observability and controllability – provide the ability to establish a desired set of input conditions and state register values, sample the necessary outputs, and determine whether the system is functioning correctly.
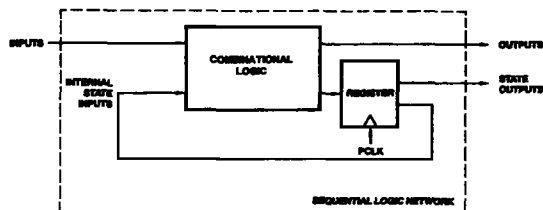
## Testing Combinational and Sequential Networks

The problem of testing a combinational logic network is well understood (Figure 1). Sets of input signals (test vectors) are applied to the network and the network outputs are compared to the set of computed outputs (result vectors). In some cases sets of test vectors and result vectors can be generated in a computer-aided environment, minimizing engineering effort. Additionally, fault coverage analysis can be automated to provide a measure of how efficient a set of test vectors is at pin-pointing hardware failures. For example, a popular measure of fault coverage computes the percentage of stuck-at-ones (nodes with outputs always HIGH) and stuck-at-zeros (nodes with outputs always LOW) a given set at test vectors will discover.



DF000071

## Figure 1. Combinational Logic Network

A sequential network (Figure 2) is much more difficult to test systematically. The outputs of a sequential network depend not only on the present inputs but also on the internal state of the network. Initializing the internal state register to the value necessary to test a given set of inputs is difficult at best, and not easily automated. Additionally, observing the internal state of a sequential network can be very difficult and time consuming if the state information is not directly available. For example, consider the problem of determining the value of an internal 16-bit counter if only a carry-out signal is available. The counter must be clocked until it reaches the carry-out state and the starting value computed. Up to 65,535 clock cycles may be necessary! An easier method must exist. Serial Shadow Register diagnostics provides this method.
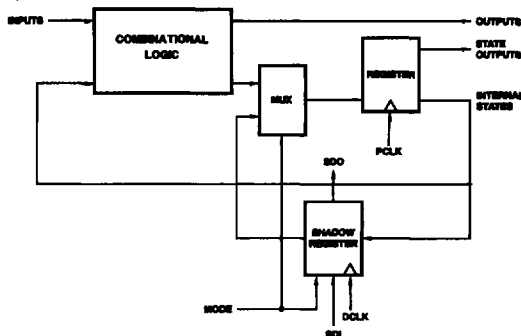


DF000061

## Figure 2. Sequential Network

## Serial Shadow Register Diagnostics

Serial Shadow Register diagnostics provides sufficient observability and controllability to turn any sequential network into a combinational network. This is accomplished by providing the means to both initialize (control) and sample (observe) the state elements of a sequential network. Figure 3 shows the method by which serial shadow register diagnostics accomplishes these two functions.
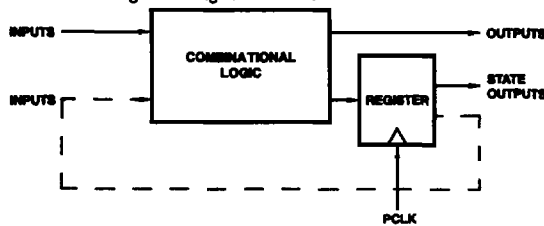


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## Figure 3. SSR Diagnostics Diagram

Serial Shadow Register diagnostics utilizes an extra multiplexer on the input of each state register and a duplicate or shadow of each state flip/flop in an additional register. The shadow register can be loaded serially via the serial data input (thus the name Serial Shadow Register diagnostics) for controllability. Once the desired state information is loaded into the serial register it can be transferred into the internal state register by selecting the multiplexer and clocking the state register with PLCK. This allows any internal state to be set to a desired state in a simple, quick, and systematic manner.

Internal state information can be sampled by loading the serial register from the state register outputs. This state information can then be shifted out via the serial data output to provide observability. Notice that the serial data inputs and outputs can be cascaded to make long chains of state information available on a minimum number of connections.

In effect, Serial Shadow Register diagnostics breaks the normal feedback path of the sequential network and establishes a logical path with which inputs can be defined and outputs sampled (Figure 4). This means that those techniques which have been developed to test combinational networks can be applied to any sequential network in which Serial Shadow Register diagnostics is utilized.
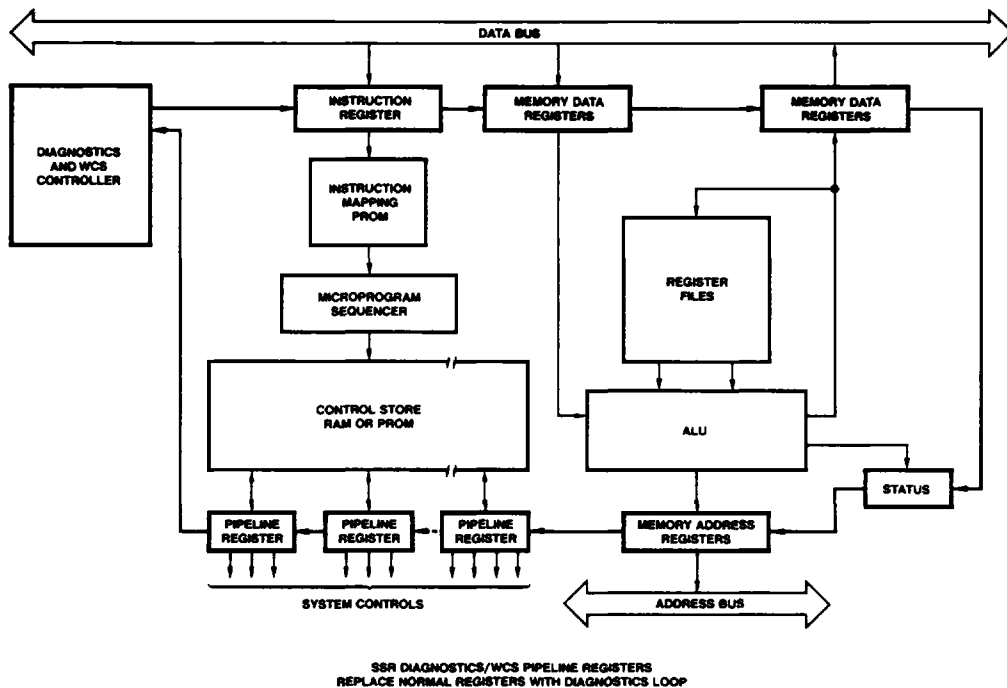


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## Figure 4. SSR Diagnostics Logical Path

## A Typical Computer Architecture with SSR Diagnostics

When normal pipeline registers are replaced by SSR diagnostics pipeline registers system debug and diagnostics are easily implemented. State information which was inaccessible is now both observable and controllable. Figure 5 shows a typical computer system using the Am29818A.

Serial paths have been added to all the important state registers (macro instruction, data, status, address, and micro instruction registers). This extra path will make it easier to diagnose system failures by breaking the feed-back paths and turning sequential state machines into combinatorial logic blocks. For example, the status outputs of the ALU may be checked by loading the micro instruction register with the necessary micro instruction. The desired ALU function is then executed and the status outputs captured in the status register. The status bits can then be serially shifted out and checked for validity.

A single diagnostic loop was shown in Figure 5 for simplicity, but several loops can be employed in more complicated systems to reduce scan time. Additionally, the Am29818A's can be used to sample intermediate test points not associated with normal state information. These additional test points can further ease diagnostics, testability and debug.
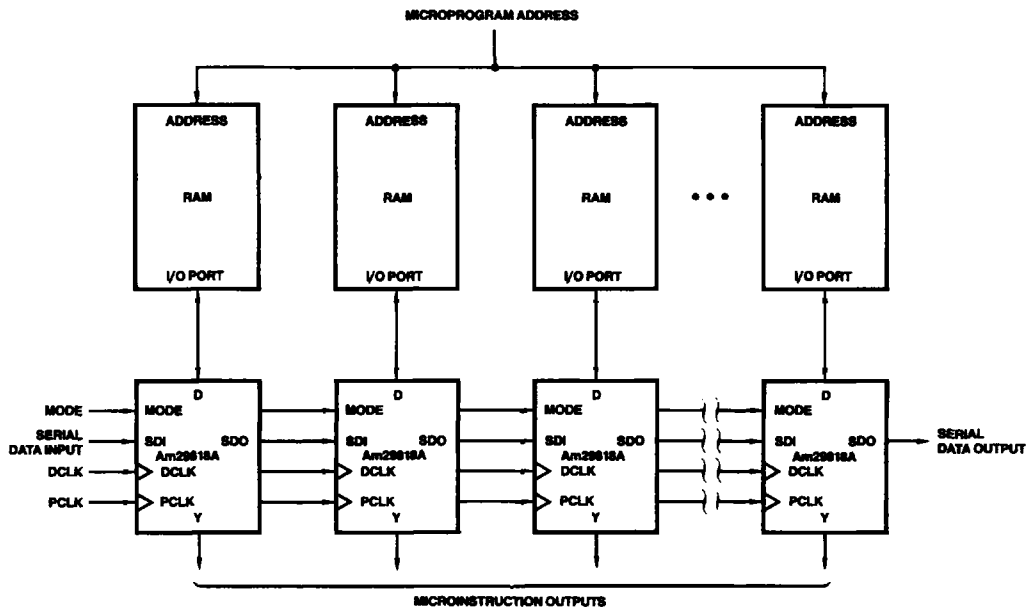


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**Figure 5. Typical System Configuration**

## Use of the Am29818A Pipeline Register in Writable Control Store (WCS) Designs

The Am29818A SSR diagnostics/WCS Pipeline Register was designed specifically to support writable control store designs. In the past, designers of WCS based systems needed to use an excessive amount of support circuitry to implement a WCS. As shown in Figure 7, additional input and output buffers are necessary to provide paths from the parallel input data bus to the memory, and from the instruction register to the output data bus. The input port is necessary to write data to the control store, initializing the micromemory. The output port provides the access to the instruction register, indirectly allowing the RAM to be read. Additionally, access to the instruction register is useful during system debugging and system diagnostics.

The Am29818A supports all of the above operations (and more) without any support circuitry. Figure 6 shows a typical WCS design with the Am29818A. Access to memory is now possible over the serial diagnostics port. The instruction register contents may be read by serially shifting the information out on the diagnostics port. Additionally, the instruction register may be written from the serial port via the shadow register. This simplifies system debug and diagnostics operations considerably.
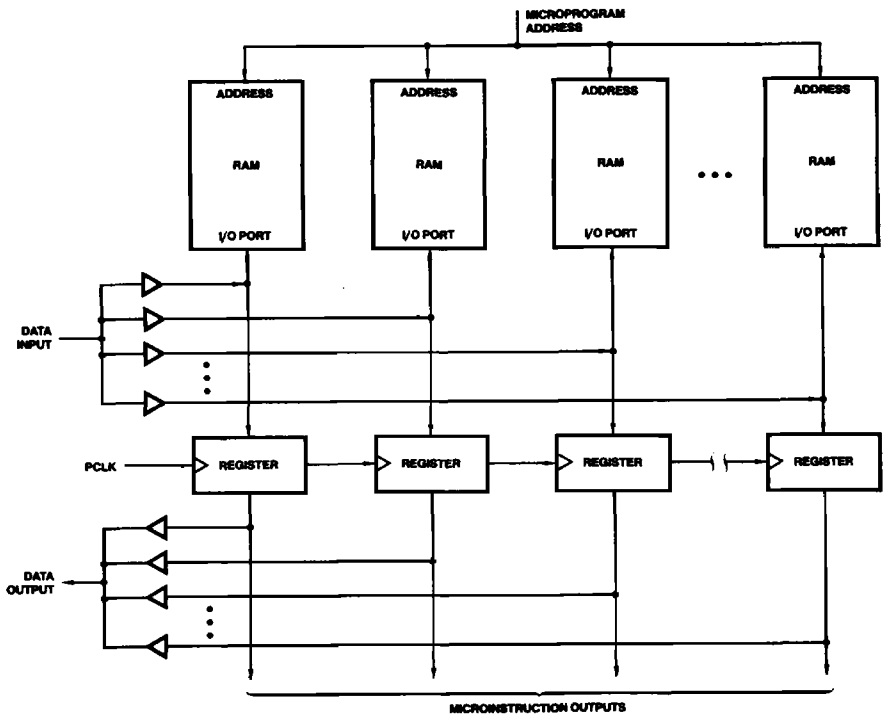
### Conclusion

Serial Shadow Register diagnostics provides the observability and controllability necessary to take any sequential network and turn it into a combinational network. This provides a method for pin-pointing digital system hardware failures in a systematic and well-understood fashion.

Figure 6. Am29818A-Based WCS Application

DF000102



Figure 7. WCS Application without Am29818As

DF000090

## ABSOLUTE MAXIMUM RATINGS

Storage Temperature ......................... −65°C to +150°C
Ambient Temperature with
  Power Applied ............................... −55°C to +125°C
Supply Voltage to Ground Potential
  Continuous .................................... −0.5 V to +7.0 V
DC Voltage Applied to Outputs
  for High Output State ..................... −0.5 V to +5.5 V
DC Input Voltage .............................. −1.5 V to +6.0 V
DC Output Current, into Outputs ....................... 100 mA
DC Input Current ........................... −30 mA to +5.0 mA

*Stresses above those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent device failure. Functionality at or above these limits is not implied. Exposure to absolute maximum ratings for extended periods may affect device reliability.*

## OPERATING RANGES

Commercial (C) Devices
  Temperature ($T_A$) ............................... 0°C to +70°C
  Supply Voltage ($V_{CC}$) ................... +4.5 V to +5.5 V

Military (M) and Extended Commercial (E) Devices
  Temperature ($T_C$) ............................ −55 to +125°C
  Supply Voltage ($V_{CC}$) ................... +4.5 V to +5.5 V

*Operating ranges define those limits between which the functionality of the device is guaranteed.*

## DC CHARACTERISTICS over operating range unless otherwise specified (for APL Products, Group A, Subgroups 1, 2, 3 are tested unless otherwise noted)

| Parameter Symbol | Parameter Description | Test Conditions (Note 1) | | | Min. | Max. | Units |
|---|---|---|---|---|---|---|---|
| $V_{OH}$ | Output HIGH Voltage | $V_{CC}$ = 4.5 V $V_{IN}$ = $V_{IH}$ or $V_{IL}$ | $Y_0 - Y_7$: $I_{OH}$ = −6 mA $D_0 - D_7$, SDO: $I_{OH}$ = −1 mA | | 2.4 | | Volts |
| $V_{OL}$ | Output LOW Voltage | $V_{CC}$ = 4.5 V $V_{IN}$ = $V_{IH}$ or $V_{IL}$ | $Y_0 - Y_7$ | $I_{OL}$ = 24 mA | | 0.5 | V |
| | | | $D_0 - D_7$, SDO | COM'L $I_{OL}$ = 8 mA | | 0.5 | |
| | | | | MIL $I_{OL}$ = 4 mA | | 0.5 | |
| $V_{IH}$ | Input HIGH Voltage | Guaranteed Input Logical HIGH Voltage for all Inputs (Note 1) | | | 2.0 | | |
| $V_{IL}$ | Input LOW Voltage | Guaranteed Input Logical LOW Voltage for all Inputs (Note 1) | | | | 0.8 | Volts |
| $V_I$ | Input Clamp Voltage | $V_{CC}$ = 4.5 V, $I_{IN}$ = −18 mA | | | | −1.2 | Volts |
| $I_{IL}$ | Input LOW Current | $V_{CC}$ = 5.5 V, $V_{IN}$ = 0.5 V | | | | −0.25 | mA |
| $I_{IH}$ | Input HIGH Current | $V_{CC}$ = 5.5 V, $V_{IN}$ = 2.4 V | | | | 50 | $\mu A$ |
| $I_I$ | Input HIGH Current | $V_{CC}$ = 5.5 V, $V_{IN}$ = 5.5 V | | | | 1.0 | mA |
| $I_O$ | Off-State Current (High Impedance) | $V_{CC}$ = 5.5 V | $V_O$ = 0.5 V | | | −250 | $\mu A$ |
| | | | $V_O$ = 2.4 V | | | 100 | |
| $I_{SC}$ | Output Short-Circuit Current | $V_{CC}$ = 5.5 V (Note 2) | $Y_0 - Y_7$ | | −30 | −100 | mA |
| | | | $D_0 - D_7$, SDO | | −15 | −50 | |
| $I_{OFF}$ | Bus Leakage | $V_{CC}$ = 0 V, $V_{OUT}$ = 2.9 V | | | | 100 | $\mu A$ |
| $I_{CC}$ | Power Supply Current | $V_{CC}$ = 5.5 V | Outputs Hi-Z | | | 145 | mA |

Notes: 1. Input thresholds are tested during DC parameter testing, and may be tested in combination with other DC parameters.
2. Not more than one output shorted at a time. Duration of the short-circuit test should not exceed one second.

## SWITCHING CHARACTERISTICS

| Parameter Symbol | Paramter Description | Test Conditions | COMMERCIAL | | MILITARY | | Units |
|---|---|---|---|---|---|---|---|
| | | | Min. | Max. | Min. | Max. | |
| $t_{PLH}$ and $t_{PHL}$ | PCLK→$Y_x$ | | | 9 | | 12 | ns |
| | MODE→SDO | | | 16 | | 18 | ns |
| | SDI→SDO | | | 15 | | 18 | ns |
| | DCLK→SDO | | | 25 | | 30 | ns |
| $t_S$ | $D_x$→PCLK | | 4 | | 6 | | ns |
| | MODE→PCLK | | 15 | | 15 | | ns |
| | $Y_x$→DCLK | | 5 | | 5 | | ns |
| | MODE→DCLK | | 12 | | 12 | | ns |
| | SDI→DCLK | | 10 | | 12 | | ns |
| | DCLK→PCLK | | 15 | | 15 | | ns |
| | DCLK→DCLK | | 40 | | 45 | | ns |
| $t_H$ | $D_x$→PCLK | See Test Output Load Conditions Below $C_L$ = 50 pF | 2 | | 2 | | ns |
| | MODE→PCLK | | 0 | | 0 | | ns |
| | $Y_x$→DCLK | | 5 | | 5 | | ns |
| | MODE→DCLK | | 2 | | 5 | | ns |
| | SDI→DCLK | | 0 | | 0 | | ns |
| $t_{LZ}$ | $\overline{OEY}$→$Y_x$ | | | 15 | | 20 | ns |
| | DCLK→$D_x$ | | | 45 | | 45 | ns |
| $t_{HZ}$ | $\overline{OEY}$→$Y_x$ | | | 25 | | 30 | ns |
| | DCLK→$D_x$ | | | 80 | | 90 | ns |
| $t_{ZL}$ | $\overline{OEY}$→$Y_x$ | | | 15 | | 20 | ns |
| | DCLK→$D_x$ | | | 25 | | 35 | ns |
| $t_{ZH}$ | $\overline{OEY}$→$Y_x$ | | | 15 | | 20 | ns |
| | DCLK→$D_x$ | | | 25 | | 30 | ns |
| $t_{PW}$ | PCLK (HIGH and LOW) | | 10 | | 15 | | ns |
| | DCLK (HIGH and LOW) | | 15 | | 25 | | ns |

## SWITCHING TEST CIRCUITS
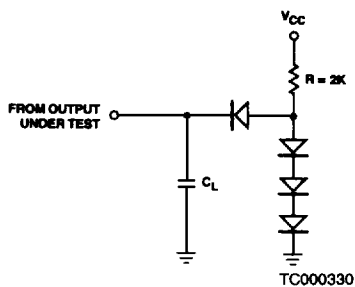


SDO Output
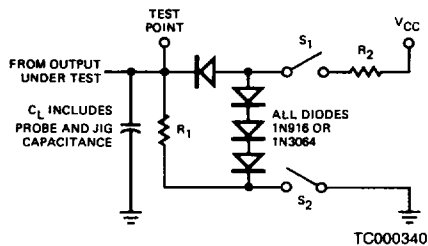


Three-State Outputs

| Pin | $R_1$ | $R_2$ |
|---|---|---|
| $Y_0$ – $Y_7$ | 1K | 280 |
| $D_{0-7}$ | 5K | 2K |