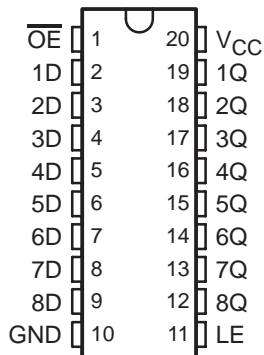


# SN74LV573AT OCTAL TRANSPARENT D-TYPE LATCH WITH 3-STATE OUTPUTS

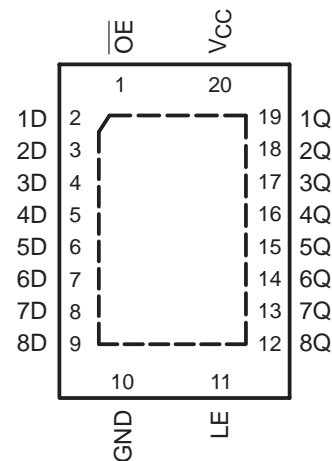
SCES574B – JUNE 2004 – REVISED JANUARY 2005

- Inputs Are TTL-Voltage Compatible
- 4.5-V to 5.5-V  $V_{CC}$  Operation
- Typical  $t_{pd} = 5.1$  ns at 5 V
- Typical  $V_{OLP}$  (Output Ground Bounce)  $<0.8$  V at  $V_{CC} = 5$  V,  $T_A = 25^\circ\text{C}$
- Typical  $V_{OHV}$  (Output  $V_{OH}$  Undershoot)  $>2.3$  V at  $V_{CC} = 5$  V,  $T_A = 25^\circ\text{C}$
- Supports Mixed-Mode Voltage Operation on All Ports
- $I_{off}$  Supports Partial-Power-Down Mode Operation
- Latch-Up Performance Exceeds 250 mA Per JESD 17
- ESD Protection Exceeds JESD 22
  - 2000-V Human-Body Model (A114-A)
  - 200-V Machine Model (A115-A)
  - 1000-V Charged-Device Model (C101)

DB, DGV, DW, NS, OR PW PACKAGE  
(TOP VIEW)



RGY PACKAGE  
(TOP VIEW)



## description/ordering information

The SN74LV573AT is an octal transparent D-type latch. When the latch-enable (LE) input is high, the Q outputs follow the data (D) inputs. When LE is low, the Q outputs are latched at the logic levels of the D inputs.

## ORDERING INFORMATION

$T_A$	PACKAGE†		ORDERABLE PART NUMBER	TOP-SIDE MARKING
–40°C to 85°C	QFN – RGY	Tape and reel	SN74LV573ATRGYR	LV573AT
	SOIC – DW	Tube	SN74LV573ATDW	LV573AT
		Tape and reel	SN74LV573ATDWR	
	SOP – NS	Tape and reel	SN74LV573ATNSR	74LV573AT
	SSOP – DB	Tape and reel	SN74LV573ATDBR	LV573AT
	TSSOP – PW	Tube	SN74LV573ATPW	LV573AT
		Tape and reel	SN74LV573ATPWR	
	TVSOP – DGV	Tape and reel	SN74LV573ATDGVR	LV573AT

† Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at [www.ti.com/sc/package](http://www.ti.com/sc/package).



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# SN74LV573AT

## OCTAL TRANSPARENT D-TYPE LATCH

### WITH 3-STATE OUTPUTS

SCES574B – JUNE 2004 – REVISED JANUARY 2005

#### description/ordering information (continued)

A buffered output-enable ( $\overline{OE}$ ) input can be used to place the eight outputs in either a normal logic state (high or low) or the high-impedance state. In the high-impedance state, the outputs neither load nor drive the bus lines significantly. The high-impedance state and increased drive provide the capability to drive bus lines without interface or pullup components.

To ensure the high-impedance state during power up or power down,  $\overline{OE}$  shall be tied to  $V_{CC}$  through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

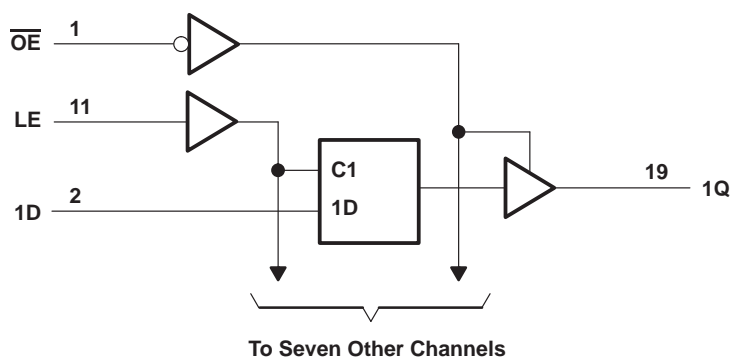
$\overline{OE}$  does not affect the internal operations of the latches. Old data can be retained or new data can be entered while the outputs are in the high-impedance state.

This device is fully specified for partial-power-down applications using  $I_{off}$ . The  $I_{off}$  circuitry disables the outputs, preventing damaging current backflow through the device when it is powered down.

FUNCTION TABLE  
(each latch)

INPUTS			OUTPUT
$\overline{OE}$	LE	D	Q
L	H	H	H
L	H	L	L
L	L	X	$Q_0$
H	X	X	Z

#### logic diagram (positive logic)



# SN74LV573AT OCTAL TRANSPARENT D-TYPE LATCH WITH 3-STATE OUTPUTS

SCES574B – JUNE 2004 – REVISED JANUARY 2005

## absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, $V_{CC}$ .....	–0.5 V to 7 V
Input voltage range, $V_I$ (see Note 1) .....	–0.5 V to 7 V
Voltage range applied to any output in the high-impedance or power-off state, $V_O$ (see Note 1) .....	–0.5 V to 7 V
Output voltage range applied in the high or low state, $V_O$ (see Notes 1 and 2) .....	–0.5 V to $V_{CC} + 0.5$ V
Input clamp current, $I_{IK}$ ( $V_I < 0$ ) .....	–20 mA
Output clamp current, $I_{OK}$ ( $V_O < 0$ ) .....	–50 mA
Continuous output current, $I_O$ ( $V_O = 0$ to $V_{CC}$ ) .....	±35 mA
Continuous current through $V_{CC}$ or GND .....	±70 mA
Package thermal impedance, $\theta_{JA}$ (see Note 3): DB package .....	70°C/W
(see Note 3): DGV package .....	92°C/W
(see Note 3): DW package .....	58°C/W
(see Note 3): NS package .....	60°C/W
(see Note 3): PW package .....	83°C/W
(see Note 4): RGY package .....	37°C/W
Storage temperature range, $T_{stg}$ .....	–65°C to 150°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

- NOTES: 1. The input and output negative-voltage ratings may be exceeded if the input and output current ratings are observed.  
 2. This value is limited to 5.5 V maximum.  
 3. The package thermal impedance is calculated in accordance with JESD 51-7.  
 4. The package thermal impedance is calculated in accordance with JESD 51-5.

## recommended operating conditions (see Note 5)

		MIN	MAX	UNIT
$V_{CC}$	Supply voltage	4.5	5.5	V
$V_{IH}$	High-level input voltage	$V_{CC} = 4.5$ V to 5.5 V		V
$V_{IL}$	Low-level input voltage	$V_{CC} = 4.5$ V to 5.5 V		V
$V_I$	Input voltage	0	5.5	V
$V_O$	Output voltage	High or low state	0	$V_{CC}$
		3-state	0	5.5
$I_{OH}$	High-level output current	$V_{CC} = 4.5$ V to 5.5 V		–16 mA
$I_{OL}$	Low-level output current	$V_{CC} = 4.5$ V to 5.5 V		16 mA
$\Delta t/\Delta v$	Input transition rise or fall rate	$V_{CC} = 4.5$ V to 5.5 V		20 ns/V
$T_A$	Operating free-air temperature	–40	85	°C

NOTE 5: All unused inputs of the device must be held at  $V_{CC}$  or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.



**SN74LV573AT**  
**OCTAL TRANSPARENT D-TYPE LATCH**  
**WITH 3-STATE OUTPUTS**

SCES574B – JUNE 2004 – REVISED JANUARY 2005

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	V <sub>CC</sub>	T <sub>A</sub> = 25°C			T <sub>A</sub> = -40°C TO 85°C		UNIT
			MIN	TYP	MAX	MIN	MAX	
V <sub>OH</sub>	I <sub>OH</sub> = -50 μA	4.5 V	4.4	4.5		4.4		V
	I <sub>OH</sub> = -16 mA	4.5 V	3.8			3.8		
V <sub>OL</sub>	I <sub>OL</sub> = 50 μA	4.5 V		0	0.1		0.1	V
	I <sub>OL</sub> = 16 mA	4.5 V			0.55		0.55	
I <sub>I</sub>	V <sub>I</sub> = 5.5 V or GND	0 to 5.5 V			±0.1		±1	μA
I <sub>OZ</sub>	V <sub>O</sub> = V <sub>CC</sub> or GND	5.5 V			±0.25		±2.5	μA
I <sub>CC</sub>	V <sub>I</sub> = V <sub>CC</sub> or GND, I <sub>O</sub> = 0	5.5 V			2		20	μA
ΔI <sub>CC</sub> <sup>†</sup>	One input at 3.4 V, Other inputs at V <sub>CC</sub> or GND	5.5 V			1.35		1.5	mA
I <sub>off</sub>	V <sub>I</sub> or V <sub>O</sub> = 0 to 5.5 V	0			0.5		5	μA
C <sub>i</sub>	V <sub>I</sub> = V <sub>CC</sub> or GND			4.5				pF

<sup>†</sup> This is the increase in supply current for each input at one of the specified TTL voltage levels, rather than 0 V or V<sub>CC</sub>.

timing requirements over recommended operating free-air temperature range, V<sub>CC</sub> = 5 V ± 0.5 V (unless otherwise noted) (see Figure 1)

		T <sub>A</sub> = 25°C		T <sub>A</sub> = -40°C TO 85°C		UNIT
		MIN	MAX	MIN	MAX	
t <sub>w</sub>	Pulse duration, LE high	6.5		8.5		ns
t <sub>su</sub>	Setup time, data before LE↓	1.5		1.5		ns
t <sub>h</sub>	Hold time, data after LE↓	3.5		3.5		ns



# SN74LV573AT

## OCTAL TRANSPARENT D-TYPE LATCH WITH 3-STATE OUTPUTS

SCES574B – JUNE 2004 – REVISED JANUARY 2005

switching characteristics over recommended operating free-air temperature range,  
 $V_{CC} = 5\text{ V} \pm 0.5\text{ V}$  (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	LOAD CAPACITANCE	$T_A = 25^\circ\text{C}$			$T_A = -40^\circ\text{C}$ TO $85^\circ\text{C}$		UNIT
				MIN	TYP	MAX	MIN	MAX	
$t_{PLH}$	D	Q	$C_L = 15\text{ pF}$	2.6	5.1	8.5	1	9.5	ns
$t_{PHL}$				3	5.1	8.5	1	9.5	
$t_{PLH}$	LE	Q	$C_L = 15\text{ pF}$	3	7.7	12.3	1	14.5	ns
$t_{PHL}$				3.5	7.7	12.3	1	14.5	
$t_{PZH}$	$\overline{OE}$	Q	$C_L = 15\text{ pF}$	3	6.3	10.9	1	12.5	ns
$t_{PZL}$				3.3	6.3	10.9	1	12.5	
$t_{PHZ}$	$\overline{OE}$	Q	$C_L = 15\text{ pF}$	2.8	5.5	8	1	11	ns
$t_{PLZ}$				1.6	5.4	8	1	9.5	
$t_{PLH}$	D	Q	$C_L = 50\text{ pF}$	3.7	5.9	9.5	1	10.5	ns
$t_{PHL}$				5.5	5.9	9.5	1	10.5	
$t_{PLH}$	LE	Q	$C_L = 50\text{ pF}$	4.3	8.5	13.3	1	14.5	ns
$t_{PHL}$				5.9	8.5	13.3	1	14.5	
$t_{PZH}$	$\overline{OE}$	Q	$C_L = 50\text{ pF}$	4.5	7.1	11.9	1	13.5	ns
$t_{PZL}$				5.4	7.1	11.9	1	13.5	
$t_{PHZ}$	$\overline{OE}$	Q	$C_L = 50\text{ pF}$	3.3	8.8	11.2	1	12	ns
$t_{PLZ}$				2.6	8.8	11.2	1	12	
$t_{sk(o)}$			$C_L = 50\text{ pF}$			1.5		1.5	ns

noise characteristics,  $V_{CC} = 5\text{ V}$ ,  $C_L = 50\text{ pF}$  (see Note 6)

PARAMETER		$T_A = 25^\circ\text{C}$			UNIT
		MIN	TYP	MAX	
$V_{OL(P)}$	Quiet output, maximum dynamic $V_{OL}$		1.1	1.5	V
$V_{OL(V)}$	Quiet output, minimum dynamic $V_{OL}$	-1.1		-1.5	V
$V_{OH(V)}$	Quiet output, minimum dynamic $V_{OH}$		4		V
$V_{IH(D)}$	High-level dynamic input voltage	2			V
$V_{IL(D)}$	Low-level dynamic input voltage			0.8	V

NOTE 6: Characteristics are for surface-mount packages only.

operating characteristics,  $V_{CC} = 5\text{ V}$ ,  $T_A = 25^\circ\text{C}$

PARAMETER		TEST CONDITIONS	TYP	UNIT
$C_{pd}$	Power dissipation capacitance	Outputs enabled $C_L = 50\text{ pF}$ , $f = 10\text{ MHz}$	8	pF

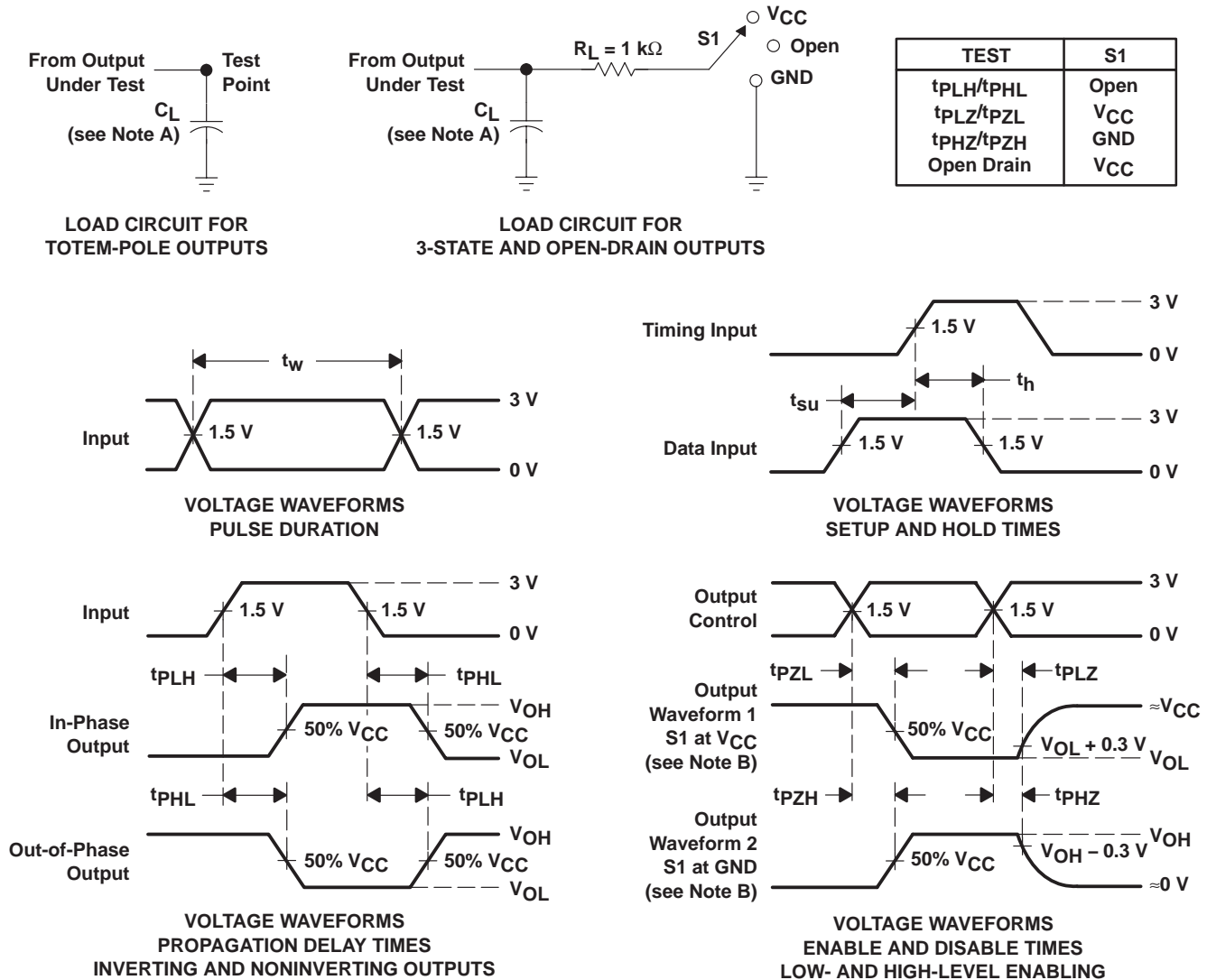
# SN74LV573AT

## OCTAL TRANSPARENT D-TYPE LATCH

### WITH 3-STATE OUTPUTS

SCES574B – JUNE 2004 – REVISED JANUARY 2005

#### PARAMETER MEASUREMENT INFORMATION



- NOTES:
- A.  $C_L$  includes probe and jig capacitance.
  - B. Waveform 1 is for an output with internal conditions such that the output is low, except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high, except when disabled by the output control.
  - C. All input pulses are supplied by generators having the following characteristics:  $PRR \leq 1\text{ MHz}$ ,  $Z_O = 50\ \Omega$ ,  $t_r \leq 3\text{ ns}$ ,  $t_f \leq 3\text{ ns}$ .
  - D. The outputs are measured one at a time, with one input transition per measurement.
  - E.  $t_{PLZ}$  and  $t_{PHZ}$  are the same as  $t_{dis}$ .
  - F.  $t_{PZL}$  and  $t_{PZH}$  are the same as  $t_{en}$ .
  - G.  $t_{PHL}$  and  $t_{PLH}$  are the same as  $t_{pd}$ .
  - H. All parameters and waveforms are not applicable to all devices.

Figure 1. Load Circuits and Voltage Waveforms

DGV (R-PDSO-G\*\*)

PLASTIC SMALL-OUTLINE

24 PINS SHOWN



- NOTES: A. All linear dimensions are in millimeters.  
 B. This drawing is subject to change without notice.  
 C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15 per side.  
 D. Falls within JEDEC: 24/48 Pins – MO-153  
 14/16/20/56 Pins – MO-194

DW (R-PDSO-G20)

PLASTIC SMALL-OUTLINE PACKAGE

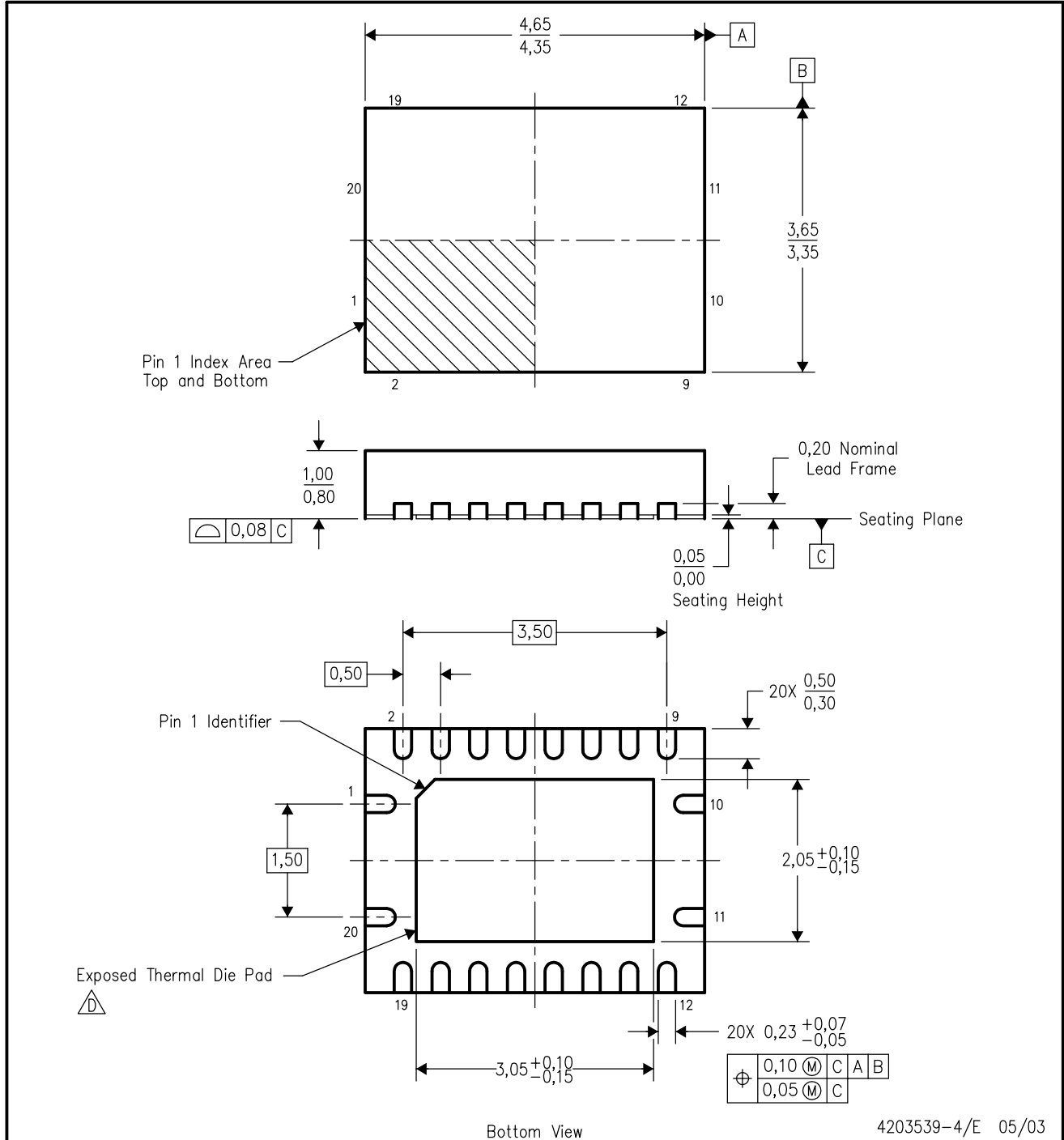


- NOTES:
- A. All linear dimensions are in inches (millimeters).
  - B. This drawing is subject to change without notice.
  - C. Body dimensions do not include mold flash or protrusion not to exceed 0.006 (0,15).
  - D. Falls within JEDEC MS-013 variation AC.



RGY (R-PQFP-N20)

PLASTIC QUAD FLATPACK



- NOTES:
- A. All linear dimensions are in millimeters.
  - B. This drawing is subject to change without notice.
  - C. QFN (Quad Flatpack No-Lead) package configuration.
  - The package thermal performance may be enhanced by bonding the thermal die pad to an external thermal plane. This pad is electrically and thermally connected to the backside of the die and possibly selected ground leads.
  - E. Package complies to JEDEC MO-241 variation BC.

# MECHANICAL DATA

NS (R-PDSO-G\*\*)

PLASTIC SMALL-OUTLINE PACKAGE

14-PINS SHOWN



- NOTES:
- A. All linear dimensions are in millimeters.
  - B. This drawing is subject to change without notice.
  - C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15.

DB (R-PDSO-G\*\*)

PLASTIC SMALL-OUTLINE

28 PINS SHOWN



- NOTES: A. All linear dimensions are in millimeters.  
 B. This drawing is subject to change without notice.  
 C. Body dimensions do not include mold flash or protrusion not to exceed 0,15.  
 D. Falls within JEDEC MO-150

PW (R-PDSO-G\*\*)

PLASTIC SMALL-OUTLINE PACKAGE

14 PINS SHOWN



4040064/F 01/97

- NOTES: A. All linear dimensions are in millimeters.  
 B. This drawing is subject to change without notice.  
 C. Body dimensions do not include mold flash or protrusion not to exceed 0,15.  
 D. Falls within JEDEC MO-153

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