Rochester Electronics

Datasheet

Rochester Electronics Manufactured Components

Rochester branded components are manufactured using either die/wafers purchased from the original suppliers or Rochester wafers recreated from the original IP. All recreations are done with the approval of the OCM.

Parts are tested using original factory test programs or Rochester developed test solutions to guarantee product meets or exceed the OCM data sheet.

Quality Overview

- ISO-9001
- AS9120 certification
- Qualified Manufacturers List (QML) MIL-PRF-35835
    - Class Q Military
    - Class V Space Level
- Qualified Suppliers List of Distributors (QSLD)

- Rochester is a critical supplier to DLA and meets all industry and DLA standards.

Rochester Electronics, LLC is committed to supplying products that satisfy customer expectations for quality and are equal to those originally supplied by industry manufacturers.

The original manufacturer's datasheet accompanying this document reflects the performance and specifications of the Rochester manufactured version of this device. Rochester Electronics guarantees the performance of its semiconductor products to the original OEM specifications. 'Typical' values are for reference purposes only. Certain minimum or maximum ratings may be based on product characterization, design, simulation, or sample testing.

Am29C841/Am29C843
Am29C941/Am29C943

High-Performance CMOS Bus Interface Latches

DISTINCTIVE CHARACTERISTICS

- High-speed parallel latches
  - D-Y propagation delay = 7 ns typical
- Low standby power
- I_{OL} = 24 mA, Commercial and Military
- JEDEC FCT-compatible specs
- Extra-wide (9- and 10-bit) data paths
- Am29C900 DIP pinout option reduces lead inductance on V_{CC} and GND pins

GENERAL DESCRIPTION

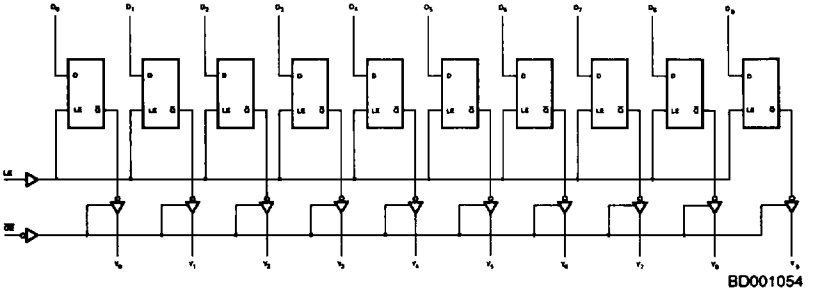
The Am29C841 and Am29C843 CMOS Bus Interface Latches are designed to eliminate the extra devices required to buffer stand alone latches and to provide extra data width for wider address/data paths or buses carrying parity. The Am29C800 latches are produced with AMD's exclusive CS-11 CMOS process, and feature typical propagation delays of 7 ns, as well as an output current drive of 24 mA.

The Am29C841 is a buffered, 10-bit version of the popular '373 function. The Am29C843 is a 9-bit buffered latch with Preset ($\overline{PRE}$) and Clear ($\overline{CLR}$) — ideal for parity bus interfacing in high-performance microprogrammed systems.

The Am29C841 and Am29C843 are available in the standard package options: DIPs, PLCCs, LCCs, SOICs, and Flatpacks. In addition, a DIP pinout option, featuring center V_{CC} and GND pins, reduces the lead inductance of the V_{CC} and GND pins. The ordering part numbers for CMOS latches with this pinout are the Am29C941 and Am29C943; their pinouts are shown later in this data sheet.

BLOCK DIAGRAMS

Am29C841



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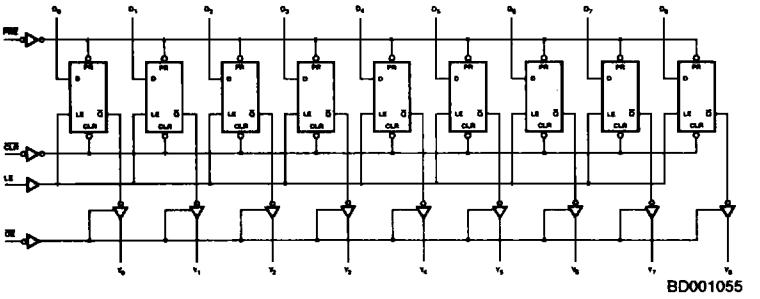
Am29C843



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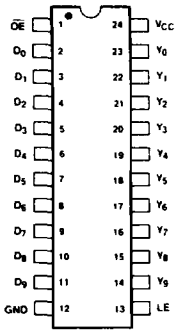
Publication # 07137 | Rev. C | Amendment /0
Issue Date: January 1988

CONNECTION DIAGRAMS
Top View

Am29C841

DIPs*



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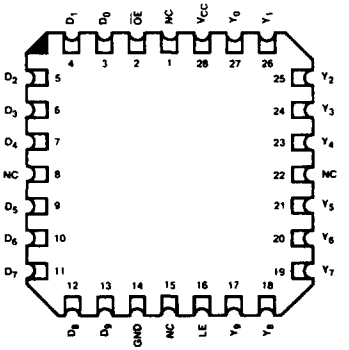
LCC**



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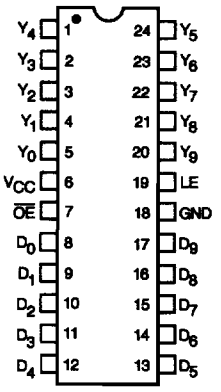
Am29C941

DIPs



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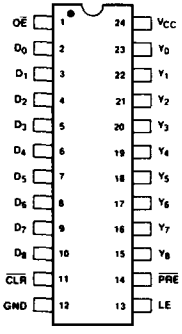
Am29C843

DIPs*



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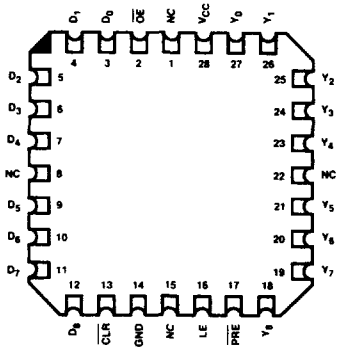
LCC**



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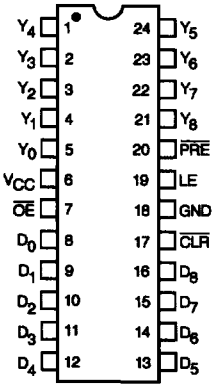
*Also available in 24-Pin Flatpack and Small Outline package; pinout identical to DIPs.

**Also available in 28-Pin PLCC; pinout identical to LCC.

Am29C943

DIPs



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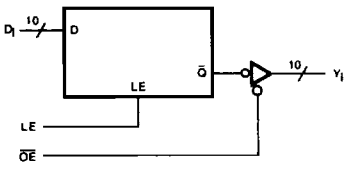
LOGIC SYMBOLS

Am29C841



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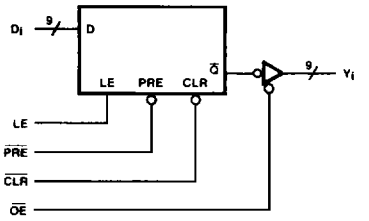
Am29C843



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FUNCTION TABLES

Am29C841

Inputs			Internal	Outputs	
$\overline{OE}$	LE	D_I	$\overline{O}_I$	Y_I	Function
H	X	X	X	Z	Hi-Z
H	H	L	H	Z	Hi-Z
H	H	H	L	Z	Hi-Z
H	L	X	NC	Z	Latched (Hi-Z)
L	H	L	H	L	Transparent
L	H	H	L	H	Transparent
L	L	X	NC	NC	Latched

Am29C843

Inputs					Internal	Outputs	
$\overline{CLR}$	$\overline{PRE}$	$\overline{OE}$	LE	D_I	$\overline{O}_I$	Y_I	Function
H	H	H	X	X	X	Z	Hi-Z
H	H	H	H	H	L	Z	Hi-Z
H	H	H	H	L	H	Z	Hi-Z
H	H	H	L	X	NC	Z	Latched (Hi-Z)
H	H	L	H	H	L	H	Transparent
H	H	L	H	L	H	L	Transparent
H	H	L	L	X	NC	NC	Latched
H	L	L	X	X	L	H	Preset
L	H	L	X	X	H	L	Clear
L	L	L	X	X	H	H	Preset
L	H	H	L	X	L	Z	Latched (Hi-Z)
H	L	H	L	X	L	Z	Latched (Hi-Z)

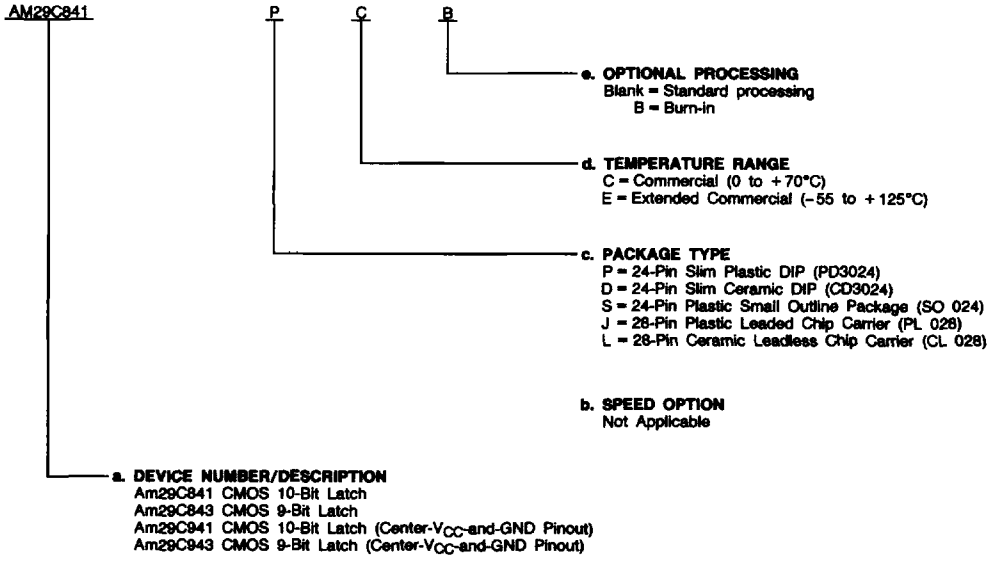
H = HIGH
L = LOW
X = Don't Care

NC = No Change
Z = High Impedance

ORDERING INFORMATION
Standard Products

AMD products are available in several packages and operating ranges. The order number (Valid Combination) is formed by a combination of:

a. Device Number
b. Speed Option (if applicable)
c. Package Type
d. Temperature Range
e. Optional Processing



Valid Combinations	
AM29C841	PC, PCB, DC, DCB, DE, SC, JC, LC
AM29C843	
AM29C941	PC, PCB, DC, DCB, DE
AM29C943	

Valid Combinations

Valid Combinations list configurations planned to be supported in volume for this device. Consult the local AMD sales office to confirm availability of specific valid combinations, to check on newly released valid combinations, and to obtain additional data on AMD's standard military grade products.

ORDERING INFORMATION (Cont'd.)

APL Products

AMD products for Aerospace and Defense applications are available in several packages and operating ranges. APL (Approved Products List) products are fully compliant with MIL-STD-883C requirements. The order number (Valid Combination) for APL products is formed by a combination of: **a. Device Number**
b. Speed Option (if applicable)
c. Device Class
d. Package Type
e. Lead Finish

AM29C841 /B L A

e. LEAD FINISH
A = Hot Solder DIP

d. PACKAGE TYPE
L = 24-Pin Slim Ceramic DIP (CD3024)
K = 24-Pin Rectangular Medium Ceramic Flatpack (CFM024)
3 = 28-Pin Ceramic Leadless Chip Carrier (CL 028)

c. DEVICE CLASS
/B = Class B

b. SPEED OPTION
Not Applicable

a. DEVICE NUMBER/DESCRIPTION
Am29C841 CMOS 10-Bit Latch
Am29C843 CMOS 9-Bit Latch
Am29C941 CMOS 10-Bit Latch (Center-V_{CC}-and-GND Pinout)
Am29C943 CMOS 9-Bit Latch (Center-V_{CC}-and-GND Pinout)

Valid Combinations	
AM29C841	/BLA, /BKA, /B3A
AM29C843	
AM29C941	/BLA
AM29C943	

Valid Combinations

Valid Combinations list configurations planned to be supported in volume for this device. Consult the local AMD sales office to confirm availability of specific valid combinations or to check for newly released valid combinations.

Group A Tests

Group A tests consist of Subgroups 1, 2, 3, 7, 8, 9, 10, 11.

PIN DESCRIPTION

Am29C841/Am29C843

D_i Data Inputs (Input)
D_i are the latch data inputs.

Y_i Data Outputs (Output)
Y_i are the three state data outputs.

LE Latch Enable (Input, Active HIGH)
The latches are transparent when LE is HIGH. Input data is latched on a HIGH-to-LOW transition.

$\overline{OE}$ Output Enable (Input, Active LOW)
When $\overline{OE}$ is LOW, the latch data is passed to the Y_i outputs. When $\overline{OE}$ is HIGH, the Y_i outputs are in the high impedance state.

Am29C843 Only

$\overline{PRE}$ Preset (Input, Active LOW)
When $\overline{PRE}$ is LOW, the outputs are HIGH if $\overline{OE}$ is LOW. $\overline{PRE}$ overrides the $\overline{CLR}$ pin. $\overline{PRE}$ will set the latch independent of the state of $\overline{OE}$.

$\overline{CLR}$ Clear (Input, Active LOW)
When $\overline{CLR}$ is LOW, the internal latch is cleared. When $\overline{CLR}$ is LOW, the outputs are LOW if $\overline{OE}$ is LOW and $\overline{PRE}$ is HIGH. When $\overline{CLR}$ is HIGH, data can be entered into the latch.

ABSOLUTE MAXIMUM RATINGS

Storage Temperature ..... −65 to +150°C
Supply Voltage to Ground Potential
Continuous ..... −0.5 V to +7.0 V
DC Output Voltage ..... −0.5 V to V_{CC} + 0.5 V
DC Input Voltage ..... −0.5 V to +V_{CC} + 0.5 V
DC Output Diode Current: Into Output ..... +50 mA
Out of Output ..... −50 mA
DC Input Diode Current: Into Input ..... +20 mA
Out of Input ..... −20 mA
DC Output Current per Pin: I_{SINK} ..... +48 mA (2 x I_{OL})
I_{SOURCE} ..... −30 mA (2 x I_{OH})
Total DC Ground Current .(n x I_{OL} + m x I_{CCT}) mA (Note 1)
Total DC V_{CC} Current .... (n x I_{OH} + m x I_{CCT}) mA (Note 1)

Stresses above those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent device failure. Functionality at or above these limits is not implied. Exposure to absolute maximum ratings for extended periods may affect device reliability.

OPERATING RANGES

Commercial (C) Devices
Temperature (T_A) ..... 0 to +70°C
Supply Voltage (V_{CC}) ..... +4.5 V to +5.5 V

Military (M) and Extended Commercial (E) Devices
Temperature (T_A) ..... −55 to +125°C
Supply Voltage (V_{CC}) ..... +4.5 V to +5.5 V

Operating ranges define those limits between which the functionality of the device is guaranteed.

DC CHARACTERISTICS over operating range unless otherwise specified (for APL Products, Group A, Subgroups 1, 2, 3 are tested unless otherwise noted)

Parameter Symbol	Parameter Description	Test Conditions			Min.	Max.	Units
V_{OH}	Output HIGH Voltage	V_{CC} = 4.5 V, V_{IN} = V_{IH} or V_{IL}	I_{OH} = −15 mA		2.4		Volts
V_{OL}	Output LOW Voltage	V_{CC} = 4.5 V, V_{IN} = V_{IH} or V_{IL}	I_{OL} = 24 mA			0.5	Volts
V_{IH}	Input HIGH Voltage	Guaranteed Input Logical HIGH Voltage for All Inputs (Note 2)			2.0		Volts
V_{IL}	Input LOW Voltage	Guaranteed Input Logical LOW Voltage for All Inputs (Note 2)				0.8	Volts
V_I	Input Clamp Voltage	V_{CC} = 4.5 V, I_{IN} = −18 mA				−1.2	Volts
I_{IL}	Input LOW Current	V_{CC} = 5.5 V, V_{IN} = GND				−10	µA
		V_{CC} = 5.5 V, V_{IN} = 0.4 V				−5	
I_{IH}	Input HIGH Current	V_{CC} = 5.5 V, V_{IN} = 2.7 V				5	µA
		V_{CC} = 5.5 V, V_{IN} = 5.5 V				10	
I_{OZH}	Output Off-State Current (High Impedance)	V_{CC} = 5.5 V, V_O = 5.5 V or 2.7 V (Note 3)				+10	µA
I_{OZL}		V_{CC} = 5.5 V, V_O = 0.4 V or GND (Note 3)				−10	µA
I_{SC}	Output Short-Circuit Current	V_{CC} = 5.5 V, V_O = 0 V (Note 4)			−60		mA
I_{CCQ}	Static Supply Current	V_{CC} = 5.5 V, Outputs Open	V_{IN} = V_{CC} or GND	MIL		160	µA
				COM'L		120	
I_{CCT}			V_{IN} = 3.4 V	Data Input		1.5	mA/Bit
				$\overline{OE}$, $\overline{PRE}$, $\overline{CLR}$, LE		3.0	
I_{CCD}†	Dynamic Supply Current	V_{CC} = 5.5 V (Note 5)				275	µA/MHz/Bit

Notes: 1. n = number of outputs, m = number of inputs.
2. Input thresholds are tested in combination with other DC parameters or by correlation.
3. Off-state currents are only tested at worst-case conditions of V_{OUT} = 5.5 V or 0.0 V.
4. Not more than one output shorted at a time. Duration should not exceed 100 milliseconds.
5. Measured at a frequency ≤ 10 MHz with 50% duty cycle.

† Not included in Group A tests.

SWITCHING CHARACTERISTICS over operating range unless otherwise specified (for APL Products, Group A, Subgroups 9, 10, 11 are tested unless otherwise noted)

Parameter Symbol	Parameter Description		Test Conditions*	COMMERCIAL		MILITARY		Units
				Min.	Max.	Min.	Max.	
t_{PLH}	Data (D_i) to Output Y_i (LE = HIGH)		C_L = 50 pF R_1 = 500 Ω R_2 = 500 Ω		11		14	ns
t_{PHL}					11		14	ns
t_S	Data to LE Setup Time			3		3		ns
t_H	Data to LE Hold Time			4		4		ns
t_{PLH}	Latch Enable (LE) to Y_i				12		14	ns
t_{PHL}					12		14	ns
t_{PLH}	Propagation Delay, Preset to Y_i				13		15	ns
t_{PHL}					13		15	ns
t_{REC}	Preset ($\overline{PRE}$ ↓) to LE Setup Time			4		4		ns
t_{PLH}	Propagation Delay, Clear to Y_i				12		14	ns
t_{PHL}					12		14	ns
t_{REC}	Clear ($\overline{CLR}$ ↓) to LE Setup Time			3		3		ns
t_{PWH}	LE Pulse Width	HIGH		6		9		ns
t_{PWL}	Preset Pulse Width	LOW		8		12		ns
t_{PWL}	Clear Pulse Width	LOW		8		12		ns
t_{ZH}	Output Enable Time $\overline{OE}$ ↑ to Y_i				12		14	ns
t_{ZL}					12		14	ns
t_{HZ}	Output Disable Time $\overline{OE}$ ↓ to Y_i				12		14	ns
t_{LZ}					12		14	ns

*See Test Circuit and Waveforms.