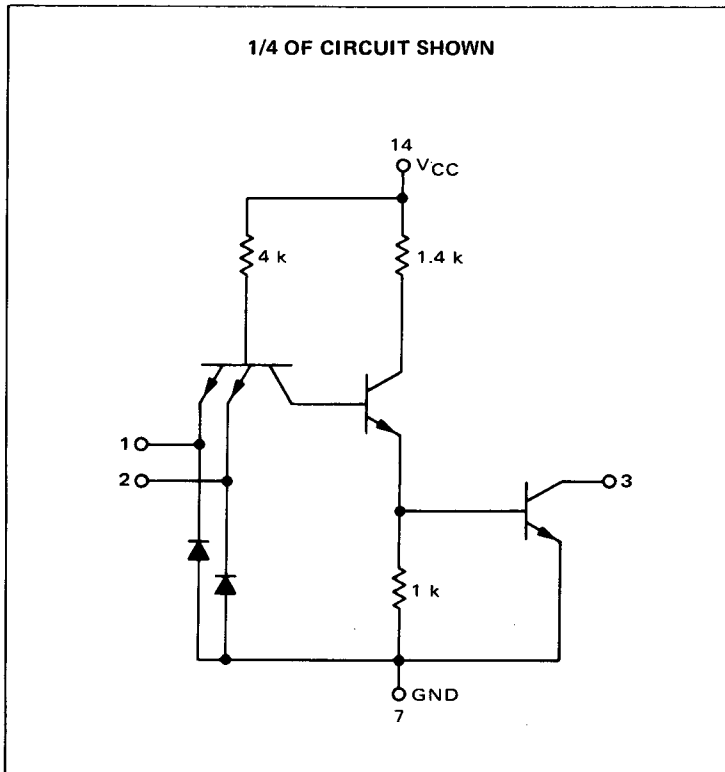
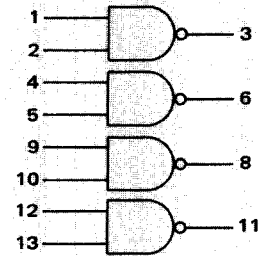




MC5403L*
MC7403P,L*



This device consists of four 2-input NAND gates with no output pullup circuits. It can be used where the Wired-OR function is required, or for driving discrete components.



Positive Logic: $3 = \overline{1 \cdot 2}$
Negative Logic: $3 = \overline{1 + 2}$

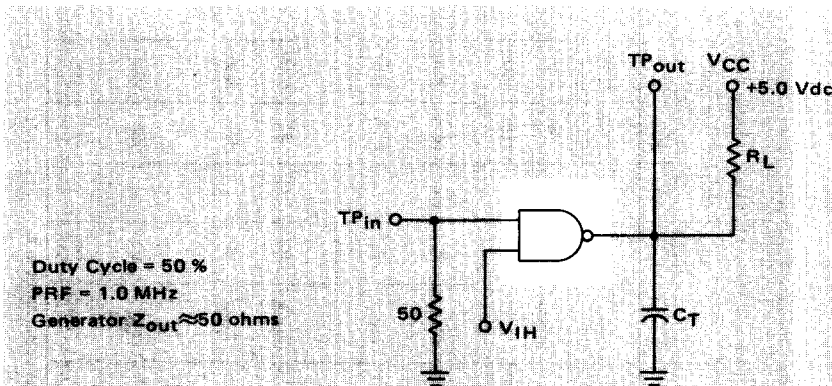
Input Loading Factor = 1
Output Loading Factor = 10

Total Power Dissipation = 40 mW typ/pkg
Propagation Delay Time = 35 ns typ

* L suffix = TO-116 ceramic package (Case 632)
P suffix = TO-116 plastic package (Case 605)
See General Information section for package outline dimensions.

42 *OAIg*
4467 *004467* *not*

VOLTAGE WAVEFORMS AND DEFINITIONS

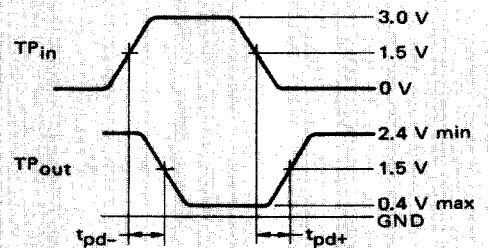


$R_L = 400$ ohms for t_{pd-} test.
 4.0 k ohms for t_{pd+} test.

$C_T = 15$ pF = total parasitic capacitance, which includes probe, wiring, and load capacitances.

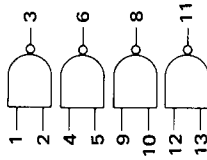
High impedance probes (>1.0 megohm) must be used for tests.

SWITCHING TIME TEST CIRCUIT



ELECTRICAL CHARACTERISTICS

Test procedures are shown for only one gate. The other gates are tested in the same manner. Further, test procedures are shown for only one input of the gate under test. To complete testing, sequence through remaining inputs.



MC5403

MC7403

MC7403 Test Limits
0 to +70°C

MC5403 Test Limits
-55 to +125°C

Pin Under Test

Symbol

Characteristic

Characteristic	Symbol	Pin Under Test	MC5403 Test Limits -55 to +125°C		MC7403 Test Limits 0 to +70°C		TEST CURRENT / VOLTAGE VALUES (All Temperatures)													
			Min	Max	Unit	Min	Max	Unit	Volts											
Input								I_{OL}	V_{IL}	V_{IH}	V_{IHH}	V_{R1}	V_{R2}	V_{th1}	V_{th0}	V_{CEX}	V_{CC}	V_{CCL}	V_{CCH}	
Forward Current	I_F	1	-	-1.6	mAdc	-	-1.6	-	1	-	-	2	-	-	-	-	-	-	-	-
Leakage Current	I_{R1}	1	-	40	μ Adc	-	40	-	-	1	-	-	-	-	-	-	-	-	-	-
	I_{R2}	1	-	1.0	mAdc	-	1.0	-	-	-	1	-	-	-	-	-	-	-	-	-
	V_{OL}	3	-	0.4	Vdc	-	0.4	-	-	-	-	-	-	1.2	-	-	-	-	-	-
Output Leakage Current	I_{CEX}	3	-	0.25	mAdc	-	0.25	-	-	-	1	-	-	-	-	2	3	-	-	-
Power Requirements (Total Device)	I_{PDH}	14	-	22	mAdc	-	22	-	-	-	-	-	-	-	-	-	-	-	-	14
	I_{PDL}	14	-	8.0	mAdc	-	8.0	-	-	-	-	-	-	-	-	-	-	-	-	14
Switching Parameters	t_{pd-}	1,3	-	15**	ns	-	15**	-	-	-	-	-	-	-	-	-	-	-	-	-
	t_{pd+}	1,3	-	45**	ns	-	45**	-	-	-	-	-	-	-	-	-	-	-	-	-

* Ground inputs to gates not under test.
** Tested only at 25°C.



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