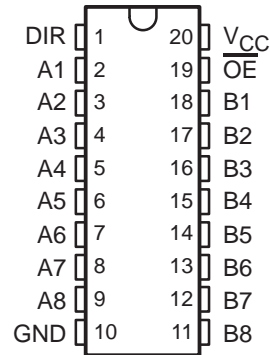


SN54LVT245B, SN74LVT245B 3.3-V ABT OCTAL BUS TRANSCEIVERS WITH 3-STATE OUTPUTS

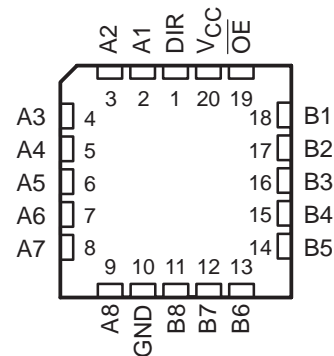
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- State-of-the-Art Advanced BiCMOS Technology (ABT) Design for 3.3-V Operation and Low Static-Power Dissipation
- High-Impedance State During Power Up and Power Down
- Support Mixed-Mode Signal Operation (5-V Input and Output Voltages With 3.3-V V_{CC})
- Support Unregulated Battery Operation Down to 2.7 V
- Power Off Disables Outputs, Permitting Live Insertion
- Typical V_{OLP} (Output Ground Bounce) < 0.8 V at $V_{CC} = 3.3$ V, $T_A = 25^\circ\text{C}$
- Latch-Up Performance Exceeds 500 mA Per JESD 17
- ESD Protection Exceeds 2000 V Per MIL-STD-883, Method 3015; Exceeds 200 V Using Machine Model ($C = 200$ pF, $R = 0$)
- Package Options Include Plastic Small-Outline (DW), Shrink Small-Outline (DB), and Thin Shrink Small-Outline (PW) Packages, Ceramic Chip Carriers (FK), Ceramic Flat (W) Packages, and Ceramic (J) DIPs

SN54LVT245B . . . J OR W PACKAGE
SN74LVT245B . . . DB, DW, OR PW PACKAGE
(TOP VIEW)



SN54LVT245B . . . FK PACKAGE
(TOP VIEW)



description

These octal bus transceivers are designed specifically for low-voltage (3.3-V) V_{CC} operation, but with the capability to provide a TTL interface to a 5-V system environment.

These devices are designed for asynchronous communication between data buses. They transmit data from the A bus to the B bus or from the B bus to the A bus, depending on the logic level at the direction-control (DIR) input. The output-enable (\overline{OE}) input can be used to disable the devices so the buses are effectively isolated.

When V_{CC} is between 0 and 1.5 V, the device is in the high-impedance state during power up or power down. However, to ensure the high-impedance state above 1.5 V, \overline{OE} should be tied to V_{CC} through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

The SN54LVT245B is characterized for operation over the full military temperature range of -55°C to 125°C . The SN74LVT245B is characterized for operation from -40°C to 85°C .



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UNLESS OTHERWISE NOTED this document contains PRODUCTION DATA information current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

 **TEXAS
INSTRUMENTS**

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SN54LVT245B, SN74LVT245B

3.3-V ABT OCTAL BUS TRANSCEIVERS

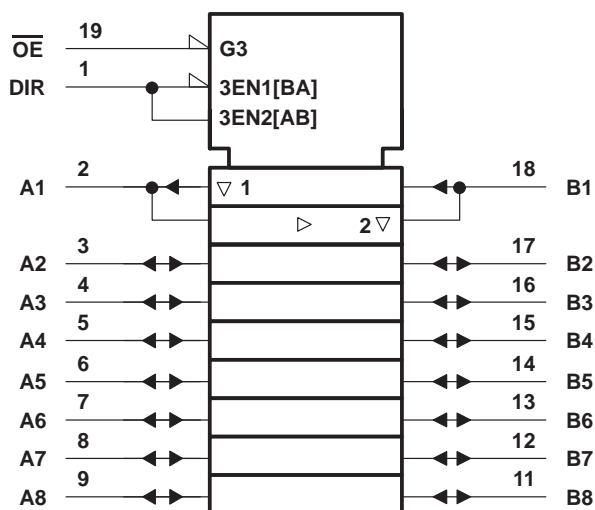
WITH 3-STATE OUTPUTS

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FUNCTION TABLE

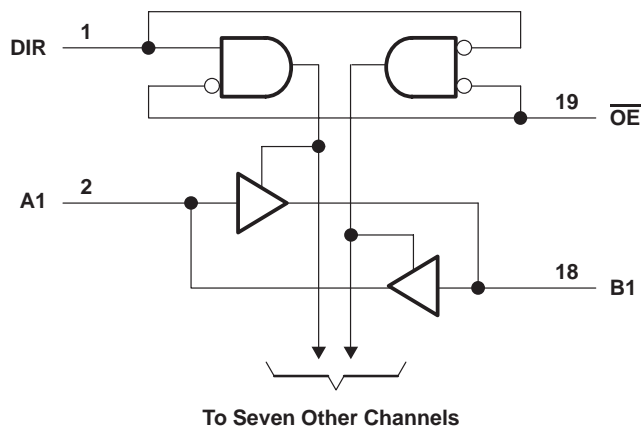
INPUTS		OPERATION
\overline{OE}	DIR	
L	L	B data to A bus
L	H	A data to B bus
H	X	Isolation

logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

logic diagram (positive logic)



SN54LVT245B, SN74LVT245B 3.3-V ABT OCTAL BUS TRANSCEIVERS WITH 3-STATE OUTPUTS

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absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{CC}	–0.5 V to 4.6 V
Input voltage range, V_I (see Note 1)	–0.5 V to 7 V
Voltage range applied to any output in the high or power-off state, V_O (see Note 1)	–0.5 V to 7 V
Current into any output in the low state, I_O : SN54LVT245B	96 mA
SN74LVT245B	128 mA
Current into any output in the high state, I_O (see Note 2): SN54LVT245B	48 mA
SN74LVT245B	64 mA
Input clamp current, I_{IK} ($V_I < 0$)	–50 mA
Output clamp current, I_{OK} ($V_O < 0$)	–50 mA
Package thermal impedance, θ_{JA} (see Note 3): DB package	115°C/W
DW package	97°C/W
PW package	128°C/W
Storage temperature range, T_{stg}	–65°C to 150°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

- NOTES: 1. The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.
 2. This current flows only when the output is in the high state and $V_O > V_{CC}$.
 3. The package thermal impedance is calculated in accordance with JESD 51.

recommended operating conditions (see Note 4)

		SN54LVT245B		SN74LVT245B		UNIT
		MIN	MAX	MIN	MAX	
V_{CC}	Supply voltage	2.7	3.6	2.7	3.6	V
V_{IH}	High-level input voltage	2		2		V
V_{IL}	Low-level input voltage		0.8		0.8	V
V_I	Input voltage		5.5		5.5	V
I_{OH}	High-level output current		–24		–32	mA
I_{OL}	Low-level output current		48		64	mA
$\Delta t/\Delta v$	Input transition rise or fall rate	Outputs enabled		10	10	ns/V
$\Delta t/\Delta V_{CC}$	Power-up ramp rate	200		200		μs/V
T_A	Operating free-air temperature	–55	125	–40	85	°C

NOTE 4: All unused inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

SN54LVT245B, SN74LVT245B

3.3-V ABT OCTAL BUS TRANSCEIVERS

WITH 3-STATE OUTPUTS

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electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS		SN54LVT245B			SN74LVT245B			UNIT
			MIN	TYP†	MAX	MIN	TYP†	MAX	
V _{IK}	V _{CC} = 2.7 V, I _I = -18 mA		-1.2			-1.2			V
V _{OH}	V _{CC} = 2.7 V to 3.6 V, I _{OH} = -100 μA		V _{CC} -0.2			V _{CC} -0.2			V
	V _{CC} = 2.7 V, I _{OH} = -8 mA		2.4			2.4			
	V _{CC} = 3 V	I _{OH} = -24 mA	2			2			
V _{OL}	V _{CC} = 2.7 V	I _{OL} = 100 μA	0.2			0.2			V
		I _{OL} = 24 mA	0.5			0.5			
	V _{CC} = 3 V	I _{OL} = 16 mA	0.4			0.4			
		I _{OL} = 32 mA	0.5			0.5			
		I _{OL} = 48 mA	0.55			0.55			
I _I	Control inputs	V _{CC} = 3.6 V, V _I = V _{CC} or GND	±1			±1			μA
		V _{CC} = 0 or 3.6 V, V _I = 5.5 V	10			10			
	A or B ports‡	V _{CC} = 3.6 V, V _I = 5.5 V	20			20			
		V _{CC} = 3.6 V, V _I = 0	-5			-5			
I _{off}	V _{CC} = 0, V _I or V _O = 0 to 4.5 V				±100			μA	
I _{OZH}	V _{CC} = 3.6 V, V _O = 3 V	5			5			μA	
I _{OZL}	V _{CC} = 3.6 V, V _O = 0.5 V	-5			-5			μA	
I _{OZPU}	V _{CC} = 0 to 1.5 V, V _O = 0.5 V to 3 V, OE = don't care	±100*			±100			μA	
I _{OZPD}	V _{CC} = 1.5 V to 0, V _O = 0.5 V to 3 V, OE = don't care	±100*			±100			μA	
I _{CC}	V _{CC} = 3.6 V, I _O = 0, V _I = V _{CC} or GND	Outputs high	0.19			0.19			mA
		Outputs low	5			5			
		Outputs disabled	0.19			0.19			
ΔI _{CC} §	V _{CC} = 3 V to 3.6 V, One input at V _{CC} - 0.6 V, Other inputs at V _{CC} or GND		0.2			0.2			mA
C _i	V _I = 3 V or 0		4			4			pF
C _{io}	V _O = 3 V or 0		9			9			pF

* On products compliant to MIL-PRF-38535, this parameter is not production tested.

† All typical values are at V_{CC} = 3.3 V, T_A = 25°C.

‡ Unused terminals are at V_{CC} or GND.

§ This is the increase in supply current for each input that is at the specified TTL voltage level rather than V_{CC} or GND.

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switching characteristics over recommended operating free-air temperature range, $C_L = 50$ pF (unless otherwise noted) (see Figure 1)

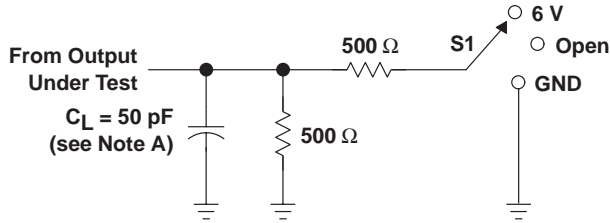
PARAMETER	FROM (INPUT)	TO (OUTPUT)	SN54LVT245B				SN74LVT245B				UNIT	
			$V_{CC} = 3.3\text{ V} \pm 0.3\text{ V}$		$V_{CC} = 2.7\text{ V}$		$V_{CC} = 3.3\text{ V} \pm 0.3\text{ V}$			$V_{CC} = 2.7\text{ V}$		
			MIN	MAX	MIN	MAX	MIN	TYP†	MAX	MIN		MAX
t_{PLH}	A or B	B or A	1.1	3.7		4.2	1.2	2.3	3.5		4	ns
t_{PHL}			1.1	3.7		4.2	1.2	2.1	3.5		4	
t_{PZH}	\overline{OE}	A or B	1.2	5.7		7.4	1.3	3.2	5.5		7.1	ns
t_{PZL}			1.6	5.7		6.8	1.7	3.4	5.5		6.5	
t_{PHZ}	\overline{OE}	A or B	2.1	6.2		6.8	2.2	3.5	5.9		6.5	ns
t_{PLZ}			2.1	5.3		5.5	2.2	3.4	5		5.1	

† All typical values are at $V_{CC} = 3.3\text{ V}$, $T_A = 25^\circ\text{C}$.

SN54LVT245B, SN74LVT245B
3.3-V ABT OCTAL BUS TRANSCEIVERS
WITH 3-STATE OUTPUTS

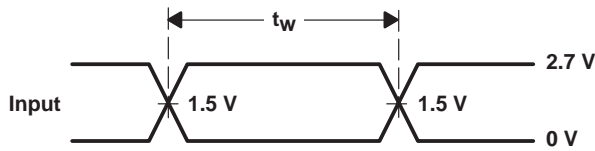
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PARAMETER MEASUREMENT INFORMATION

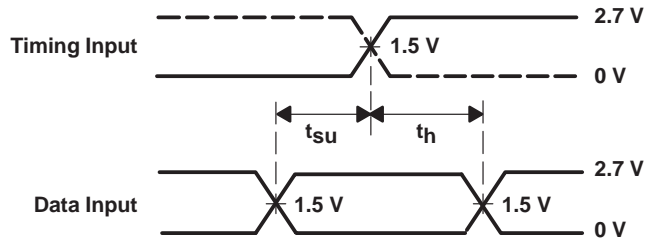


LOAD CIRCUIT

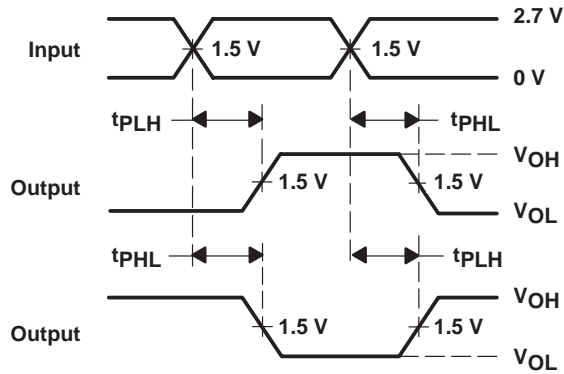
TEST	S1
t_{PLH}/t_{PHL}	Open
t_{PLZ}/t_{PZL}	6 V
t_{PHZ}/t_{PZH}	GND



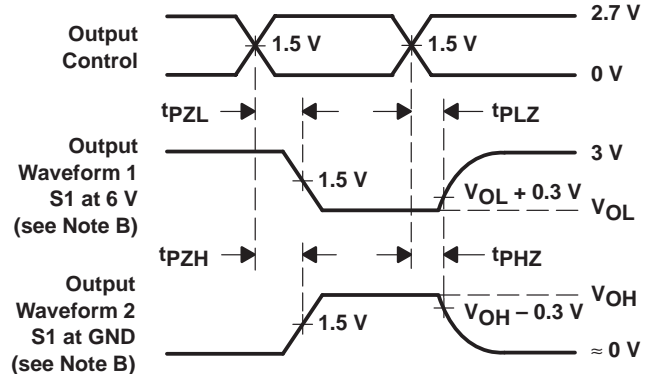
VOLTAGE WAVEFORMS
PULSE DURATION



VOLTAGE WAVEFORMS
SETUP AND HOLD TIMES



VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES
INVERTING AND NONINVERTING OUTPUTS



VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES
LOW- AND HIGH-LEVEL ENABLING

- NOTES: A. C_L includes probe and jig capacitance.
 B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
 C. All input pulses are supplied by generators having the following characteristics: $PRR \leq 10 \text{ MHz}$, $Z_O = 50 \Omega$, $t_r \leq 2.5 \text{ ns}$, $t_f \leq 2.5 \text{ ns}$.
 D. The outputs are measured one at a time with one transition per measurement.

Figure 1. Load Circuit and Voltage Waveforms

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