Signetics

54F175
Flip-Flop

Military Logic Products

Quad D Flip-Flop

Product Specification

FEATURES
- **Four edge-triggered D flip-flops**
- **Buffered common Clock**
- **Buffered, asynchronous Master Reset**
- **True and complementary output**

DESCRIPTION
The 54F175 is a quad, edge-triggered D-type flip-flop with individual D inputs and both Q and $\overline{Q}$ outputs. The common buffered Clock (CP) and Master Reset ($\overline{MR}$) inputs load and reset (clear) all flip-flops simultaneously.

The register is fully edge-triggered. The state of each D input, one setup time before the Low-to-High clock transition, is transferred to the corresponding flip-flop's Q output.

All Q outputs will be forced LOW independently of Clock or Data inputs by a Low voltage level on the $\overline{MR}$ input. The device is useful for applications where both true and complement outputs are required, and the Clock and Master Reset are common to all storage elements.

ORDERING INFORMATION

DESCRIPTION	ORDER CODE
Ceramic DIP	54F175/BEA
Ceramic Flat Pack	54F175/BFA
Ceramic LLCC	54F175/B2A

INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

PINS	DESCRIPTION	54F (U.L.) HIGH/LOW	LOAD VALUE HIGH/LOW
D_0 - D_3	Data inputs	1.0/1.0	20µA/0.6mA
CP	Clock pulse input (active rising edge)	1.0/1.0	20µA/0.6mA
$\overline{MR}$	Master Reset input (active Low)	1.0/1.0	20µA/0.6mA
Q_0 - Q_3	True outputs	50/33	1.0mA/20mA
$\overline{Q}_0$ - $\overline{Q}_3$	Complementary outputs	50/33	1.0mA/20mA

NOTE: One (1.0) FAST Unit Load (U.L.) is defined as: 20µA in the High state and 0.6mA in the Low state.

PIN CONFIGURATION

For LLCC Pin Assignments see JEDEC Standard No. 2

LOGIC SYMBOL

For LLCC Pin Assignments see JEDEC Standard No. 2
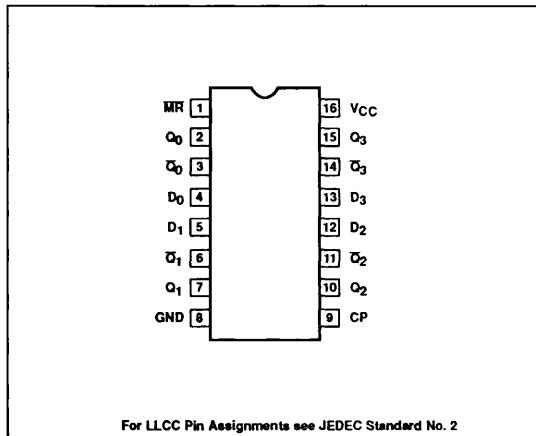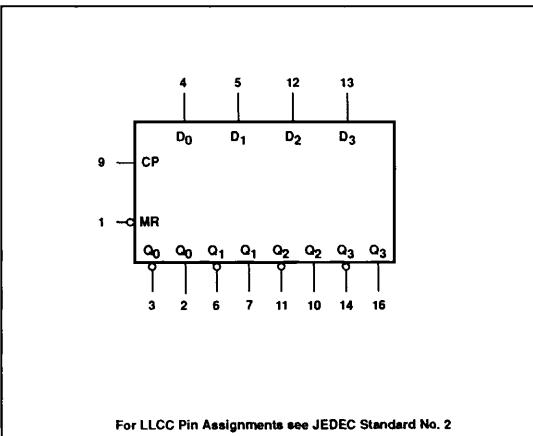
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LOGIC DIAGRAM
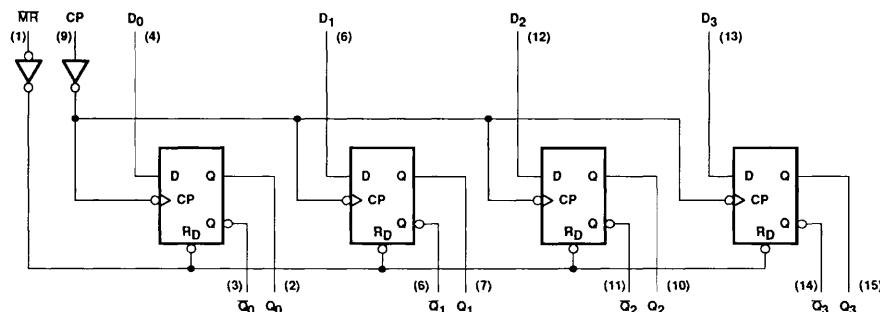
For LLCC pin assignment, see JEDEC Standard No. 2.

FUNCTION TABLE

OPERATING MODE	INPUTS			OUTPUTS	
	$\overline{MR}$	CP	D_n	Q_n	$\overline{Q}_n$
Reset (clear)	L	X	X	L	H
Load "1"	H	↑	h	H	L
Load "0"	H	↑	l	L	H

H = High voltage level steady state.
h = High voltage level one setup time prior to the Low-to-High Clock transition.
L = Low voltage level steady state.
l = Low voltage level one setup time prior to the Low-to-High Clock transition.
X = Don't Care.
↑ = Low-to-High Clock transition.

ABSOLUTE MAXIMUM RATINGS (Operation beyond the limits set forth in this table may impair the useful life of the device. Unless otherwise noted these limits are over the operating free-air temperature range.)

SYMBOL	PARAMETER	RATING	UNIT
V_{CC}	Supply voltage range	-0.5 to +7.0	V
V_I	Input voltage range	-0.5 to +7.0	V
I_I	Input current range	-30 to +5.0	mA
V_O	Voltage applied to output in High output state range	-0.5 to $+V_{CC}$	V
I_O	Current applied to output in Low output state	40	mA
T_{STG}	Storage temperature range	-65 to +150	°C

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	LIMITS			UNIT
		Min	Nom	Max	
V_{CC}	Supply voltage	4.5	5.0	5.5	V
V_{IH}	High-level input voltage	2.0			V
V_{IL}	Low-level input voltage			0.8	V
I_{IK}	Input clamp current			-18	mA
I_{OH}	High-level output current			-1	mA
I_{OL}	Low-level output current			20	mA
T_A	Operating free-air temperature range	-55		+125	°C

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DC ELECTRICAL CHARACTERISTICS (Over recommended operating free-air temperature range unless otherwise noted.)

SYMBOL	PARAMETER	TEST CONDITIONS[1,4]	LIMITS			UNIT
			Min	Typ[2]	Max	
V_{OH}	High-level output voltage	V_{CC} = Min, V_{IL} = Max, I_{OH} = Max, V_{IH} = Min	2.5			V
V_{OL}	Low-level output voltage	V_{CC} = Min, V_{IL} = Max, I_{OL} = Max, V_{IH} = Min		0.35	0.50	V
V_{IK}	Input clamp voltage	V_{CC} = Min, I_I = I_{IK}		-0.73	-1.2	V
I_{IH2}	Input current at maximum input voltage	V_{CC} = Max, V_I = 7.0V			100	μA
I_{IH1}	High-level input current	V_{CC} = Max, V_I = 2.7V		1	20	μA
I_{IL}	Low-level input current	V_{CC} = Max, V_I = 0.5V		-0.4	-0.6	mA
I_{OS}	Short-circuit output current[3]	V_{CC} = Max	-60		-150	mA
I_{CC}	Supply current (total)	V_{CC} = Max, D_n = $\overline{MR}$ ≥ 4.0V, CP = ↑		25	34	mA

AC ELECTRICAL CHARACTERISTICS (When measured in accordance with the procedures outlined in Signetics LOGIC App Note 202, "Testing and Specifying FAST Logic.")

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS					UNIT
			T_A = +25°C V_{CC} = +5.0V C_L = 50pF, R_L = 500Ω			T_A = -55°C to +125°C V_{CC} = +5.0V ± 10% C_L = 50pF, R_L = 500Ω		
			Min	Typ	Max	Min	Max	
f_{MAX}	Maximum Clock frequency	Waveform 1	100	140		80[5]		MHz
t_{PLH} t_{PHL}	Propagation delay CP to Q_n or $\overline{Q}_n$	Waveform 1	4.0 4.0	5.0 6.5	6.5 8.5	3.5 4.0	8.5 10.5	ns ns
t_{PHL}	Propagation delay $\overline{MR}$ to Q_n	Waveform 3	4.5	9.0	11.5	4.5	15	ns
t_{PLH}	Propagation delay $\overline{MR}$ to $\overline{Q}_n$	Waveform 3	4.0	6.5	8.0	4.0	10	ns

NOTES:
1. For conditions shown as Min or Max, use the appropriate value specified under recommended operating conditions for the applicable type and function table operating mode.
2. All typical values are at V_{CC} = 5V, T_A = 25°C.
3. Not more than one output should be shorted at a time. For testing I_{OS}, the use of high-speed test apparatus and/or sample-and-hold techniques are preferable in order to minimize internal heating and more accurately reflect operational values. Otherwise, prolonged shorting of a High output may raise the chip temperature well above normal and thereby cause invalid readings in other parameter tests. In any sequence of parameter tests, I_{OS} tests should be performed last.
4. When testing devices to the functional table specified refer to the "Recommended Operating Conditions Section" of Application Note 202, "Testing and Specifying FAST Logic".
5. These parameters are guaranteed, but not tested.

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AC SETUP REQUIREMENTS

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS					UNIT
			$T_A = +25°C$ $V_{CC} = +5.0V$ $C_L = 50pF, R_L = 500\Omega$			$T_A = -55°C$ to $+125°C$ $V_{CC} = +5.0V \pm 10\%$ $C_L = 50pF, R_L = 500\Omega$		
			Min	Typ	Max	Min	Max	
$t_s(H)$ $t_s(L)$	Setup time, High or Low D_n to CP	Waveform 2	3.0 3.0			3.0 3.0		ns ns
$t_h(H)$ $t_h(L)$	Hold time, High or Low D_n to CP	Waveform 2	1.0 1.0			1.0 1.0		ns ns
$t_w(H)$ $t_w(L)$	CP pulse width, High or Low	Waveform 1	4.0 5.0			4.0 5.0		ns ns
$t_w(L)$	$\overline{MR}$ pulse width Low	Waveform 3	5.0			5.0		ns
t_{rec}	Recovery time $\overline{MR}$ to CP	Waveform 3	5.0			5.0		ns

AC WAVEFORMS
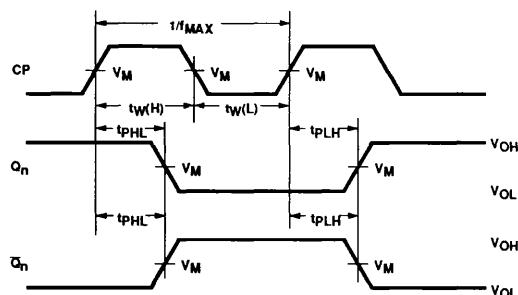
Waveform 1. Clock to Output Delays
and Clock Pulse Width
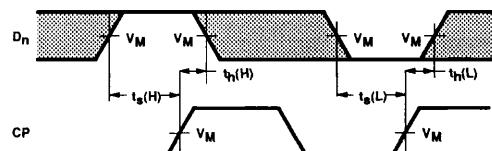
Waveform 2. Data Setup and Hold Times
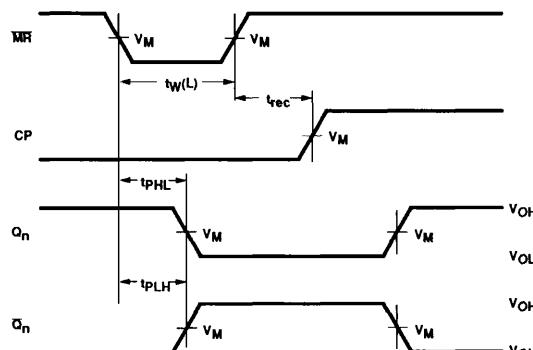
Waveform 3. Master Reset to Output Delay,
Master Reset Pulse Width, and Master Reset Recovery Time

NOTE: For all waveforms $V_M = 1.5V$
The shaded areas indicate when the input is permitted to change for predictable output performance.

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TEST CIRCUIT AND WAVEFORM
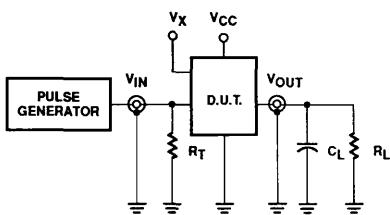
Test Circuit for Totem-Pole Outputs

Input Pulse Definition

DEFINITIONS:

R_L = Load Resistor; see AC Characteristics for value.

C_L = Load capacitance includes jig and probe capacitance; see AC Characteristics for value.

R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.

V_X = Unclocked pins must be held at: $\leq 0.8V$; $\geq 2.7V$ or open per Function Table.
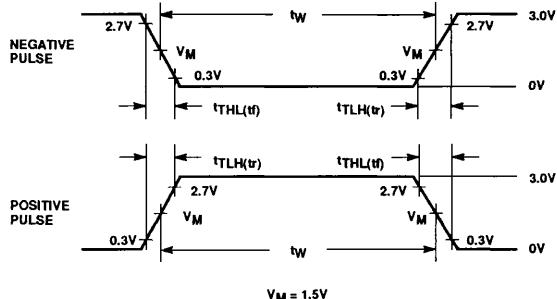
INPUT PULSE CHARACTERISTICS				
Family	Rep. Rate	Pulse Width	t_{TLH}	t_{THL}
54F	1MHz	500ns	≤ 2.5ns	≤ 2.5ns