

# 4076B/74C173/54C173

## QUAD D FLIP-FLOP WITH 3-STATE OUTPUT

**DESCRIPTION** — The 4076B is a Quad Edge-Triggered D Flip-Flop with four Data Inputs ( $D_0$ - $D_3$ ), two active LOW Data Enable Inputs ( $\overline{ED}_0$ - $\overline{ED}_1$ ), an edge-triggered Clock Input (CP), four 3-State Outputs ( $Q_0$ - $Q_3$ ), two active LOW Output Enable inputs ( $\overline{EO}_0$ ,  $\overline{EO}_1$ ), and an overriding asynchronous Master Reset Input (MR).

Information on the Data Inputs ( $D_0$ - $D_3$ ) is stored in the four flip-flops on the LOW-to-HIGH transition of the Clock Input (CP) if both Data Enable Inputs ( $\overline{ED}_0$ - $\overline{ED}_1$ ) are LOW. A HIGH on either Data Enable Input ( $\overline{ED}_0$ - $\overline{ED}_1$ ) prevents the flip-flops from changing on the LOW-to-HIGH transition of the Clock Input (CP), independent of the information on the Data Inputs ( $D_0$ - $D_3$ ).

When both Output Enable inputs ( $\overline{EO}_0$ - $\overline{EO}_1$ ) are LOW, the contents of the four flip-flops are available at the outputs ( $Q_0$ - $Q_3$ ). A HIGH on either Output Enable input ( $\overline{EO}_0$ ,  $\overline{EO}_1$ ) forces the outputs ( $Q_0$ - $Q_3$ ) into the high impedance OFF state.

A HIGH on the overriding asynchronous Master Reset Input (MR) resets all four flip-flops, independent of all other input conditions.

The 4076B is a direct replacement for the 54C173/74C173.

- FULLY INDEPENDENT CLOCK
- 3-STATE OUTPUTS
- CLOCK IS L → H EDGE-TRIGGERED
- ACTIVE LOW DATA ENABLE INPUTS
- ACTIVE LOW OUTPUT ENABLE INPUTS
- ASYNCHRONOUS MASTER RESET

### PIN NAMES

$D_0$ - $D_3$	Data Inputs
$\overline{ED}_0$ - $\overline{ED}_1$	Data Enable Inputs (Active LOW)
$\overline{EO}_0$ , $\overline{EO}_1$	Output Enable Inputs (Active LOW)
CP	Clock Input (L → H Edge-Triggered)
MR	Master Reset Input
$Q_0$ - $Q_3$	Data Outputs

### TRUTH TABLE

INPUTS			OUTPUTS
$\overline{ED}_0$	$\overline{ED}_1$	$D_n$	$Q_{n+1}$
H	X	X	$Q_n$
X	H	X	$Q_n$
L	L	L	L
L	L	H	H

### CONDITIONS:

MR =  $\overline{EO}_0$  =  $\overline{EO}_1$  = LOW

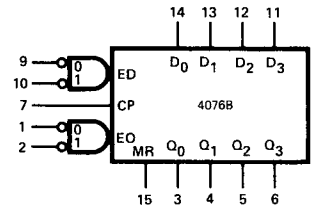
L = LOW Level

H = HIGH Level

X = Don't Care

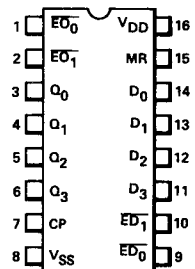
$Q_{n+1}$  = State After Positive Clock Transition

### LOGIC SYMBOL



$V_{DD}$  = Pin 16  
 $V_{SS}$  = Pin 8

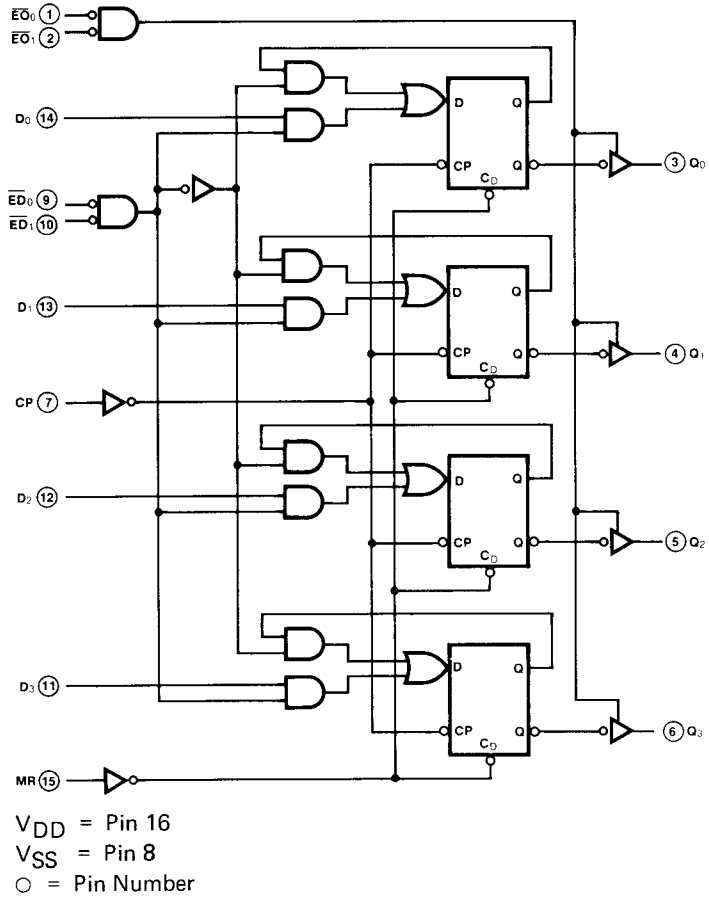
### CONNECTION DIAGRAM DIP (TOP VIEW)



### NOTE:

The Flatpak version has the same pin-outs (Connection Diagram) as the Dual In-line Package.

LOGIC DIAGRAM



FAIRCHILD CMOS • 4076B/74C173/54C173

DC CHARACTERISTICS:  $V_{DD}$  as shown,  $V_{SS} = 0$  V (Note 1)

SYMBOL	PARAMETER	LIMITS									UNITS	TEMP	TEST CONDITIONS
		$V_{DD} = 5$ V			$V_{DD} = 10$ V			$V_{DD} = 15$ V					
		MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX			
$I_{OZH}$	Output OFF Current High	XC								1.6	$\mu$ A	MIN, 25°C	Output returned to $V_{DD}$ . $\overline{E}O_1 = \overline{E}O_0 = V_{DD}$
												12	
		XM								0.4	MIN, 25°C		
										12	MAX		
$I_{OZL}$	Output OFF Current LOW	XC								-1.6	$\mu$ A	MIN, 25°C	Output returned to $V_{SS}$ . $\overline{E}O_1 = \overline{E}O_0 = V_{DD}$
												-12	
		XM								-0.4	MIN, 25°C		
										-12	MAX		
$I_{DD}$	Quiescent Power Supply Current	XC		20			40			80	$\mu$ A	MIN, 25°C	All inputs at 0 V or $V_{DD}$
				150			300			600		MAX	
		XM		5			10			10	MIN, 25°C		
				150			300			600	MAX		

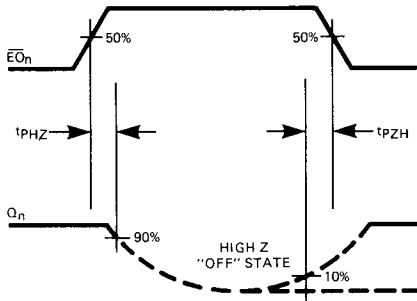
AC CHARACTERISTICS AND SET-UP REQUIREMENTS:  $V_{DD}$  as shown,  $V_{SS} = 0$  V,  $T_A = 25^\circ$ C (See Note 2)

SYMBOL	PARAMETER	LIMITS									UNITS	TEST CONDITIONS
		$V_{DD} = 5$ V			$V_{DD} = 10$ V			$V_{DD} = 15$ V				
		MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX		
$t_{PLH}$	Propagation Delay, CP to $O_n$		70	210		35	105		25	75	ns	$C_L = 50$ pF, $R_L = 200$ k $\Omega$ Input Transition Times $\leq 20$ ns ( $R_L = 1$ k $\Omega$ to $V_{SS}$ ) ( $R_L = 1$ k $\Omega$ to $V_{DD}$ ) ( $R_L = 1$ k $\Omega$ to $V_{SS}$ ) ( $R_L = 1$ k $\Omega$ to $V_{DD}$ )
$t_{PHL}$	Propagation Delay MR to $O_n$		80	240		40	120		25	75	ns	
$t_{PZH}$	Output Enable Time		95	290		50	150		35	105	ns	
$t_{PZL}$	Output Disable Time		95	290		50	150		35	105	ns	
$t_{PHZ}$	Output Transition Time		65	160		40	90		15	35	ns	
$t_{TLH}$	Output Transition Time		65	160		40	90		15	35	ns	
$t_{WCP(L)}$	Minimum Clock Pulse Width	80	25		45	10		36	8		ns	
$t_{WMR(H)}$	Minimum MR Pulse Width	60	35		30	20		24	15		ns	
$t_{rec}$	MR Recovery Time		6			5			2		ns	
$t_s$	Set-Up Time, $D_n$ to CP	15	1		5	1		2	0		ns	
$t_h$	Hold-Time, $D_n$ to CP	45	10		20	2		10	2		ns	
$t_s$	Set-Up Time, $\overline{E}D_n$ to CP	100	50		40	20		30	15		ns	
$t_h$	Hold-Time, $\overline{E}D_n$ to CP	20	2		12	1		8	1		ns	
$f_{MAX}$	Maximum Clock Frequency (Note 3)	4	9		10	16		12	19		MHz	

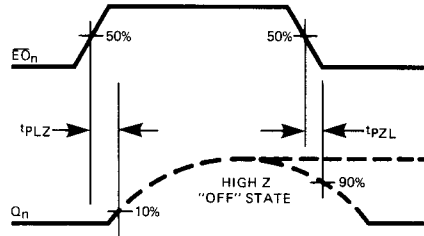
NOTES:

- Additional DC Characteristics are listed in this section under 4000B Series CMOS Family Characteristics.
- Propagation Delays and Output Transition Times are graphically described in this section under 4000B Series CMOS Family Characteristics.
- For  $f_{MAX}$ , input rise and fall times are greater than or equal to 5 ns and less than or equal to 20 ns.
- It is recommended that input rise and fall times to the Clock Input be less than 15  $\mu$ s at  $V_{DD} = 5$  V, 4  $\mu$ s at  $V_{DD} = 20$  V, and 3  $\mu$ s at  $V_{DD} = 15$  V.

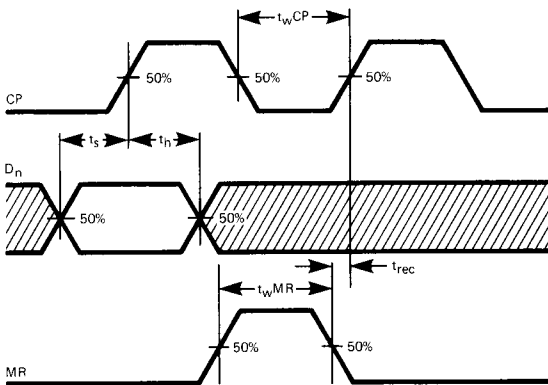
SWITCHING WAVEFORMS



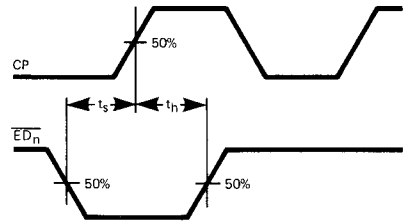
OUTPUT ENABLE TIME ( $t_{pZH}$ ) AND OUTPUT DISABLE TIME ( $t_{pZH}$ )



OUTPUT ENABLE TIME ( $t_{pZL}$ ) AND OUTPUT DISABLE TIME ( $t_{pZL}$ )



MINIMUM PULSE WIDTHS FOR CP AND MR, MR RECOVERY TIME, AND SET-UP AND HOLD-TIMES,  $D_N$  TO CP



SET-UP AND HOLD-TIMES  $\overline{ED}_N$  TO CP

NOTE:  
Set-up and Hold Times are shown as positive values but may be specified as negative values.