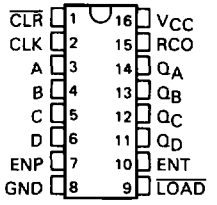
SN54F160A, SN54F162A, SN74F160A, SN74F162A SYNCHRONOUS 4-BIT DECADE COUNTERS

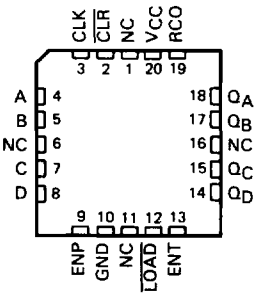
D2932, MARCH 1987

- **Internal Look-Ahead for Fast Counting**
- **Carry Output for n-Bit Cascading**
- **Fully Synchronous Operation for Counting**
- **Package Options Include Plastic "Small Outline" Packages, Ceramic Chip Carriers, and Standard Plastic and Ceramic 300-mil DIPs**
- **Dependable Texas Instruments Quality and Reliability**

SN54F160A, SN54F162A . . . J PACKAGE
SN74F160A, SN74F162A . . . D OR N PACKAGE
(TOP VIEW)



SN54F160A, SN54F162A . . . FK PACKAGE
(TOP VIEW)



NC – No internal connection

description

These synchronous, presettable decade counters feature an internal carry look-ahead for application in high-speed counting designs. Synchronous operation is provided by having all flip-flops clocked simultaneously so that the outputs change coincident with each other when so instructed by the count-enable inputs and internal gating. This mode of operation eliminates the output counting spikes that are normally associated with asynchronous (ripple clock) counters; however, counting spikes may occur on the ripple carry output (RCO). A buffered clock input triggers the four flip-flops on the rising (positive-going) edge of the clock input waveform.

The counters are fully programmable; that is, they may be preset to any number between 0 and 9. As presetting is synchronous, setting up a low level at the load input disables the counter and causes the outputs to agree with the setup data after the next clock pulse regardless of the levels of the enable inputs.

If one of these decade counters is preset to a number between 10 and 15 or assumes such an invalid state when power is applied, it will progress to the normal sequence within two counts as shown in the State Diagram.

The clear function for the 'F160A is asynchronous and a low level at the clear input sets all four of the flip-flop outputs low regardless of the levels of the clock, load, or enable inputs.

The clear function for the 'F162A is synchronous and a low level at the clear input sets all four of the flip-flop outputs low after the next low-to-high transition of the clock regardless of the levels of the enable inputs. This synchronous clear allows the count length to be modified easily by decoding the Q outputs for the maximum count desired. The active-low output of the gate used for decoding is connected to the clear input to synchronously clear the counter to 0000 (LLLL).

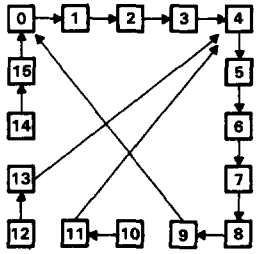
The carry look-ahead circuitry provides for cascading counters for n-bit synchronous applications without additional gating. Instrumental in accomplishing this function are two count-enable inputs and a ripple carry output. Both count-enable inputs (ENP and ENT) must be high to count, and ENT is fed forward to enable the ripple carry output (RCO). RCO thus enabled will produce a high-level pulse while the count is 9 (HLLH). This high-level overflow ripple carry pulse can be used to enable successive cascaded stages. Transitions at the ENP or ENT are allowed regardless of the level of the clock input.

description (continued)

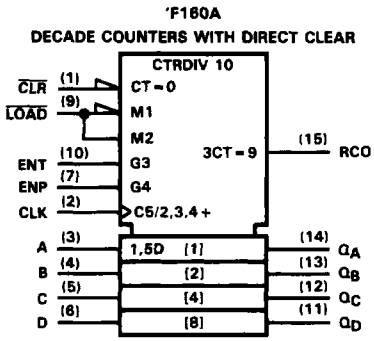
These counters feature a fully independent clock circuit. Changes at control inputs (ENP, ENT, or $\overline{\text{LOAD}}$) that will modify the operating mode have no effect on the contents of the counter until clocking occurs. The function of the counter (whether enabled, disabled, loading, or counting) will be dictated solely by the conditions meeting the setup and hold times.

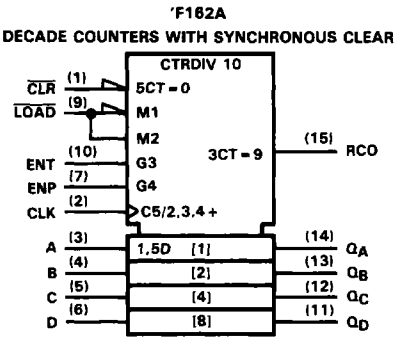
The SN54F160A and SN54F162A are characterized for operation over the full military temperature range of −55°C to 125°C. The SN74F160A and SN74F162A are characterized for operation from 0°C to 70°C.

state diagram



logic symbols†





†These symbols are in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.
Pin numbers shown are for D, J, and N packages.

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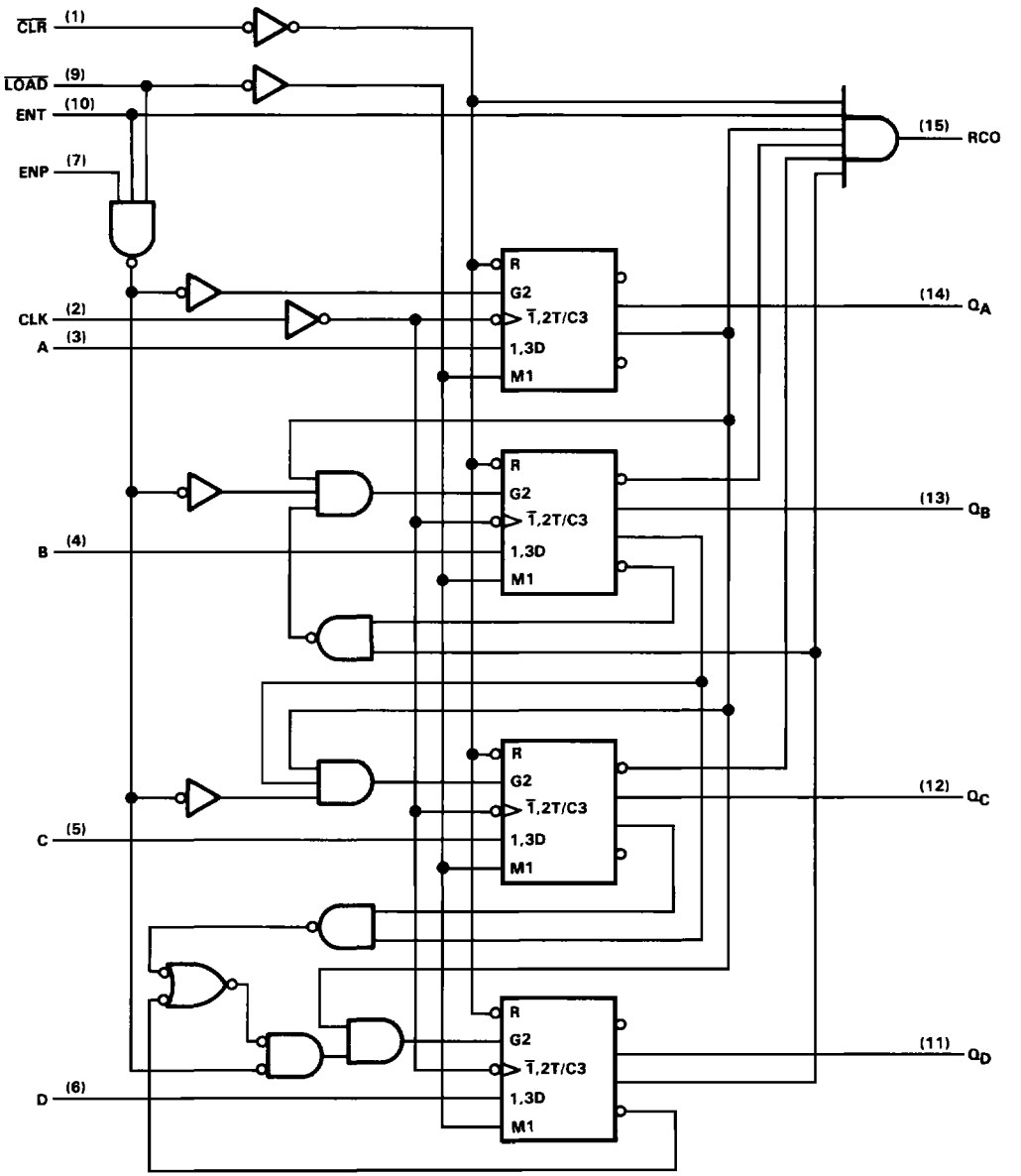
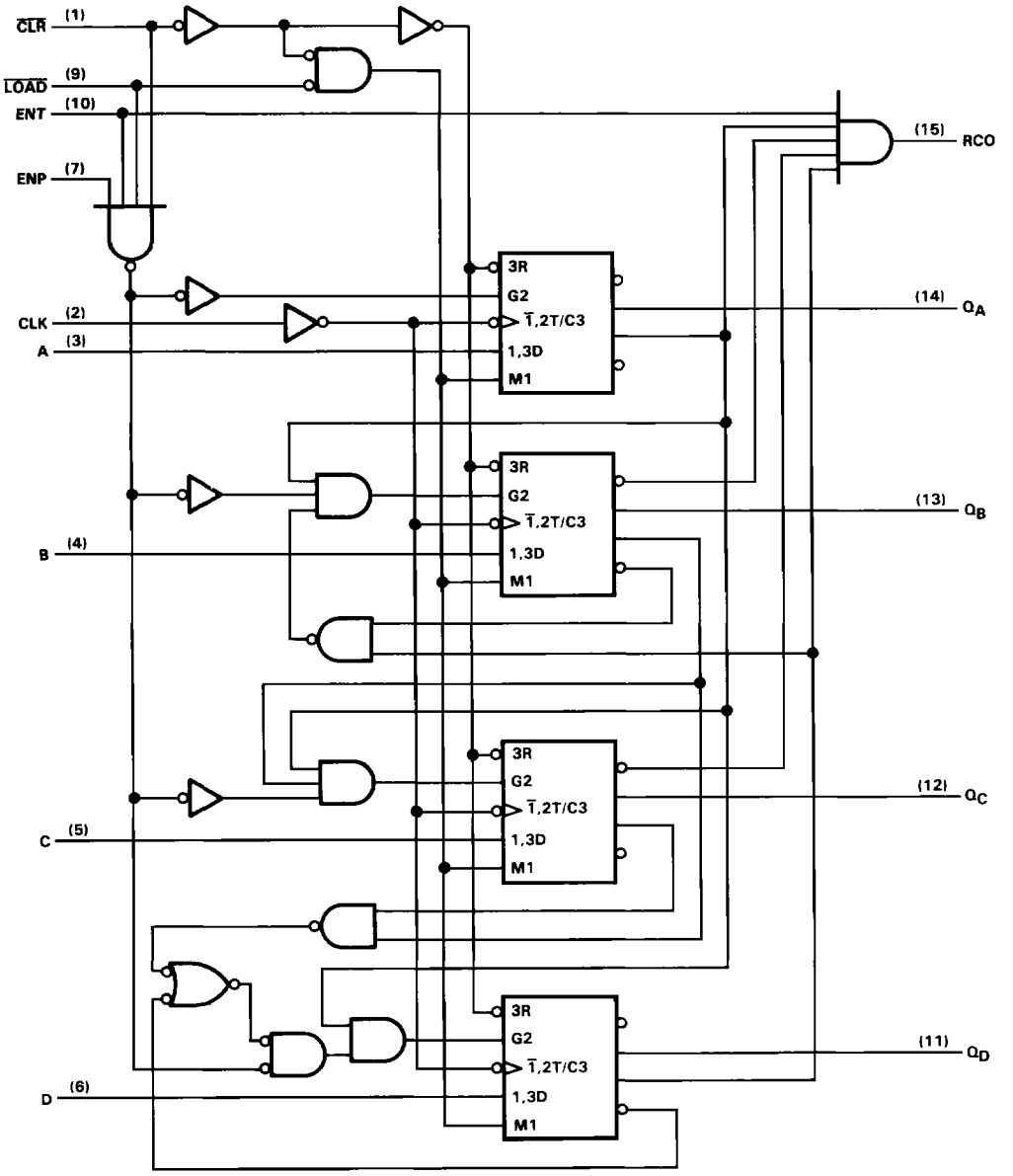
'F160A logic diagram (positive logic)



'F162A logic diagram (positive logic)



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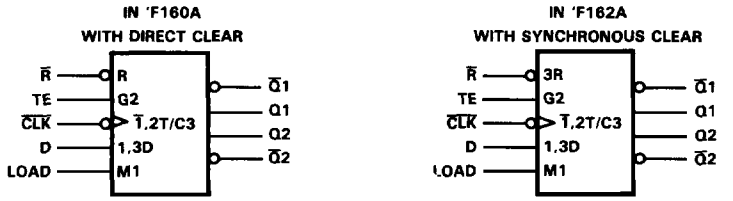
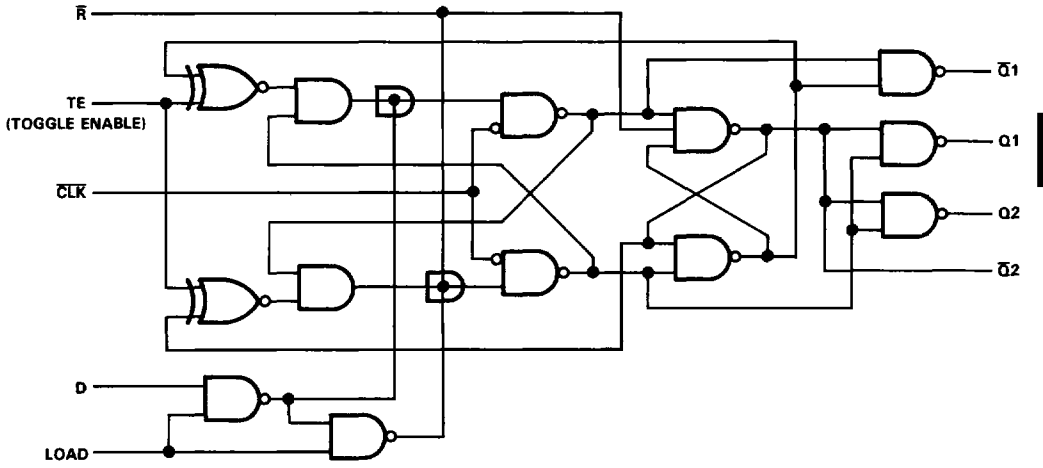
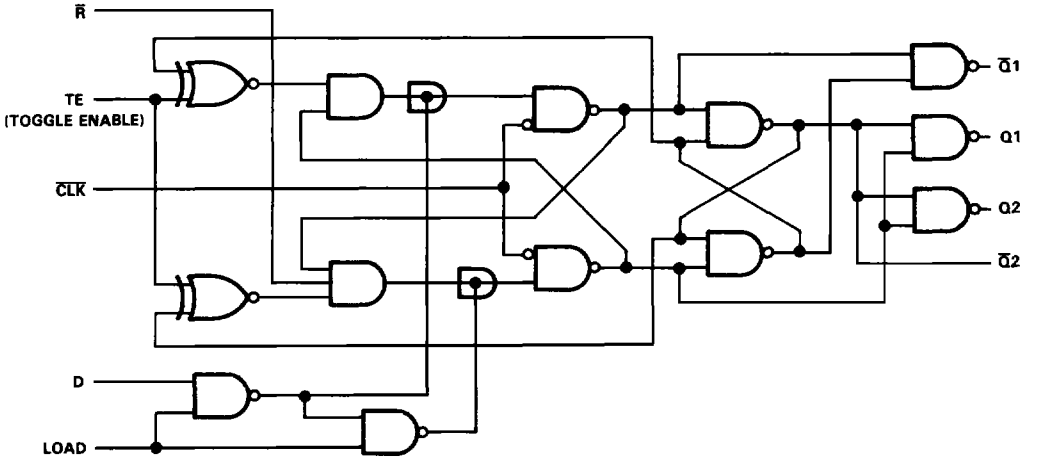
logic symbol, each flip-flop (positive logic)



logic diagram, each flip-flop in 'F160A (positive logic)



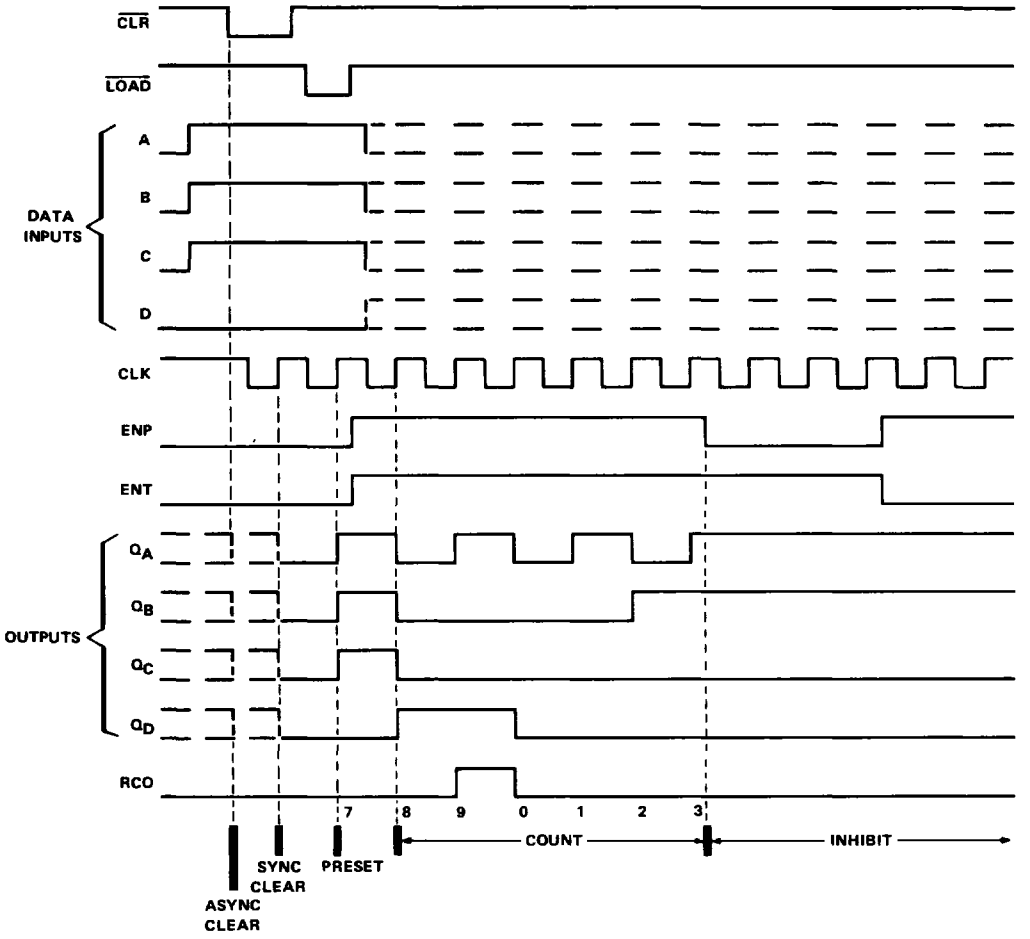
logic diagram, each flip-flop in 'F162A (positive logic)



typical clear, preset, count, and inhibit sequences

Illustrated below is the following sequence:

1. Clear outputs to zero ('F160A is asynchronous; 'F162A is synchronous)
2. Preset to BCD seven
3. Count to eight, nine, zero, one, two, and three
4. Inhibit



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absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} . . . . . −0.5 V to 7 V
Input voltage† . . . . . −1.2 V to 7 V
Input current . . . . . −30 mA to 5 mA
Voltage applied to any output in the high state . . . . . −0.5 V to V_{CC}
Current into any output in the low state . . . . . 40 mA
Operating free-air temperature range: SN54F160A, SN54F162A . . . . . −65°C to 150°C
SN74F160A, SN74F162A . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C

†The input voltage ratings may be exceeded provided the input current ratings are observed.

recommended operating conditions

		SN54F160A SN54F162A			SN74F160A SN74F162A			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage	4.5	5	5.5	4.5	5	5.5	V
V_{IH}	High-level input voltage	2			2			V
V_{IL}	Low-level input voltage			0.8			0.8	V
I_{IK}	Input clamp current			−18			−18	mA
I_{OH}	High-level outut current			−1			−1	mA
I_{OL}	Low-level output current			20			20	mA
T_A	Operating free-air temperature	−55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS		SN54F160A SN54F162A			SN74F160A SN74F162A			UNIT
				MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V_{IK}		V_{CC} = 4.5 V,	I_I = −18 mA			−1.2			−1.2	V
V_{OH}§		V_{CC} = 4.5 V,	I_{OH} = −1 mA	2.5	3.4		2.5	3.4		V
V_{OL}		V_{CC} = 4.5 V,	I_{OL} = 20 mA		0.3	0.5		0.3	0.5	V
I_I		V_{CC} = 5.5 V,	V_I = 7 V			0.1			0.1	mA
I_{IH}		V_{CC} = 5.5 V,	V_I = 2.7 V			20			20	μA
I_{IL}	ENP, CLK, A, B, C, D	V_{CC} = 5.5 V,	V_I = 0.5 V			−0.6			−0.6	mA
	ENT, $\overline{LOAD}$					−1.2			−1.2	
	$\overline{CLR}$ ('F160A)					−0.6			−0.6	
	$\overline{CLR}$ ('F162A)					−1.2			−1.2	
I_{OS}¶		V_{CC} = 5.5 V,	V_O = 0	−60		−150	−60		−150	mA
I_{CC}		V_{CC} = 5.5 V			37	55		37	55	mA

‡All typical values are at V_{CC} = 5 V, T_A = 25°C.
§For SN74F160A and SN74F162A at V_{CC} = 4.75 V and I_{OH} = −1 mA, V_{OH} min = 2.7 V.
¶Not more than one output should be shorted at a time and the duration of the short circuit should not exceed one second.

timing requirements

			V_{CC} = 5 V, T_A = 25°C			V_{CC} = 4.5 V to 5.5 V, T_A = MIN to MAX†				UNIT
			'F160A, 'F162A			SN54F160A SN54F162A		SN74F160A SN74F162A		
			MIN		MAX	MIN	MAX	MIN	MAX	
f_{clock}	Clock frequency		0		100			0	90	MHz
t_{su}	Setup time, data (A, B, C, D) high or low before CLK↑		5					5		ns
t_{hold}	Hold time, data (A, B, C, D) high or low after CLK↑		2					2		ns
t_{su}	Setup time, $\overline{LOAD}$ and (for 'F162A) $\overline{CLR}$ before CLK↑	High	11					11.5		ns
		Low	8.5					9.5		
t_{hold}	Hold time, $\overline{LOAD}$ and (for 'F162A) $\overline{CLR}$ after CLK↑	High	2					2		ns
		Low	0					0		
t_{su}	Setup time, ENP and ENT before CLK↑	High	11					11.5		ns
		Low	5					5		
t_{hold}	Hold time, ENP and ENT high or low after CLK↑		0					0		ns
t_w	Pulse duration, CLK high or low (loading)		5					5		ns
t_w	Pulse duration, CLK (counting)	High	4					4		ns
		Low	6					7		
t_w	Pulse duration, $\overline{CLR}$ low ('F160A)		5					5		ns
t_{su}	Inactive-state setup time, $\overline{CLR}$ high before CLK↑ ('F160A)‡		6					6		ns

switching characteristics (see Note 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 5 V, C_L = 50 pF, R_L = 500 Ω, T_A = 25°C			V_{CC} = 4.5 V to 5.5 V, C_L = 50 pF, R_L = 500 Ω, T_A = MIN to MAX†				UNIT
			'F160A, 'F162A			SN54F160A SN54F162A		SN74F160A SN74F162A		
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
f_{max}			100	120				90		MHz
t_{PLH}	CLK ($\overline{LOAD}$ high)	Any Q	2.7	5.1	7.5			2.7	8.5	ns
t_{PHL}			2.7	7.1	10			2.7	11	
t_{PLH}	CLK ($\overline{LOAD}$ low)	Any Q	3.2	5.6	8.5			3.2	9.5	ns
t_{PHL}			3.2	5.6	8.5			3.2	9.5	
t_{PLH}	CLK	RCO	4.2	9.6	14			4.2	15	ns
t_{PHL}			4.2	9.6	14			4.2	15	
t_{PLH}	ENT	RCO	1.7	4.1	7.5			1.7	8.5	ns
t_{PHL}			1.7	4.1	7.5			1.7	8.5	
t_{PHL}	$\overline{CLR}$ ('F160A)	Any Q	4.7	8.6	12			4.7	13	ns
t_{PHL}	$\overline{CLR}$ ('F160A)	RCO	3.7	7.6	10.5			3.7	11.5	ns

† For conditions shown as MIN or MAX, use the appropriate value specified under Recommended Operating Conditions.
‡ Inactive-state setup time is also referred to as "recovery time".
NOTE 1: See General Information for load circuits and waveforms.

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