MOTOROLA

Military 54LS240

Octal Buffer/Line Driver With 3-State Outputs (Inverting)

ELECTRICALLY TESTED PER:
MIL-M-38510/32401

The 54LS240 is an Octal Buffer and Line driver designed to be employed as a memory address driver, clock driver and bus oriented transmitter/receiver which will provide improved PC board density.

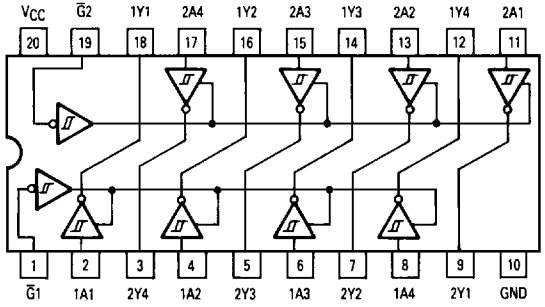
- Hysteresis at Inputs to Improve Noise Margins
- 3-State Outputs Drive Bus Lines or Buffer Memory Address Registers
- Input Clamp Diodes Limit High-Speed Termination Effects

AVAILABLE AS:

1) JAN: JM38510/32401BXA
2) SMD: 7801201
3) 883C: 54LS240/BXAJC

X = CASE OUTLINE AS FOLLOWS:
PACKAGE: CERDIP: R
CERFLAT: S
LCC: 2
***Call Factory for latest update**

LOGIC DIAGRAM



PIN ASSIGNMENTS

FUNCTION	DIL	FLATS	LCC	BURN-IN (CONDITION A)
$\overline{G}1$	1	1	1	GND
1A1	2	2	2	GND
2Y4	3	3	3	V_{CC}
1A2	4	4	4	GND
2Y3	5	5	5	V_{CC}
1A3	6	6	6	GND
2Y2	7	7	7	V_{CC}
1A4	8	8	8	GND
2Y1	9	9	9	V_{CC}
GND	10	10	10	GND
2A1	11	11	11	GND
1Y4	12	12	12	V_{CC}
2A2	13	13	13	GND
1Y3	14	14	14	V_{CC}
2A3	15	15	15	GND
1Y2	16	16	16	V_{CC}
2A4	17	17	17	GND
1Y1	18	18	18	V_{CC}
$\overline{G}2$	19	19	19	GND
V_{CC}	20	20	20	V_{CC}

BURN-IN CONDITIONS:
V_{CC} = 5.0 V MIN/6.0 V MAX

TRUTH TABLE

Inputs		Output
$1\overline{G}$, $2\overline{G}$	D	
L	L	H
L	H	L
H	X	(Z)

H = HIGH Voltage Level
L = LOW Voltage Level
X = Immaterial
Z = HIGH Impedance

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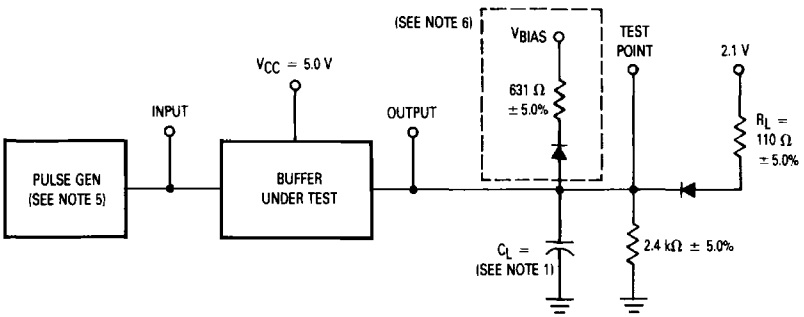
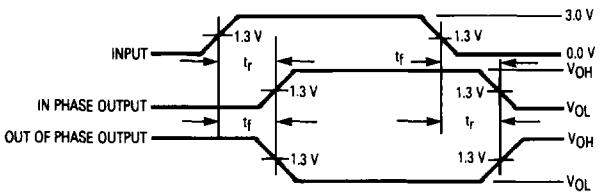
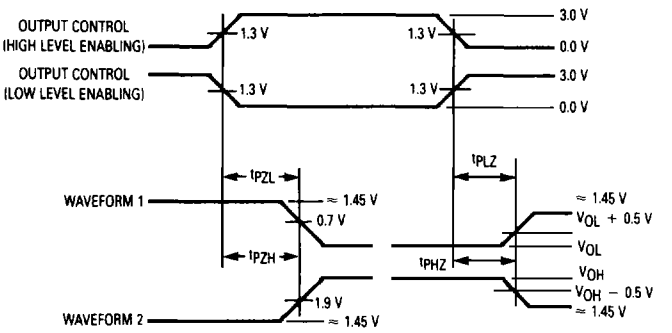
AC TEST CIRCUIT



WAVEFORMS



Voltage Waveforms Propagation Delay Times



Voltage Waveforms Enable and Disable Times, Three-State Outputs

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Symbol	Parameter	Limits						Units	Test Condition (Unless Otherwise Specified)
		+25°C		+125°C		−55°C			
	Static Parameters:	Subgroup 1		Subgroup 2		Subgroup 3			
		Min	Max	Min	Max	Min	Max		
V_{OHH}	Logical "1" Output Voltage	2.4		2.4		2.4		V	V_{CC} = 4.5 V, I_{OH} = −3.0 mA, V_{IN} = 0.7 V (other inputs are open), $\overline{G1}/\overline{G2}$ = 0.7 V or open per truth table.
V_{OHL}	Logical "1" Output Voltage	2.0		2.0		2.0		V	V_{CC} = 4.5 V, I_{OH} = −12 mA, V_{IN} = 0.5 V (other inputs are open), $\overline{G1}/\overline{G2}$ = 0.5 V or open per truth table.
V_{OL1}	Logical "0" Output Voltage		0.4		0.4		0.4	V	V_{CC} = 4.5 V, I_{OL} = 12 mA, V_{IN} = 2.0 V (other inputs are open), $\overline{G1}/\overline{G2}$ = 0.7 V or open per truth table.
V_{OL2}	Logical "0" Output Voltage		0.45		0.45		0.45	V	V_{CC} = 4.5 V, I_{OL} = 18 mA, V_{IN} = 2.0 V (other inputs are open), $\overline{G1}/\overline{G2}$ = 0.7 V or open per truth table.
V_{IC}	Input Clamping Voltage		−1.5					V	V_{CC} = 4.5 V, I_{IN} = −18 mA, all other inputs are open.
I_{IH}	Logical "1" Input Current		20		20		20	μA	V_{CC} = 5.5 V, V_{IH} = 2.7 V, other inputs are open.
I_{IHH}	Logical "1" Input Current		100		100		100	μA	V_{CC} = 5.5 V, V_{IHH} = 5.5 V, other inputs are open.
I_{IL}	Logical "0" Input Current	−5.0	−200	−5.0	−200	−5.0	−200	μA	V_{CC} = 5.5 V, V_{IN} = 0.4 V, other inputs are open.
I_{OS}	Output Short Circuit Current	−40	−225	−40	−225	−40	−225	mA	V_{CC} = 5.5 V, V_{IN} = GND (other inputs are open), V_{OUT} = GND, $\overline{G1}/\overline{G2}$ = GND or open per truth table.
I_{IOZH}	Output Off Current High		20		20		20	μA	V_{CC} = 5.5 V, all inputs are open, V_{OUT} = 2.7 V, $\overline{G1}/\overline{G2}$ = 2.0 V or open per truth table.
I_{IOZL}	Output Off Current Low		−20		−20		−20	μA	V_{CC} = 5.5 V, all inputs are open, V_{OUT} = 0.4 V, $\overline{G1}/\overline{G2}$ = 2.0 V or open per truth table.
I_{CCH}	Power Supply Current		27		27		27	mA	V_{CC} = 5.5 V, V_{IN} = GND (all inputs).
I_{CCL}	Power Supply Current		44		44		44	mA	V_{CC} = 5.5 V, V_{IN} = 5.5 V (all inputs), $\overline{G1}/\overline{G2}$ = GND.
I_{CCZ}	Power Supply Current Off		50		50		50	mA	V_{CC} = 5.5 V, all inputs are open, $\overline{G1}/\overline{G2}$ = 5.5 V.
V_{IH}	Logical "1" Input Voltage	2.0		2.0		2.0		V	V_{CC} = 4.5 V.
V_{IL}	Logical "0" Input Voltage		0.7		0.7		0.7	V	V_{CC} = 4.5 V.

Symbol	Parameter	Limits			Units	Test Condition (Unless Otherwise Specified)
		+25°C	+125°C	−55°C		
		Subgroup 7	Subgroup 8A	Subgroup 8B		
	Functional Tests					per Truth Table with V_{CC} = 5.0 V, V_{INL} = 0.4 V, and V_{INH} = 2.4 V.

Symbol	Parameter	Limits						Units	Test Condition (Unless Otherwise Specified)
	Switching Parameters	+25°C		+125°C		−55°C			
		Subgroup 9		Subgroup 10		Subgroup 11			
		Min	Max	Min	Max	Min	Max		
t_{PHL1} t_{PHL1}	Propagation Delay /Data-Output Output High-Low	2.0	18 18	2.0	23 23	2.0	23 23	ns	V_{CC} = 5.0 V, C_L = 50 pF, R_L = 110 Ω. V_{CC} = 5.0 V, C_L = 45 pF, R_L = 667 Ω.
t_{PLH1} t_{PLH1}	Propagation Delay /Data-Output Output Low-High	2.0	14 14	2.0	18 18	2.0	18 18	ns	V_{CC} = 5.0 V, C_L = 50 pF, R_L = 110 Ω. V_{CC} = 5.0 V, C_L = 45 pF, R_L = 667 Ω.
t_{PLZ1} t_{PLZ1}	Propagation Delay /Data-Output Output Low-High	2.0	30 25	2.0	39 34	2.0	39 34	ns	V_{CC} = 5.0 V, C_L = 50 pF, R_L = 110 Ω. V_{CC} = 5.0 V, C_L = 45 pF, R_L = 667 Ω.
t_{PHZ1} t_{PHZ1}	Propagation Delay /Data-Output Output High-Low	2.0	35 18	2.0	45 40	2.0	45 40	ns	V_{CC} = 5.0 V, C_L = 50 pF, R_L = 110 Ω. V_{CC} = 5.0 V, C_L = 45 pF, R_L = 667 Ω.
t_{PZL1} t_{PZL1}	Propagation Delay /Data-Output Output Low-High	2.0	30 30	2.0	39 34	2.0	39 34	ns	V_{CC} = 5.0 V, C_L = 50 pF, R_L = 110 Ω. V_{CC} = 5.0 V, C_L = 45 pF, R_L = 667 Ω.
t_{PZH1} t_{PZH1}	Propagation Delay /Data-Output Output High-Low	2.0	30 23	2.0	39 34	2.0	39 34	ns	V_{CC} = 5.0 V, C_L = 50 pF, R_L = 110 Ω. V_{CC} = 5.0 V, C_L = 45 pF, R_L = 667 Ω.

NOTES:
1. C_L = 50 pF ± 10%. C_L includes scope probe and jig capacitance.
2. All diodes are 1N3064 or equivalent.
3. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
4. In the test circuit example, the phase relationships between inputs and outputs have been chosen arbitrarily.
5. All input pulses are supplied by generators having the following characteristics:
   PRR ≤ 1.0 MHz, t_p = 500 ns, Z_{OUT} ≈ 50 Ω, V_{gen} = 3.0 V, t_r ≤ 15 ns and t_f ≤ 6.0 ns between 0.7 V and 2.7 V.
6. The diode and resistor shown within the dotted area are optional. When the diode and resistor are used, V_{BIAS} shall be 5.5 V for all tests except for t_{PHZ}, for t_{PHZ} tests, V_{BIAS} shall be −0.6 V.

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