MOTOROLA

Military 54LS10

Triple 3-Input Positive NAND Gate

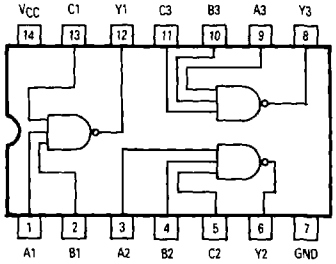
ELECTRICALLY TESTED PER:
MIL-M-38510/30005

AVAILABLE AS:

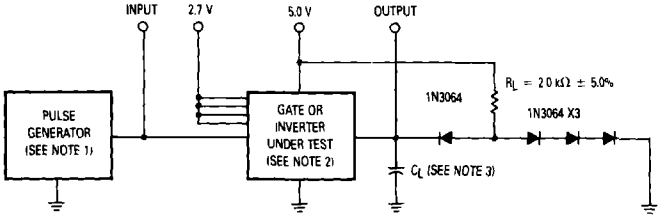
1) JAN: JM38510/30005BXA
2) SMD: *
3) 883C: 54LS10/BXAJC

X = CASE OUTLINE AS FOLLOWS:
PACKAGE: CERDIP: C
CERFLAT: D
LCC: 2
***Call Factory for latest update**

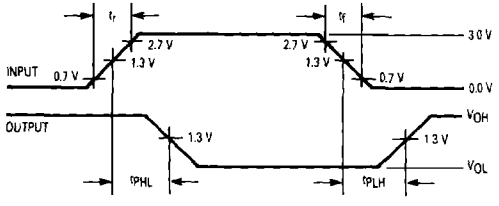
LOGIC DIAGRAM



AC TEST CIRCUIT



WAVEFORMS



NOTES:
1. Pulse generator has the following characteristics: $t_r \leq 15$ ns, $t_f \leq 6.0$ ns, PRR ≤ 1.0 MHz, duty cycle ≈ 50% and $Z_{OUT} = 50\ \Omega$.
2. Inputs not under test are at 2.7 V.
3. $C_L = 50$ pF ± 10%, including scope probe, wiring and stray capacitance.
4. $R_L = 2.0$ kΩ ± 5.0%.
5. Voltage measurements are to be made with respect to network ground terminal.

PIN ASSIGNMENTS

FUNCTION	DIL	FLATS	LCC	BURN-IN (CONDITION A)
A1	1	1	2	V_{CC}
B1	2	2	3	GND
A2	3	3	4	V_{CC}
B2	4	4	6	V_{CC}
C2	5	5	8	GND
Y2	6	6	9	V_{CC}
GND	7	7	10	GND
Y3	8	8	12	V_{CC}
A3	9	9	13	V_{CC}
B3	10	10	14	GND
C3	11	11	16	V_{CC}
Y1	12	12	18	V_{CC}
C1	13	13	19	GND
V_{CC}	14	14	20	V_{CC}

BURN-IN CONDITIONS:
V_{CC} = 5.0 V MIN/6.0 V MAX

TRUTH TABLE

A	B	C	Y
0	0	0	0
0	0	1	1
0	1	0	1
0	1	1	1
1	0	0	1
1	0	1	1
1	1	0	1
1	1	1	1

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Symbol	Parameter	Limits						Units	Test Condition (Unless Otherwise Specified)
		+25°C		+125°C		−55°C			
	Static Parameters:	Subgroup 1		Subgroup 2		Subgroup 3			
		Min	Max	Min	Max	Min	Max		
V_{OH}	Logical "1" Output Voltage	2.5		2.5		2.5		V	V_{CC} = 4.5 V, I_{OH} = −400 μA, V_{IL} = 0.7 V, V_{IN} = 5.5 V on other input.
V_{OL}	Logical "0" Output Voltage		0.4		0.4		0.4	V	V_{CC} = 4.5 V, I_{OL} = 4.0 mA, V_{IH} = 2.0 V on all inputs.
V_{IC}	Input Clamping Voltage		−1.5					V	V_{CC} = 4.5 V, I_{IN} = −18 mA, other inputs are open.
I_{IH1}	Logical "1" Input Current		20		20		20	μA	V_{CC} = 5.5 V, V_{IN} = 2.7 V, other inputs = 0 V.
I_{IH2}	Logical "1" Input Current		100		100		100	μA	V_{CC} = 5.5 V, V_{IN} = 5.5 V, other inputs = 0 V.
I_{IL}	Logical "0" Input Current	−160	−400	−160	−400	−160	−400	μA	V_{CC} = 5.5 V, V_{IN} = 0.4 V, other inputs = 5.5 V.
I_{OS}	Output Short Circuit Current	−15	−100	−15	−100	−15	−100	mA	V_{CC} = 5.5 V, V_{IN} = 0 V (all inputs), V_{OUT} = 0 V.
I_{CCH}	Power Supply Current		1.2		1.2		1.2	mA	V_{CC} = 5.5 V, V_{IN} = 0 V (all inputs).
I_{CCL}	Power Supply Current		3.3		3.3		3.3	mA	V_{CC} = 5.5 V, V_{IN} = 5.5 V (all inputs).
V_{IH}	Logical "1" Input Voltage	2.0		2.0		2.0		V	V_{CC} = 4.5 V.
V_{IL}	Logical "0" Input Voltage		0.7		0.7		0.7	V	V_{CC} = 4.5 V.
		Subgroup 7		Subgroup 8A		Subgroup 8B			
	Functional Tests								per Truth Table with V_{CC} = 5.0 V, V_{INL} = 0.5 V, and V_{INH} = 2.5 V.

Symbol	Parameter	Limits						Units	Test Condition (Unless Otherwise Specified)
		+25°C		+125°C		−55°C			
	Switching Parameters	Subgroup 9		Subgroup 10		Subgroup 11			
		Min	Max	Min	Max	Min	Max		
t_{PHL}	Propagation Delay /Data-Output	2.0	17	2.0	24	2.0	24	ns	V_{CC} = 5.0 V, C_L = 50 pF, R_L = 2.0 kΩ.
t_{PHL}	Output High-Low	—	15	—	19	—	19	ns	V_{CC} = 5.0 V, C_L = 15 pF, R_L = 2.0 kΩ.
t_{PLH}	Propagation Delay /Data-Output	2.0	15	2.0	20	2.0	20	ns	V_{CC} = 5.0 V, C_L = 50 pF, R_L = 2.0 kΩ.
t_{PLH}	Output Low-High	—	15	—	15	—	15	ns	V_{CC} = 5.0 V, C_L = 15 pF, R_L = 2.0 kΩ.

NOTE:
1. The limits specified for C_L = 15 pF are guaranteed but not tested.

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