

SLLIMM™ (small low-loss intelligent molded module) IPM, single phase - 35 A, 600 V short-circuit rugged IGBT

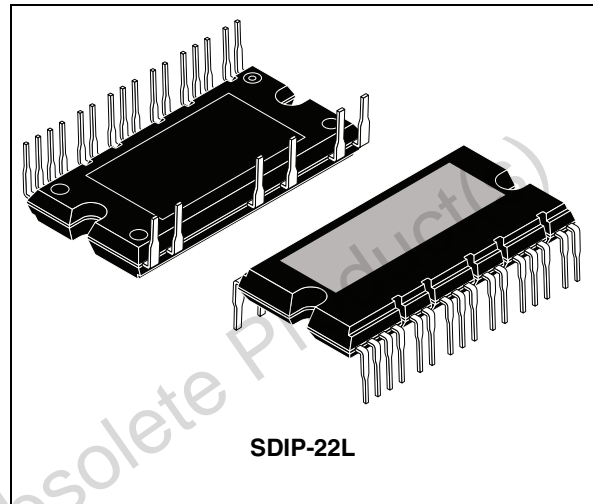
Datasheet – production data

Features

- IPM 35 A, 600 V single phase IGBT including control ICs for gate driving and free-wheeling diodes
- Short-circuit rugged IGBTs
- $V_{CE(sat)}$ negative temperature coefficient
- 3.3 V, 5 V, 15 V CMOS/TTL inputs comparators with hysteresis and pull down / pull up resistors
- Undervoltage lockout
- Internal bootstrap diode
- Dead time and interlocking function
- Smart shutdown function
- Comparator for fault protection against over temperature and overcurrent
- Op amp for advanced current sensing
- DBC substrate leading to low thermal resistance
- Isolation rating of 2500 V_{rms}/min
- 4.7 kΩ NTC for temperature control
- UL Recognized : UL1557 file E81734

Applications

- Power inverters for compressors



Description

This intelligent power module provides a compact, high performance AC motor drive for a simple and rugged design. It targets power inverters for air conditioners. It combines ST proprietary control ICs with the most advanced short-circuit rugged IGBT system technology. SLLIMM™ is a trademark of STMicroelectronics.

Table 1. Device summary

| Order code | Marking | Package | Packaging |
|---------------|-------------|----------|-----------|
| STGIPS35K60L1 | GIPS35K60L1 | SDIP-22L | Tube |

Contents

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Obsolete Product(s) - Obsolete Product(s)

1 Internal schematic diagram and pin configuration

Figure 1. Internal schematic diagram

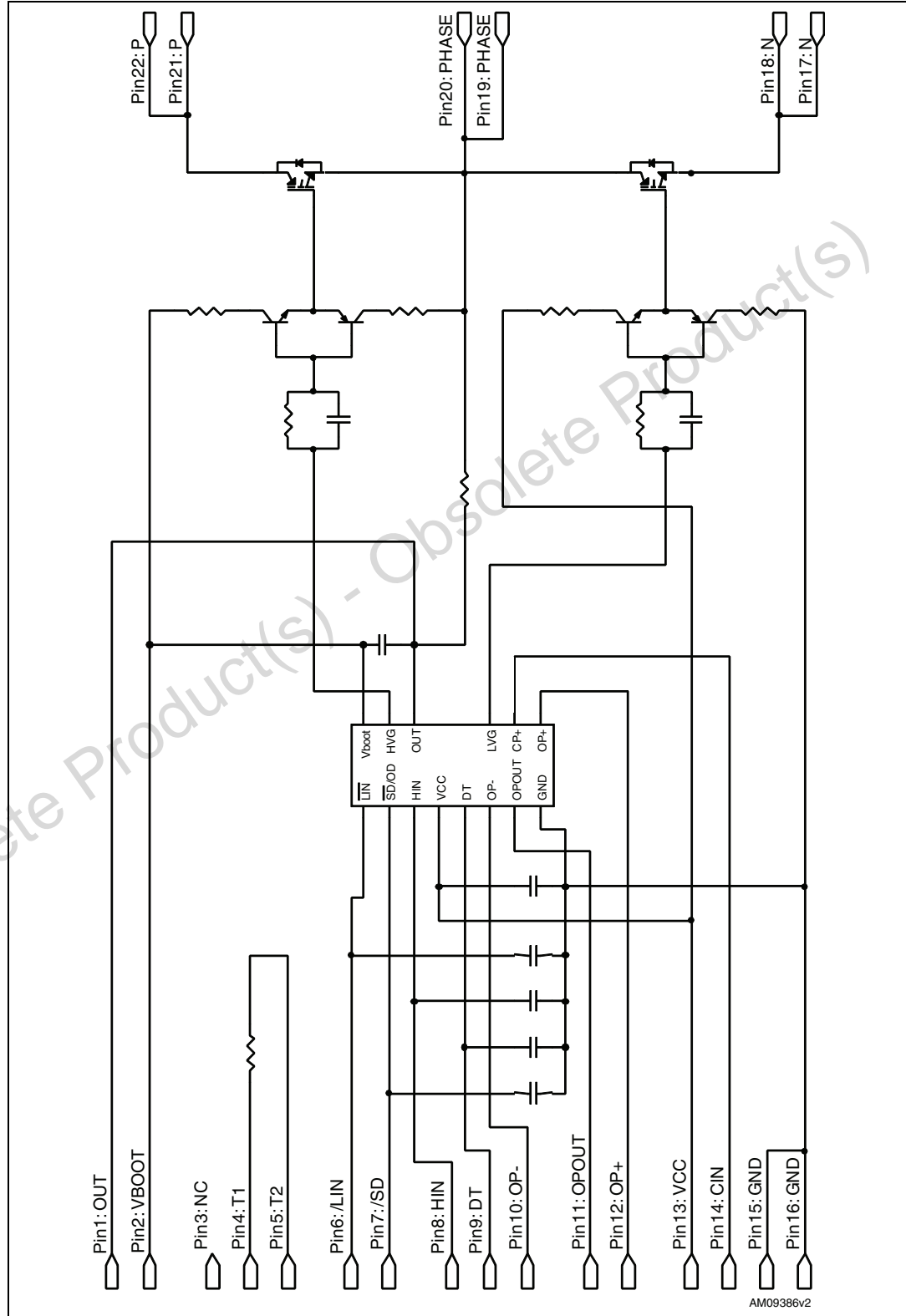
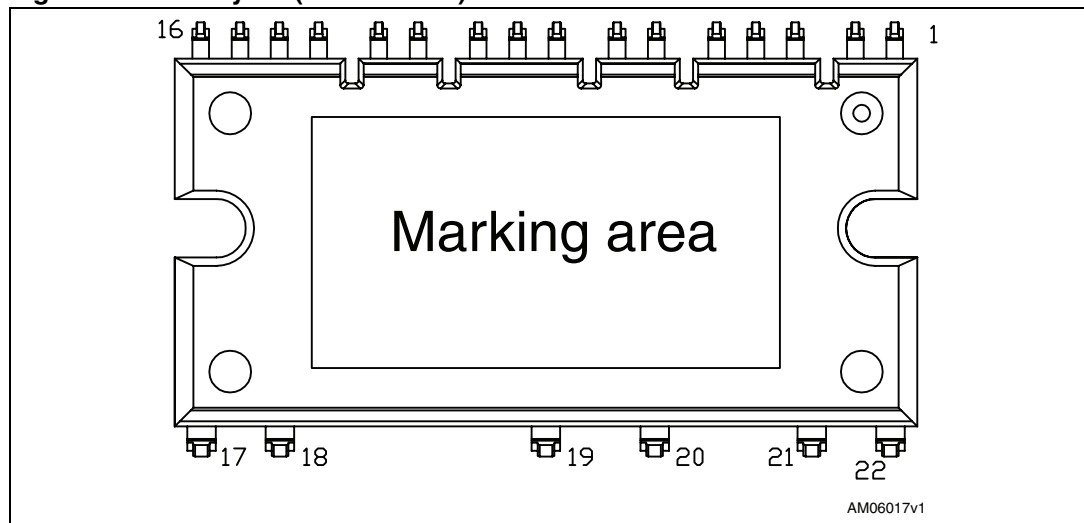


Table 2. Pin description

| Pin | Symbol | Description |
|-----|---------------------------|--------------------------------------------------------------------|
| 1 | OUT _{PHASE} | PHASE reference output |
| 2 | V _{boot} | Bootstrap voltage |
| 3 | NC | Not connected |
| 4 | T ₁ | NTC thermistor terminal 1 |
| 5 | T ₂ | NTC thermistor terminal 2 |
| 6 | $\overline{\text{LIN}}$ | Low side logic input |
| 7 | $\overline{\text{SD/OD}}$ | Shutdown logic input (active low) / open drain (comparator output) |
| 8 | HIN | High side logic input |
| 9 | DT | Dead time setting |
| 10 | OP- | Op amp inverting input |
| 11 | OP _{OUT} | Op amp output |
| 12 | OP+ | Op amp non inverting input |
| 13 | V _{CC} | Low voltage power supply |
| 14 | CIN | Comparator input |
| 15 | GND | Ground |
| 16 | GND | Ground |
| 17 | N | Negative DC input |
| 18 | N | Negative DC input |
| 19 | PHASE | Phase output |
| 20 | PHASE | Phase output |
| 21 | P | Positive DC input |
| 22 | P | Positive DC input |

Figure 2. Pin layout (bottom view)



2 Electrical ratings

2.1 Absolute maximum ratings

Table 3. Inverter part

| Symbol | Parameter | Value | Unit |
|--------------------|-----------------------------------------------------------------------------------------------------------------------------------------------------|-------|---------------|
| V_{CES} | Each IGBT collector emitter voltage ($V_{IN} = 0$) | 600 | V |
| $\pm I_C^{(1)}$ | Each IGBT continuous collector current at $T_C = 25^\circ\text{C}$ | 35 | A |
| $\pm I_{CP}^{(2)}$ | Each IGBT pulsed collector current | 70 | A |
| P_{TOT} | Each IGBT total dissipation at $T_C = 25^\circ\text{C}$ | 100 | W |
| t_{scw} | Short circuit withstand time, $V_{CE} = 0.5 V_{(BR)CES}$ $T_J = 125^\circ\text{C}$, $V_{CC} = V_{boot} = 15\text{ V}$, $V_I = 1$ "logic state" | 5 | μs |

1. Calculated according to the iterative formula:

$$I_C(T_C) = \frac{T_{j(\max)} - T_C}{R_{thj-c} \times V_{CE(\text{sat})(\max)}(T_{j(\max)}, I_C(T_C))}$$

2. Pulse width limited by max junction temperature

Table 4. Control part

| Symbol | Parameter | Min. | Max. | Unit |
|---------------|----------------------------------------------------------------------|-----------------|------------------|------|
| V_{OUT} | Output voltage applied between OUT_U , OUT_V , OUT_W - GND | $V_{boot} - 21$ | $V_{boot} + 0.3$ | V |
| V_{CC} | Low voltage power supply | - 0.3 | 21 | V |
| V_{CIN} | Comparator input voltage | - 0.3 | $V_{CC} + 0.3$ | V |
| V_{op+} | OPAMP non-inverting input | - 0.3 | $V_{CC} + 0.3$ | V |
| V_{op-} | OPAMP inverting input | - 0.3 | $V_{CC} + 0.3$ | V |
| V_{boot} | Bootstrap voltage | - 0.3 | 620 | V |
| V_{IN} | Logic input voltage applied between HIN , \overline{LIN} and GND | - 0.3 | 15 | V |
| $V_{SD/OD}$ | Open drain voltage | - 0.3 | 15 | V |
| dV_{OUT}/dt | Allowed output slew rate | | 50 | V/ns |

Table 5. Total system

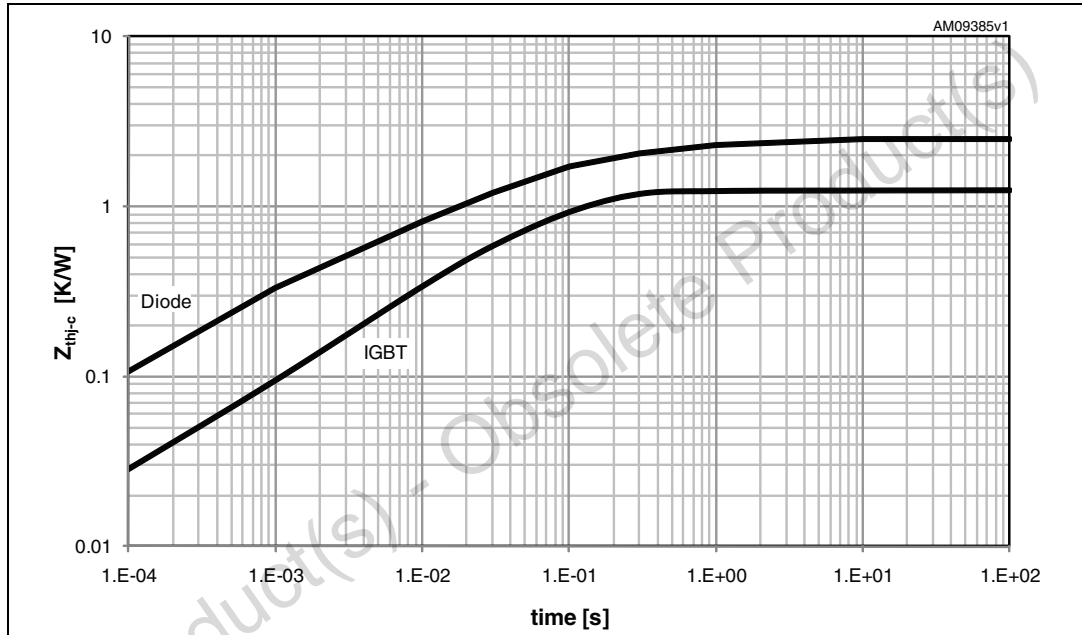
| Symbol | Parameter | Value | Unit |
|-----------|-------------------------------------------------------------------------------------------------------------|------------|------------------|
| V_{ISO} | Isolation withstand voltage applied between each pin and heatsink plate (AC voltage, $t = 60\text{ sec.}$) | 2500 | V |
| T_J | Power chips operating junction temperature | -40 to 150 | $^\circ\text{C}$ |
| T_C | Module case operation temperature | -40 to 125 | $^\circ\text{C}$ |

2.2 Thermal data

Table 6. Thermal data

| Symbol | Parameter | Value | Unit |
|------------|-----------------------------------------------|-------|------|
| R_{thJC} | Thermal resistance junction-case single IGBT | 1.25 | °C/W |
| | Thermal resistance junction-case single diode | 2.5 | °C/W |

Figure 3. Transient thermal impedance IGBT/diode - inverter



3 Electrical characteristics

$T_J = 25\text{ °C}$ unless otherwise specified.

Table 7. Inverter part

| Symbol | Parameter | Test conditions | Value | | | Unit |
|---------------------------------------------------------|---------------------------------------------------------------|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|-------|------|------|------------------------|
| | | | Min. | Typ. | Max. | |
| $V_{CE(sat)}$ | Collector-emitter saturation voltage | $V_{CC} = V_{boot} = 15\text{ V}$, $V_{IN} = 1$ "logic state", $I_C = 30\text{ A}$ | - | 2.1 | 2.7 | V |
| | | $V_{CC} = V_{boot} = 15\text{ V}$, $V_{IN} = 1$ "logic state", $I_C = 30\text{ A}$, $T_J = 125\text{ °C}$ | - | 1.9 | | |
| I_{CES} | Collector-cut off current ($V_{IN}^{(1)} = 0$ "logic state") | $V_{CE} = 550\text{ V}$, $V_{CC} = V_{Boot} = 15\text{ V}$ | - | | 500 | μA |
| V_F | Diode forward voltage | $V_{IN} = 0$ "logic state", $I_F = 30\text{ A}$ | - | | 2.5 | V |
| Switching on/off (inductive load) ⁽¹⁾ | | | | | | |
| t_{on} | Turn-on time | $V_{DD} = 410\text{ V}$, $V_{CC} = V_{boot} = 15\text{ V}$, $V_{IN} = 1$ "logic state" (see Table 13) $I_C = 30\text{ A}$ (see Figure 4 and 5) | - | 440 | - | ns |
| $t_{c(on)}$ | Crossover time (on) | | - | 87 | - | |
| t_{off} | Turn-off time | | - | 280 | - | |
| $t_{c(off)}$ | Crossover time (off) | | - | 130 | - | |
| t_{rr} | Reverse recovery time | | - | 60 | - | μJ |
| E_{on} | Turn-on switching losses | | - | 680 | - | |
| E_{off} | Turn-off switching losses | - | 760 | - | | |
| $di/dt_{(on)}$ | Rate of rise of on-state current | $V_{DD} = 410\text{ V}$, $V_{CC} = V_{boot} = 15\text{ V}$, $V_{IN} = 1$ "logic state" (see Table 13), $I_C = 70\text{ A}$ (see Figure 4 and 5) | - | 2000 | - | $\text{A}/\mu\text{s}$ |
| t_{on} | Turn-on time | $V_{DD} = 410\text{ V}$, $V_{CC} = V_{boot} = 15\text{ V}$, $V_{IN} = 1$ "logic state" (see Table 13) $I_C = 30\text{ A}$, $T_J = 125\text{ °C}$ (see Figure 4 and 5) | - | 550 | - | ns |
| $t_{c(on)}$ | Crossover time (on) | | - | 110 | - | |
| t_{off} | Turn-off time | | - | 410 | - | |
| $t_{c(off)}$ | Crossover time (off) | | - | 200 | - | |
| t_{rr} | Reverse recovery time | | - | 85 | - | μJ |
| E_{on} | Turn-on switching losses | | - | 1025 | - | |
| E_{off} | Turn-off switching losses | | - | 1400 | - | |
| $di/dt_{(on)}$ | Rate of rise of on-state current | $V_{DD} = 410\text{ V}$, $V_{CC} = V_{boot} = 15\text{ V}$, $V_{IN} = 1$ "logic state" (see Table 13) $I_C = 70\text{ A}$, $T_J = 125\text{ °C}$ (see Figure 4 and 5) | - | 1750 | - | $\text{A}/\mu\text{s}$ |

1. t_{ON} and t_{OFF} include the propagation delay time of the internal drive. $t_{C(ON)}$ and $t_{C(OFF)}$ are the switching time of IGBT itself under the internally given gate driving condition. Parameter values take into account a 20 nH stray inductance.

Figure 4. Switching time test circuit

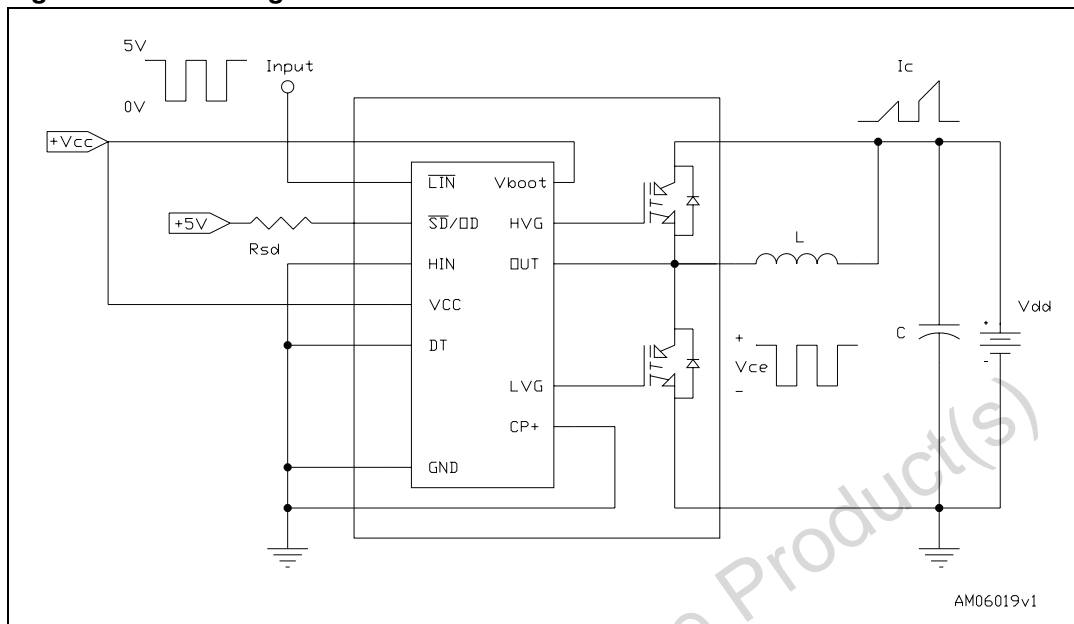
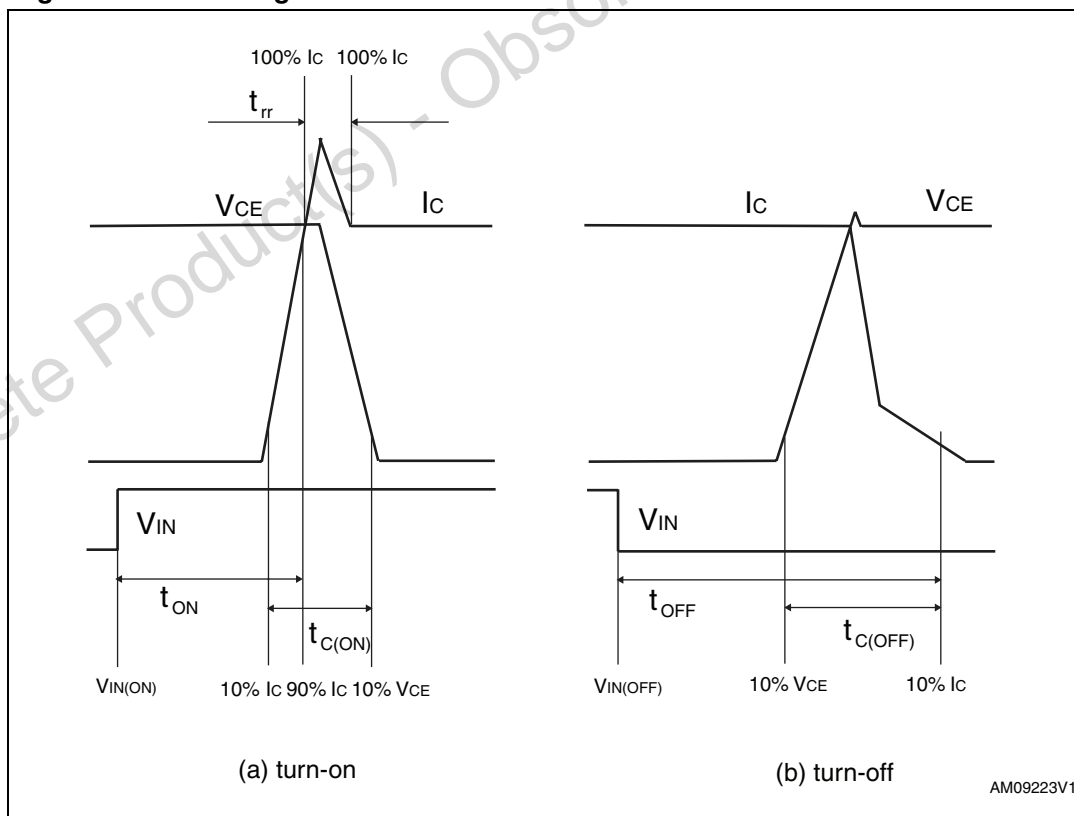


Figure 5. Switching time definition (1)



1. "Switching time definition" refers to HIN inputs (active high). For LIN inputs (active low), VIN polarity must be inverted for turn-on and turn-off.

3.1 Control part

Table 8. Low voltage power supply ($V_{CC} = 15\text{ V}$ unless otherwise specified)

| Symbol | Parameter | Test conditions | Min. | Typ. | Max. | Unit |
|-----------------|---------------------------------------|----------------------------------------------------------------------------------------------------------------------|------|------|------|---------------|
| V_{CC_hys} | V_{CC} UV hysteresis | | 1.2 | 1.5 | 1.8 | V |
| V_{CC_thON} | V_{CC} UV turn ON threshold | | 11.5 | 12 | 12.5 | V |
| V_{CC_thOFF} | V_{CC} UV turn OFF threshold | | 10 | 10.5 | 11 | V |
| I_{qccu} | Undervoltage quiescent supply current | $V_{CC} = 10\text{ V}$ $\overline{SD}/OD = 5\text{ V}$; $\overline{LIN} = 5\text{ V}$; $HIN = 0$, $CIN = 0$ | | | 200 | μA |
| I_{qcc} | Quiescent current | $V_{CC} = 15\text{ V}$ $\overline{SD}/OD = 5\text{ V}$; $\overline{LIN} = 5\text{ V}$ $HIN = 0$, $CIN = 0$ | | | 1 | mA |
| V_{ref} | Internal reference voltage | | 0.5 | 0.54 | 0.58 | V |

Table 9. Bootstrapped voltage ($V_{CC} = 15\text{ V}$ unless otherwise specified)

| Symbol | Parameter | Test conditions | Min. | Typ. | Max. | Unit |
|-----------------|-----------------------------------------|--------------------------------------------------------------------------------------------------------------------|------|------|------|---------------|
| V_{BS_hys} | V_{BS} UV hysteresis | | 1.2 | 1.5 | 1.8 | V |
| V_{BS_thON} | V_{BS} UV turn ON threshold | | 10.6 | 11.5 | 12.4 | V |
| V_{BS_thOFF} | V_{BS} UV turn OFF threshold | | 9.1 | 10 | 10.9 | V |
| I_{QBSU} | Undervoltage V_{BS} quiescent current | $V_{BS} < 9\text{ V}$ $\overline{SD}/OD = 5\text{ V}$; \overline{LIN} and $HIN = 5\text{ V}$; $CIN = 0$ | | 70 | 110 | μA |
| I_{QBS} | V_{BS} quiescent current | $V_{BS} = 15\text{ V}$ $\overline{SD}/OD = 5\text{ V}$; \overline{LIN} and $HIN = 5\text{ V}$; $CIN = 0$ | | 150 | 210 | μA |
| $R_{DS(on)}$ | Bootstrap driver on resistance | LVG ON | | 120 | | Ω |

Table 10. Logic inputs ($V_{CC} = 15\text{ V}$ unless otherwise specified)

| Symbol | Parameter | Test conditions | Min. | Typ. | Max. | Unit |
|------------|-----------------------------------------------|--------------------------------|------|------|------|---------------|
| V_{il} | Low logic level voltage | | | | 0.8 | V |
| V_{ih} | High logic level voltage | | 2.25 | | | V |
| I_{HINh} | HIN logic "1" input bias current | $HIN = 15\text{ V}$ | 110 | 175 | 260 | μA |
| I_{HINl} | HIN logic "0" input bias current | $HIN = 0\text{ V}$ | | | 1 | μA |
| I_{LINl} | \overline{LIN} logic "1" input bias current | $\overline{LIN} = 0\text{ V}$ | 3 | 6 | 20 | μA |
| I_{LINh} | \overline{LIN} logic "0" input bias current | $\overline{LIN} = 15\text{ V}$ | | | 1 | μA |
| I_{SDh} | \overline{SD} logic "0" input bias current | $\overline{SD} = 15\text{ V}$ | 10 | 40 | 100 | μA |
| I_{SDl} | \overline{SD} logic "1" input bias current | $\overline{SD} = 0\text{ V}$ | | | 1 | μA |

Table 11. Op amp characteristics ($V_{CC} = 15\text{ V}$ unless otherwise specified)

| Symbol | Parameter | Test condition | Min. | Typ. | Max. | Unit |
|-----------|-----------------------------------|-------------------------------------------------------------|------|------|------|------------|
| V_{io} | Input offset voltage | $V_{ic} = 0\text{ V}$, $V_o = 7.5\text{ V}$ | | | 6 | mV |
| I_{io} | Input offset current | $V_{ic} = 0\text{ V}$, $V_o = 7.5\text{ V}$ | | 4 | 40 | nA |
| I_{ib} | Input bias current ⁽¹⁾ | | | 100 | 200 | nA |
| V_{icm} | Input common mode voltage range | | 0 | | | V |
| V_{OL} | Low level output voltage | $R_L = 10\text{ k}\Omega$ to V_{CC} | | 75 | 150 | mV |
| V_{OH} | High level output voltage | $R_L = 10\text{ k}\Omega$ to GND | 14 | 14.7 | | V |
| I_o | Output short circuit current | Source, $V_{id} = +1$; $V_o = 0\text{ V}$ | 16 | 30 | | mA |
| | | Sink, $V_{id} = -1$; $V_o = V_{CC}$ | 50 | 80 | | mA |
| SR | Slew rate | $V_i = 1 - 4\text{ V}$; $C_L = 100\text{ pF}$; unity gain | 2.5 | 3.8 | | V/ μ s |
| GBWP | Gain bandwidth product | $V_o = 7.5\text{ V}$ | 8 | 12 | | MHz |
| A_{vd} | Large signal voltage gain | $R_L = 2\text{ k}\Omega$ | 70 | 85 | | dB |
| SVR | Supply voltage rejection ratio | vs. V_{CC} | 60 | 75 | | dB |
| CMRR | Common mode rejection ratio | | 55 | 70 | | dB |

1. The direction of input current is out of the IC.

Table 12. Sense comparator characteristics ($V_{CC} = 15\text{ V}$ unless otherwise specified)

| Symbol | Parameter | Test conditions | Min. | Typ. | Max. | Unit |
|---------------|----------------------------------------------------------------------------|------------------------------------------------------------------|------|------|------|--------------|
| I_{ib} | Input bias current | $V_{CP+} = 1\text{ V}$ | - | | 1 | μ A |
| V_{ol} | Open-drain low-level output voltage | $I_{od} = 3\text{ mA}$ | - | | 0.5 | V |
| t_{d_comp} | Comparator delay | \overline{SD}/OD pulled to 5 V through 100 k Ω resistor | - | 90 | 130 | ns |
| SR | Slew rate | $C_L = 180\text{ pF}$; $R_{pu} = 5\text{ k}\Omega$ | - | 60 | | V/ μ sec |
| t_{sd} | Shutdown to high / low side driver propagation delay | $V_{OUT} = 0$, $V_{boot} = V_{CC}$, $V_{IN} = 0$ to 3.3 V | 50 | 125 | 200 | ns |
| t_{isd} | Comparator triggering to high / low side driver turn-off propagation delay | Measured applying a voltage step from 0 V to 3.3 V to pin CINi | 50 | 200 | 250 | |

Table 13. Truth table

| Condition | Logic input (V _I) | | | Output | |
|---------------------------------------------|-------------------------------|-------------------------|-----|--------|-----|
| | $\overline{\text{SD/OD}}$ | $\overline{\text{LIN}}$ | HIN | LVG | HVG |
| Shutdown enable half-bridge tri-state | L | X | X | L | L |
| Interlocking half-bridge tri-state | H | L | H | L | L |
| 0 "logic state" half-bridge tri-state | H | H | L | L | L |
| 1 "logic state" low side direct driving | H | L | L | H | L |
| 1 "logic state" high side direct driving | H | H | H | L | H |

Note: X: don't care

3.1.1 NTC thermistor

Table 14. NTC thermistor

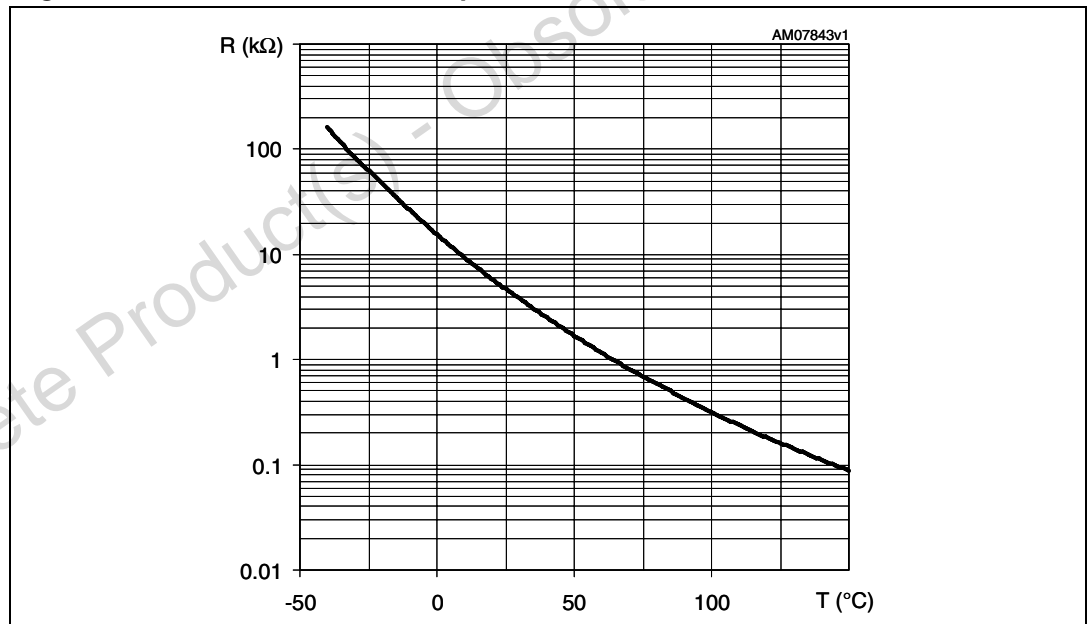
| Symbol | Parameter | Test conditions | Min. | Typ. | Max. | Unit. |
|------------------|-----------------------|------------------------|------|------|------|-------|
| R ₂₅ | Resistance | T _C = 25°C | | 4.7 | | kΩ |
| R ₁₂₅ | Resistance | T _C = 125°C | | 160 | | Ω |
| B | B-constant | T _C = 25°C | | 3950 | | K |
| T | Operating temperature | | -40 | | 150 | °C |

Equation 1: resistance variation vs. temperature

$$R(T) = R_{25} \cdot e^{B \left(\frac{1}{T} - \frac{1}{298} \right)}$$

Where T are temperatures in Kelvins

Figure 6. NTC resistance vs. temperature



3.1.2 Dead time

Figure 7. Dead time and interlocking waveforms definitions

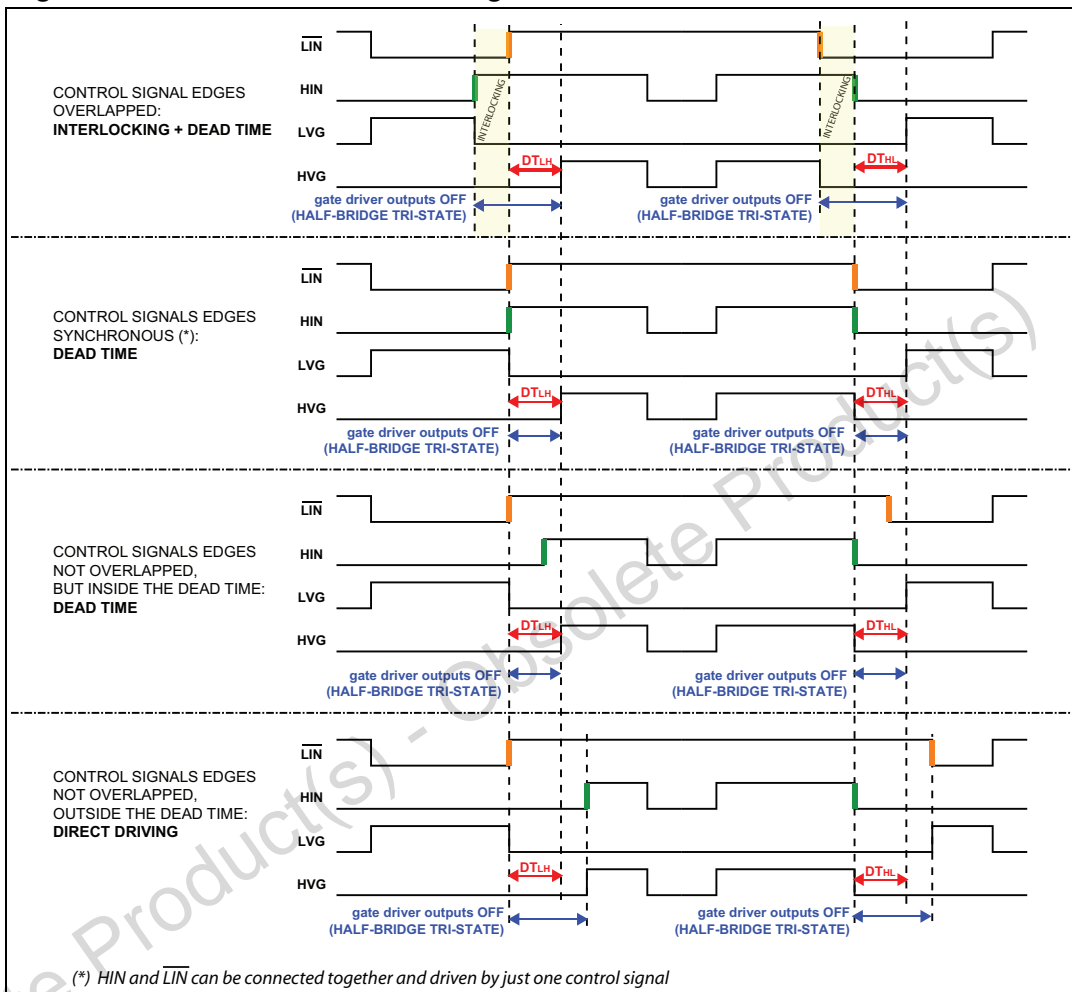
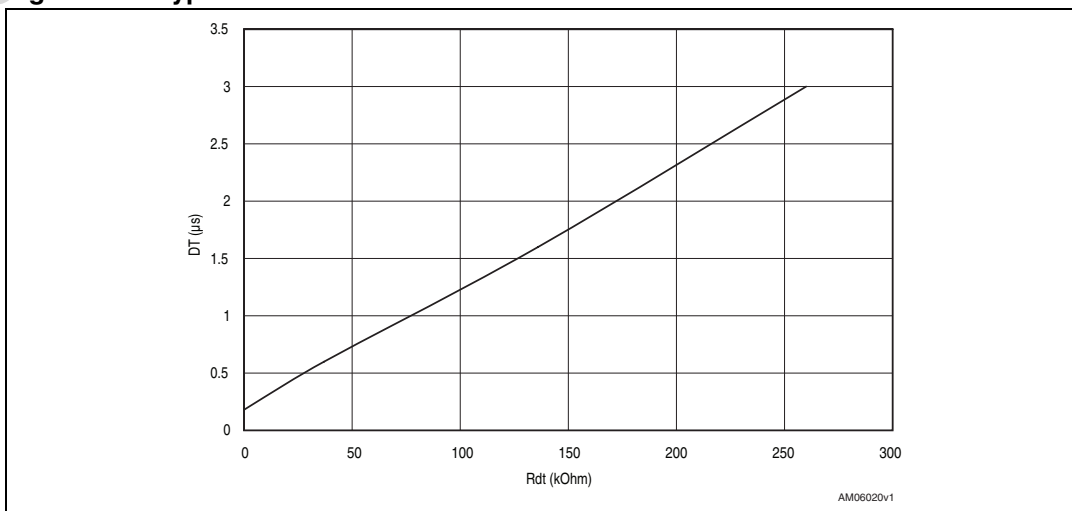


Figure 8. Typical dead time vs. DT resistor value



3.2 Recommendations

- Input signal HIN is active high logic. A 85 kΩ (typ.) pull down resistor is built-in for each high side input. If an external RC filter is used, for noise immunity, pay attention to the variation of the input signal level.
- Input signal $\overline{\text{LIN}}$ is active low logic. A 720 kΩ (typ.) pull-up resistor, connected to an internal 5 V regulator through a diode, is built-in for each low side input.
- To prevent the input signals oscillation, the wiring of each input should be as short as possible.
- By integrating an application specific type HVIC inside the module, direct coupling to MCU terminals without any opto-coupler is possible.
- Each capacitor should be located as nearby the pins of IPM as possible.
- Low inductance shunt resistors should be used for phase leg current sensing.
- Electrolytic bus capacitors should be mounted as close to the module bus terminals as possible. Additional high frequency ceramic capacitor mounted close to the module pins will further improve performance.
- The $\overline{\text{SD}}/\text{OD}$ signal should be pulled up to 5 V / 3.3 V with an external resistor (see [Section 4: Smart shutdown function](#) for detailed info).
- When setting the maximum voltage to be applied between P-N, the internal stray inductance and the maximum di/dt should be considered. Due to both internal and layout stray inductances, the di/dt results in a voltage surges between the DC-link capacitor and the switches during commutations.
- Suggested control supply voltage (V_{CC}): from 13.5 V to 18 V
- Suggested high side bias voltage (V_{BS} between V_{BOOT} and PHASE): from 13 V to 18 V

Table 15. Recommended operating conditions

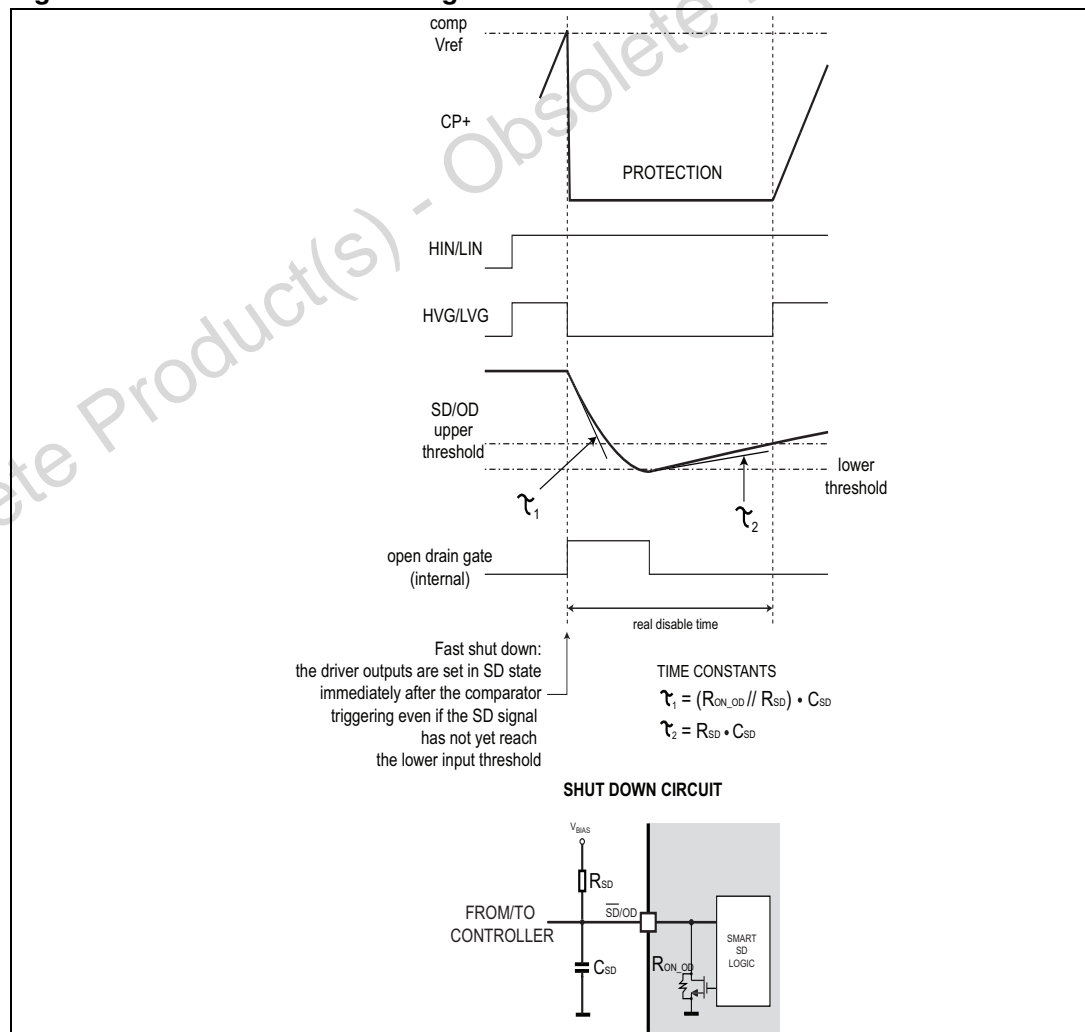
| Symbol | Parameter | Conditions | Value | | | Unit |
|-------------------|------------------------------------|------------------------------------------------------------------------------|-------|------|------|------|
| | | | Min. | Typ. | Max. | |
| V_{PN} | Supply voltage | Applied between P-Nu, Nv, Nw | | 300 | 400 | V |
| V_{CC} | Control supply voltage | Applied between V_{CC} -GND | 13.5 | 15 | 18 | V |
| V_{BS} | High side bias voltage | Applied between V_{BOOTi} - OUT_i for $i = \text{U, V, W}$ | 13 | | 18 | V |
| t_{dead} | Blanking time to prevent Arm-short | For each input signal | 1 | | | μs |
| f_{PWM} | PWM input signal | -40°C < T_{c} < 100°C -40°C < T_{j} < 125°C | | | 20 | kHz |
| T_{c} | Case operation temperature | | | | 100 | °C |

For further details refer to AN3338.

4 Smart shutdown function

The STGIPS35K60L1 integrates a comparator for fault sensing purposes. The comparator non-inverting input (C_{IN}) can be connected to an external shunt resistor in order to implement a simple overcurrent protection function. When the comparator triggers, the device is set in shutdown state and both its outputs are set to low-level leading the half-bridge in tri-state. In the common overcurrent protection architectures the comparator output is usually connected to the shutdown input through a RC network, in order to provide a mono-stable circuit, which implements a protection time that follows the fault condition. Our smart shutdown architecture allows to immediately turn-off the output gate driver in case of overcurrent, the fault signal has a preferential path which directly switches off the outputs. The time delay between the fault and the outputs turn-off is no more dependent on the RC values of the external network connected to the shutdown pin. At the same time the internal logic turns on the open-drain output and holds it on until the shutdown voltage goes below the logic input lower threshold. Finally the smart shutdown function provides the possibility to increase the real disable time without increasing the constant time of the external RC network.

Figure 9. Smart shutdown timing waveforms



Pls refer to [Table 12](#) for internal propagation delay time details.

5 Package mechanical data

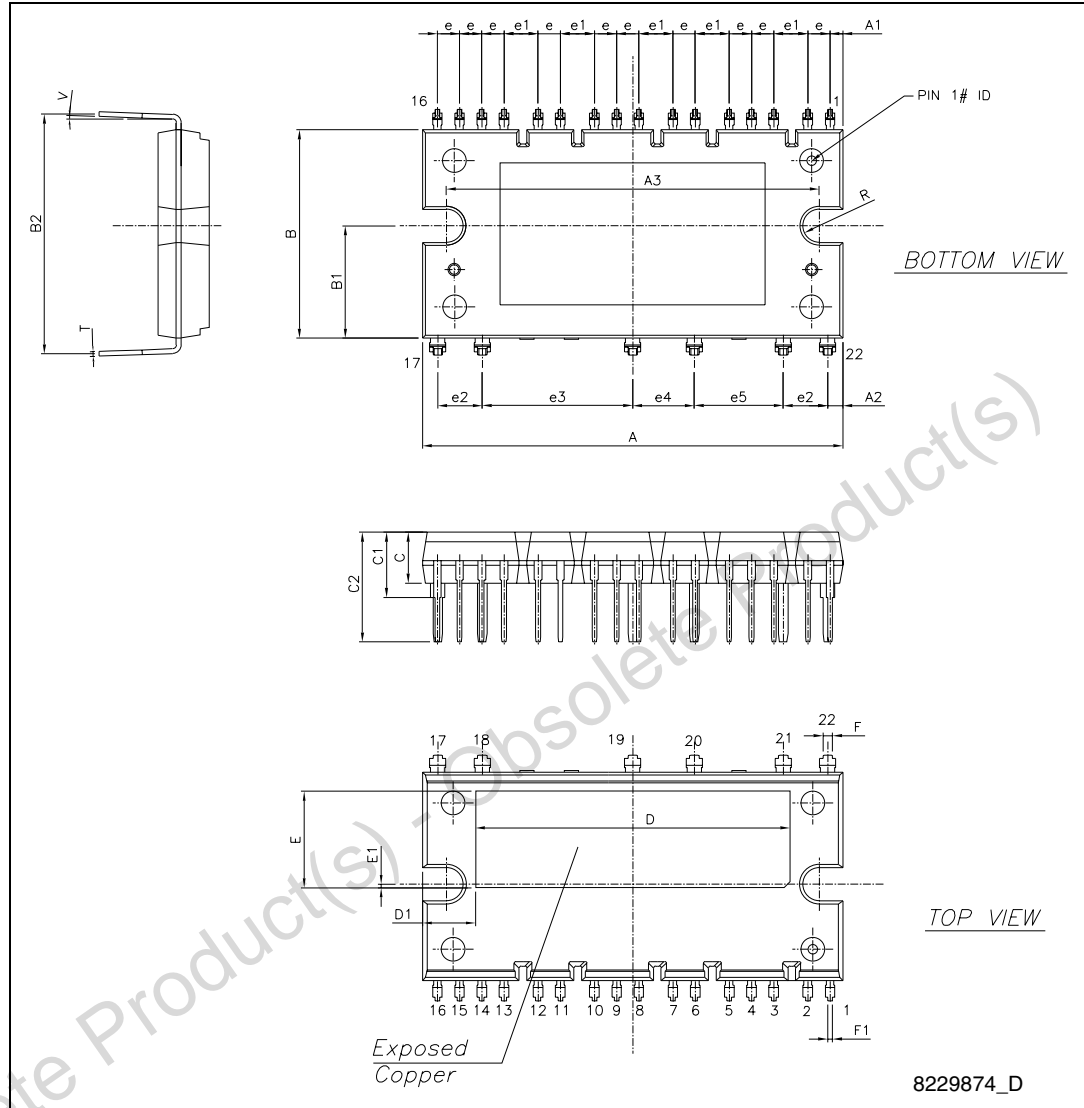
In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status are available at: www.st.com. ECOPACK® is an ST trademark.

Please refer to dedicated technical note TN0107 for mounting instructions.

Table 16. SDIP-22L package mechanical data

| Dim. | mm. | | |
|------|-------|-------|-------|
| | Min. | Typ. | Max. |
| A | 43.90 | 44.40 | 44.90 |
| A1 | 1.15 | 1.35 | 1.55 |
| A2 | 1.40 | 1.60 | 1.80 |
| A3 | 38.90 | 39.40 | 39.90 |
| B | 21.50 | 22.00 | 22.50 |
| B1 | 11.25 | 11.85 | 12.45 |
| B2 | 24.83 | 25.23 | 25.63 |
| C | 5.00 | 5.40 | 6.00 |
| C1 | 6.50 | 7.00 | 7.50 |
| C2 | 11.20 | 11.70 | 12.20 |
| e | 2.15 | 2.35 | 2.55 |
| e1 | 3.40 | 3.60 | 3.80 |
| e2 | 4.50 | 4.70 | 4.90 |
| e3 | 15.70 | 15.90 | 16.10 |
| e4 | 6.30 | 6.50 | 6.70 |
| e5 | 9.20 | 9.40 | 9.60 |
| D | | 33.20 | |
| D1 | | 5.60 | |
| E | | 10.20 | |
| E1 | | 0.40 | |
| F | 0.85 | 1.00 | 1.15 |
| F1 | 0.35 | 0.50 | 0.65 |
| R | 1.55 | 1.75 | 1.95 |
| T | 0.45 | 0.55 | 0.65 |
| V | 0° | | 6° |

Figure 10. SDIP-22L package drawing (dimensions are in mm.)



Obsolete Product(s)

Figure 11. SDIP-22L shipping tube (dimensions are in mm.)

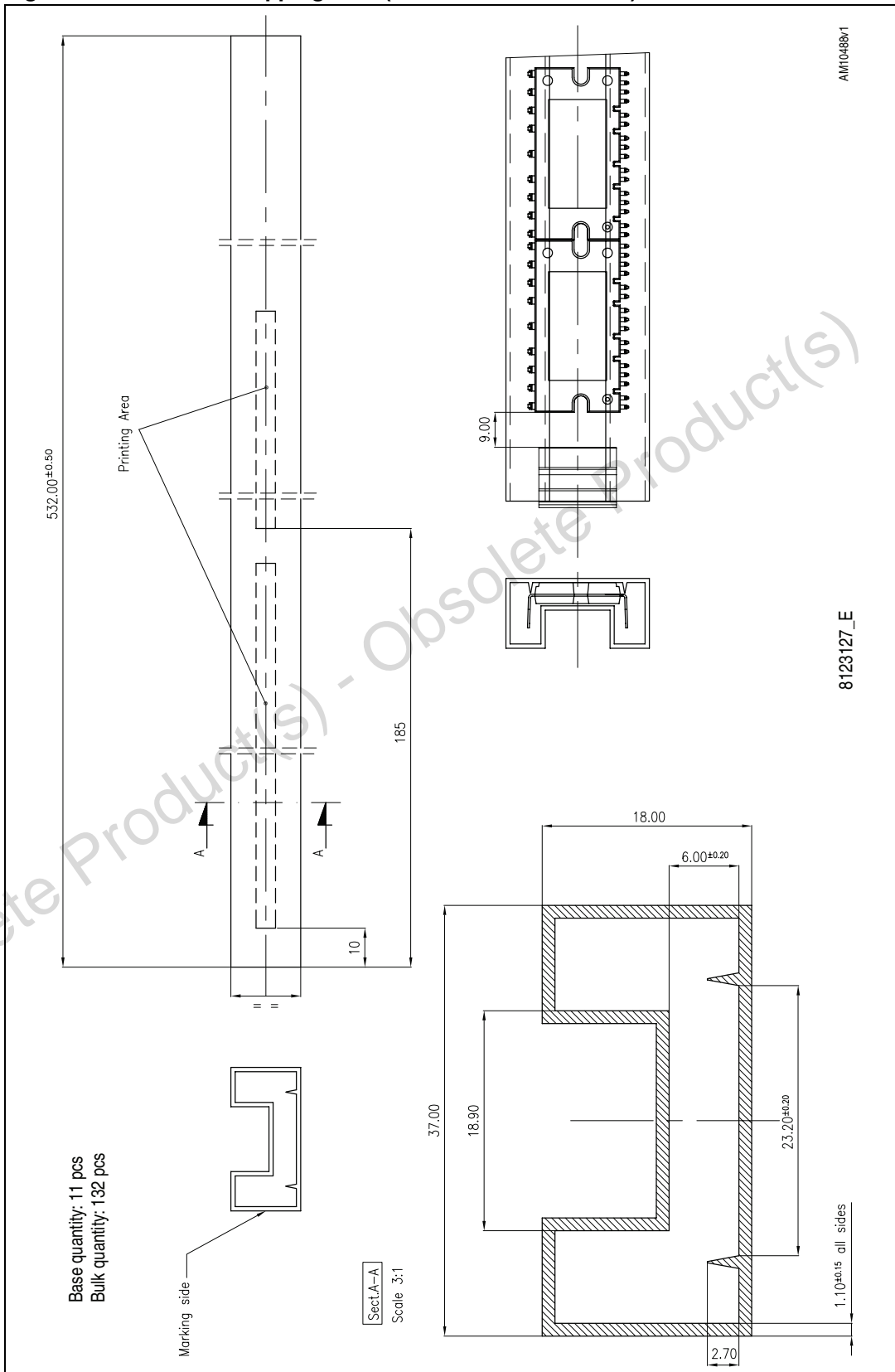
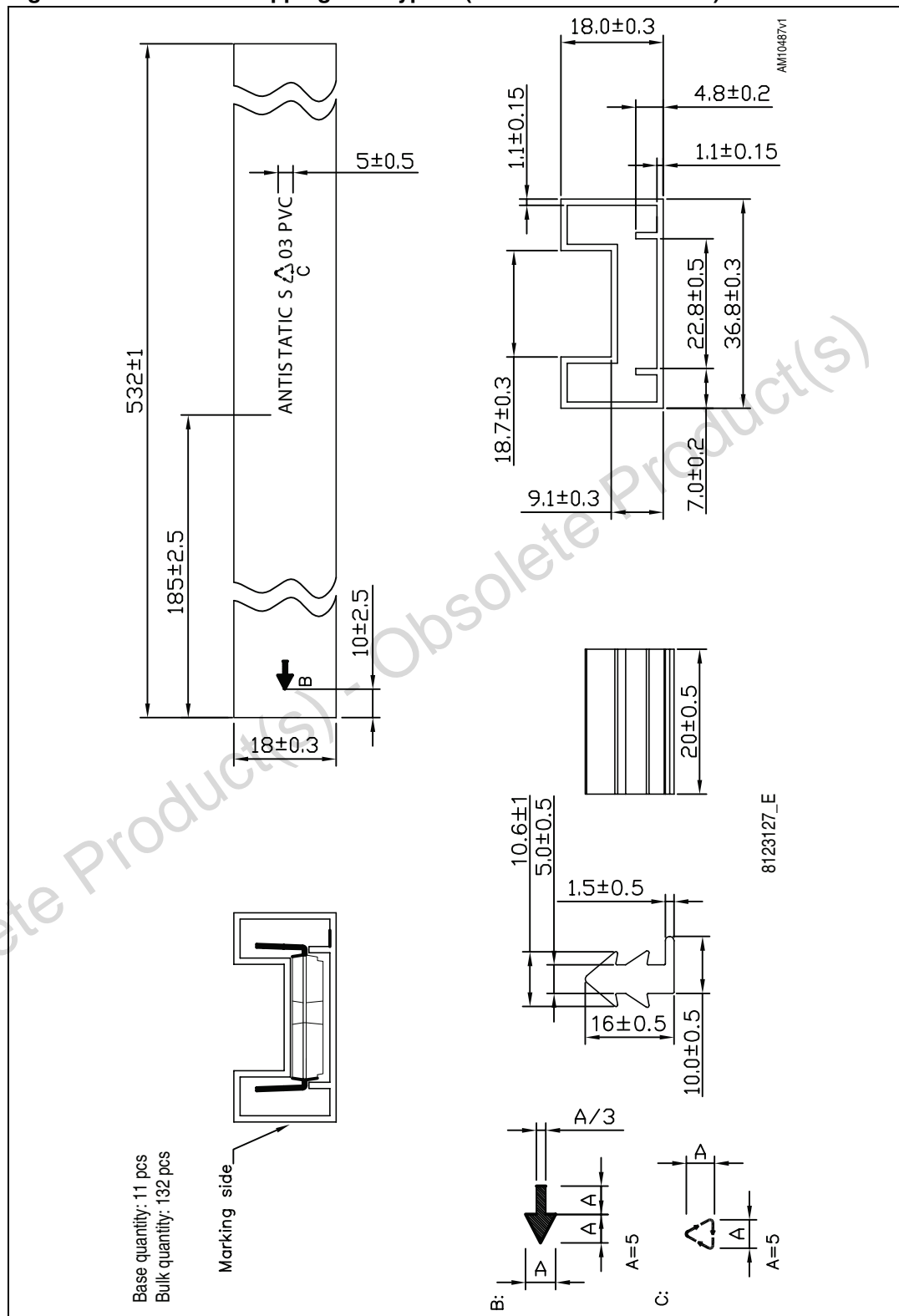


Figure 12. SDIP-22L shipping tube type B (dimensions are in mm.)



6 Revision history

Table 17. Document revision history

| Date | Revision | Changes |
|-------------|----------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 15-Jun-2011 | 1 | Initial release. |
| 24-Jan-2012 | 2 | Added: <i>Figure 11 on page 18.</i> Updated: <i>Figure 10 on page 17.</i> |
| 28-Aug-2012 | 3 | Document status promoted from preliminary data to production data. Added: feature <i>Comparator for fault protection against over temperature and overcurrent on page 1.</i> Modified: Min. and Max. value <i>Table 4 on page 5.</i> |

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