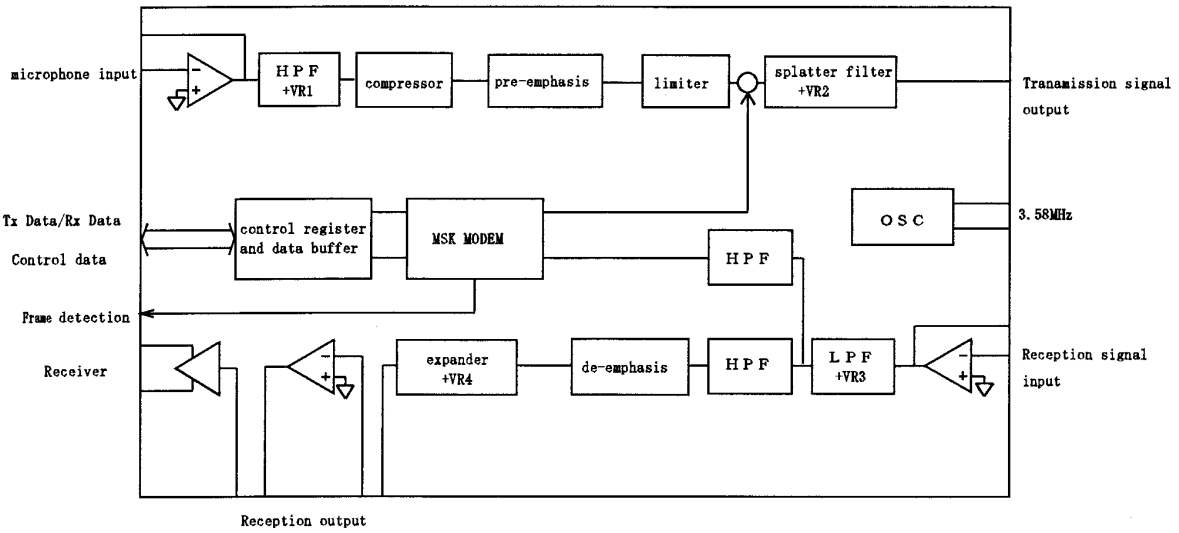
AK2361E

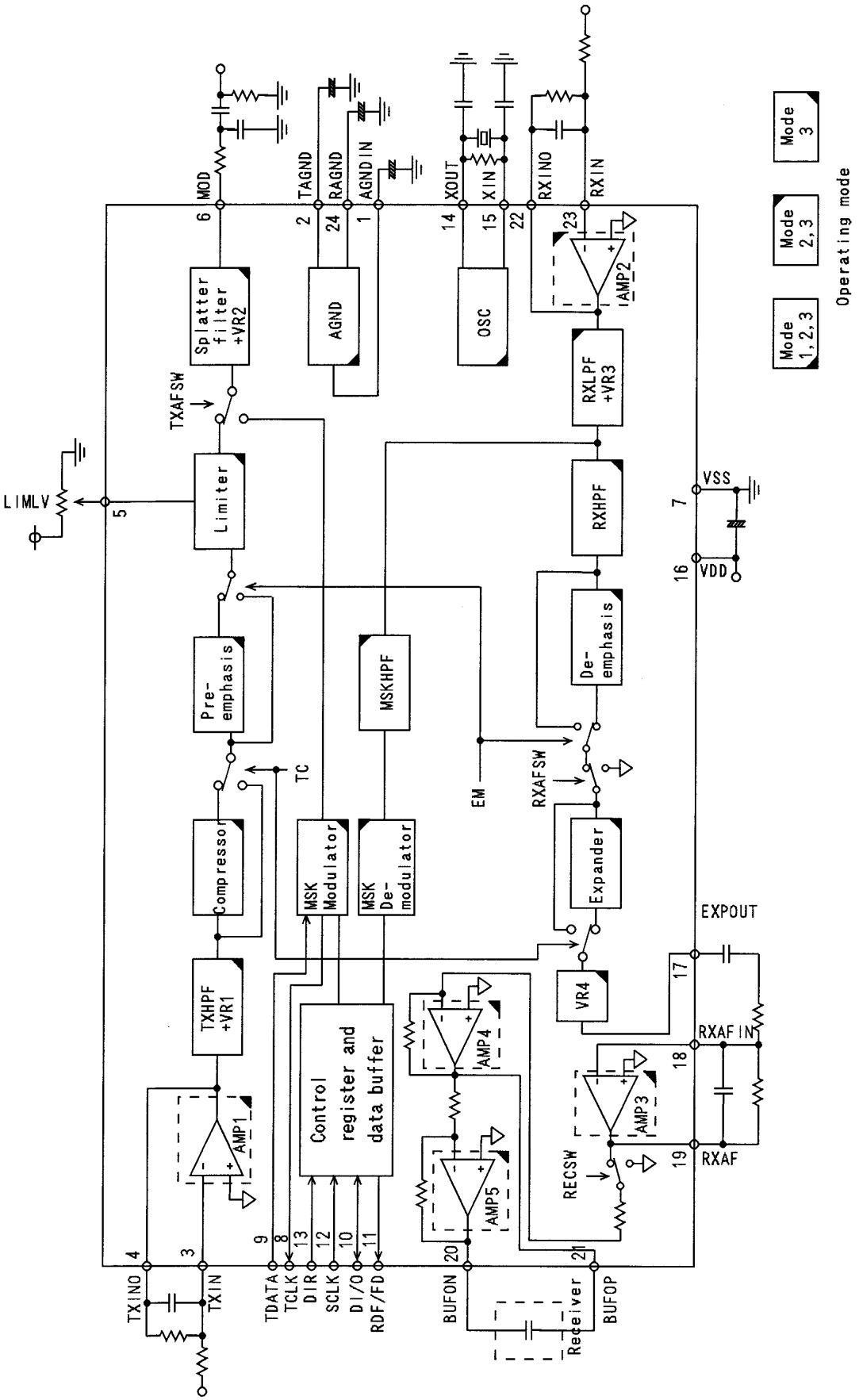
Base-band LSI for European Cordless Telephones(CT1, CT1+)

Features

- ☐ Meets to the specification of the european cordless telephones (CT1, CT1+)
- ☐ Built-in voice filter for cordless telephone, MSK MODEM (2400bps) and COMPANDOR
- ☐ Low / wide operation voltage range (1.9 V to 5.5V)
- ☐ Built-in COMPANDOR output transient response circuit and time constant circuit
- ☐ No external component is needed for COMPANDOR
- ☐ Built-in buffer amplifier for ceramic receiver driving.
- ☐ Built-in electronic volume for microphone sensitivity and modulator/demodulator sensitivity
- ☐ Receiving level switchable in 8 steps (-12 to +9dB)
- ☐ Built-in muting function for voice transmitting and receiving
- ☐ External adjustment for the limiter level
- ☐ Built-in amplifier for transmission and reception gain adjustment
- ☐ Low power CMOS and power-down function
- ☐ Built-in 3.58MHz oscillator circuit
- ☐ Built-in frame detection function for the MSK demodulator
- ☐ Control register and MSK MODEM data buffer controlled by serial interface
- ☐ Few external component is necessary resulting cost reduction and small set size.
- ☐ AK2358E/58F pin compatible
- ☐ Package: 24 pin VSOP

Block Diagram



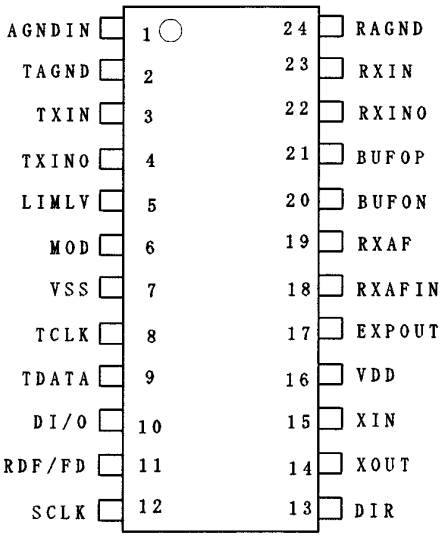

MOD
TAGND
RAGND
AGNDIN
XOUT
XIN
RXINO
RXIN
Splatter filter +VR2
AGND
OSC
AMP2
RXLPF +VR3
TXAFSW
LIMLV
Limiter
RXHPF
VSS
VDD
Pre-emphasis
MSKHPF
De-emphasis
TC
EM
RXAFSW
Compressor
MSK Modulator
MSK De-modulator
Expander
EXPOUT
TXHPF +VR1
Control register and data buffer
AMP4
VR4
RXAFIN
AMP1
AMP3
RECSW
AMP5
RXAF
TXINO
TXIN
TDATA
TCLK
DIR
SCLK
DI/O
RDF/FD
BUFON
Receiver
BUFOP
Mode 3
Mode 2,3
Mode 1,2,3
Operating mode

Description

The AK2361E, a base-band LSI for european cordless telephone (CT1, CT1+), has built-in voice filters, a 2400bps MSK MODEM for data communication, a frame detection circuit and a COMPANDOR for noise reduction.
The CMOS process provides low power operation. Application of 24 pin VSOP package with the feature of significant reduction of external component provides minimum mounting area.
The time constant circuit for the COMPANDOR output transient response is built into the LSI.
Using a 2400bps MSK MODEM for data communication has realized high data reliability and high speed communication at the same time.
This LSI is suitable for cordless system telephones etc. which requires complicated protocol control.
An oscillation circuit with a 3.58MHz crystal oscillator is built in, and no other frequency source is required for the MSK MODEM. The oscillator also can be used for the other DTMF generator etc.
Built-in electronic volumes provided for transmission and reception part realize automatic adjustment of the microphone sensitivity and the modulator/demodulator sensitivity by external EEPROM and microprocessor.
The transmission part is composed of high-pass filter, compressor, pre-emphasis circuit, limiter, MSK modulator, splatter filter, electronic volume control, etc.
The reception part is composed of band pass filter, de-emphasis circuit, buffer amplifier, expander, MSK demodulator, frame detection circuit, electronic volume control, etc.

■ Pin Arrangement

24 pin VSOP



Circuit Configuration

Block	Function
AMP1	The operational amplifier for voice signal transmission gain adjustment and for the filter to eliminate aliasing noise by the SCF(switched capacitor filter) in the following stage. Use an external resistor and capacitor to set the gain less than 30dB and the cut-off frequency to about 10kHz.
TXHPF	The SCF circuit to eliminate the low frequency component less than 300Hz from the transmission voice signal.
Compressor	The circuit to compress the amplitude of the transmission voice signal.
Pre-emphasis	The circuit to emphasis the high-frequency component of the transmission voice signal to improve the S/N of the modulation signal.
Limiter	The amplitude-limiting circuit to suppress the frequency deviation of the modulation signal. The limitation level can be adjusted by applying a DC voltage to the LIMLV pin. If the LIMLV pin is open, the default limitation level is applied.
Splatter filter	The SCF circuit to eliminate the high frequency component higher than 3.4kHz from the limiter output signal or the MSK modulator signal.
MSK modulator	The circuit to generate a 2400bps MSK signal according to the received digital signal logic from the TDATA pin.
AMP2	The operational amplifier to adjust the reception demodulation signal gain and for the filter to eliminate the aliasing noise of the SCF in the following stage. Set the gain to less than 30dB and the cut-off frequency to about 10kHz by external resister and capacitor.
RXLPF	The SCF circuit to eliminate the high frequency component higher than 3.4kHz from the limiter output signal or the MSK modulator signal.
RXHPF	The SCF circuit to eliminate the low frequency component lower than 300Hz from the reception voice signal.
De-emphasis	The circuit to de-emphasis the emphasized signal by pre-emphasis circuit.
Expander	The circuit to expand the signal amplitude compressed by the compressor.

Block	Function
AMP3	The operational amplifier used on the smoothing filter of the reception SCF output. Set the gain to 0dB and the cut-off frequency to about 20kHz by external resister and capacitor.
MSKHPF	The SCF circuit to eliminate the low frequency component lower than 100Hz from the reception MSK signal.
MSK demodulator	The circuit to reproduce the 2400bps receiving data and the clock from the received MSK signal in the RXIN pin.
AMP4 AMP5	The inverting and the non-inverting buffer amplifier to drive the ceramic receiver.
AGND	The circuit to generate the reference voltage for the internal analog signal.
Oscillation circuit	The circuit to oscillate the 3.58 MHz reference clock using an external crystal oscillator and resistor.
VR1	The volume to control the input amplitude of the transmission voice signal. The adjustment range is -8dB to +7dB by 1dB step.
VR2	The volume to control the MOD output amplitude. The adjustment range is -4dB to +3.5dB by 0.5dB step.
VR3	The volume to control the input amplitude of the reception demodulation signal. The adjustment range is -4dB to +3.5dB by 0.5dB step.
VR4	The volume to control the receiving voice amplitude. The adjustment range is -12dB to +9dB by 3dB step.
Control register and data buffer	The control register controls the status of internal switches and internal volumes of the LSI by serial data consists of 2 address bits and 8 data bits. At the start up a power-on-reset circuit works and the default values are set to the control register. (see control register map.) The data buffer stores 8 bits of the MSK receiving data to smooth the signal interface with CPU.

Pin／Function

Pin No.	Pin name	I／O	Function
1	AGNDIN	I	Analog ground input pin. Connect the capacitor to stabilize the analog ground.
2	TAGND	O	Analog ground pin for the transmission system. Connect the capacitor to stabilize the analog ground.
3	TXIN	I	Transmission voice input pin. This is the inverting input pin for AMP1. It composes a microphone amplifier with a external resister and a capacitor.
4	TXINO	O	AMP1 output pin.
5	LIMLV	I	Limitation level adjustment pin. The limitation level can be adjusted by applying a DC voltage to this pin. The default limitation level is adopted if no voltage is applied.

Pin No.	Pin name	I／O	Function
6	MOD	O	Output pin of the modulated transmission signal. A load impedance larger than 10kΩ can be driven.
7	VSS	—	Negative power supply pin.
8	TCLK	O	Clock output pin for the MSK data transmission. A 2.4kHz clock is put out by setting the internal register TDE to "0". If the register is set to "1", it goes "H" level.
9	TDATA	I	MSK transmission data input pin. Data are latched synchronizing with the TCLK rising edge.
10	DI/O	I／O	Serial data input and output pin.
11	RFD/FD	O	MSK signal reception flag output and Frame detection signal output pin. This pin puts out two types of information, depending on the status of the internal register FSL. If FSL is "1", it is MSK signal reception mode, so the pin reaches low after 8 bits of the MSK reception signal have been written to the data register. If FSL is "0", it is the frame detection signal output mode, so the low pulse is put out after a frame pattern is detected.
12	SCLK	I	Clock input pin for serial data I/O.
13	DIR	I	Serial data I/O control pin.
14	XOUT	I	Crystal oscillator connection pin. The reference clock IC is generated by connecting a 3.58MHz crystal oscillator parallel to a 1MΩ resistor between this pin and XIN pin. In case of external clock operation, connect XOUT pin to VSS and apply the clock to XIN.
15	XIN	O	Crystal oscillator connection pin.
16	VDD	—	Positive power supply pin.
17	EXPOUT	O	Expander output pin.
18	RXAFIN	I	Reception voice input pin. This is the inverting input of AMP3. It composes a smoothing filter by external resistor and capacitor.
19	RXAF	O	Reception voice output pin. This is the output pin of AMP3. A load impedance more than 10kΩ can be driven.
20 21	BUFON BUFOP	O O	Receiver amplifier output pins. Connect the ceramic receiver between these two pins.
22	RXINO	O	AMP2 output pin.
23	RXIN	I	Demodulated receiving signal input pin. This is the inverting input of AMP2. It composes a prefilter with external resistor and capacitor.
24	RAGND	O	Analog ground pin for the reception system. Connect the capacitor to stabilize analog ground.

Absolute Maximum Ratings

VSS=0V; Note 1)

Parameter	Symbol	min	max	Unit
Power supply voltage: (VDD)	VA+	-0.3	6.5	V
Input current (except the power supply pins)	I_{IN}	-	±10	mA
Analog input voltage	V_{INA}	-0.3	(VA+)+0.3	V
Digital input voltage	V_{IND}	-0.3	(VA+)+0.3	V
Storage temperature	Tstg	-55	130	℃

Note 1): All voltages with respect to the VSS pin.

Warning: Operation at or beyond these limits may result in permanent damage to the device. Normal operation is not guaranteed at these extremes.

Recommended Operating Conditions

VSS=0V; Note 1)

Parameter		Symbol	min	typ	max	Unit
Operation temperature		Ta	-10		70	℃
Power supply voltage: (VDD)		VD+	1.9	2.0	5.5	V
Analog reference voltage		AGND		1/2VD+		V
Current consumption	Mode 0	Idd0		0.1	0.8	mA
	Mode 1	Idd1		0.9	1.9	
	Mode 2	Idd2		1.5	2.9	
	Mode 3	Idd3		5.0	10	

Note 1): All voltages with respect to the VSS pin.

Analog Characteristics

f=1kHz, TC="1", EM="1", VR1 to VR4=0dB:unless otherwise specified,
0dBm=0.775Vrms
0dBx=-5dBm at AVDD=2V Note 8)

1) TX system

Parameter		min	typ	max	Unit
Standard input level	@TXINO		-10		dBx
Absolute gain	TXINO→MOD Note 1)	2.0	3.5	5.0	dB
Limiter level	MOD 1kHz Note 1) No external R Adjustment range by external R	-4.5	-3.5	-2.5 -2.5	dBx
Compressor linearity	TXINO→MOD Note 1) 2) TXINO=-44dBx TXINO=-50dBx	 -20 -24	 -17.0 -20.0	 -14 -16	dB
Noise without input	TXINO→MOD Note 1) 3)			-36.5	dBm
Compressor distortion	TXINO→MOD TXINO=-10dBx			-35	dB
Transmission MSK signal level	@MOD Note 1) 1.2kHz signal output	-4.5	-3.5	-2.5	dBx
Transmission MSK signal distortion	@MOD Note 1) 1.2kHz signal output			-32	dB

2) RX system

Parameter		min	typ	max	Unit
Standard input level	@RXINO		-10		dBx
Absolute gain	RXINO→BUFON, BUFOP Note 1)	-1.5	0	+1.5	dB
Expander linearity	RXINO→BUFON, BUFOP Note 1) 4) RXINO=-25dBx RXINO=-30dBx	 -33.0 -45.0	 -30.0 -40.0	 -27.0 -35.0	dB
Noise with no input	RXINO→BUFON, BUFOP Note 1) 3)			-70	dBm
Expander distortion	RXINO→RXAF RXINO=-5dBx			-35	dB
Reception MSK signal level	@RXINO 1.2kHz signal output	-14	-7	-1	dBx

3) Overall characteristics

Parameter	min	typ	max	Unit
Absolute gain TXINO→BUFON, BUFOP Note 5) TXINO=-10dBx	-0.5	0	+2.5	dB
Distortion TXINO→BUFON, BUFOP Note 3) 5) TXINO=-10dBx		-50	-43	dB
Crosstalk @BUFON, BUFOP Note 1) 6) Transmission → Reception TXINO=0dBx TC="0"			-60	dBx
Crosstalk @MOD Note 1) 6) Reception → Transmission RXINO=0dBx TC="0"			-56.5	dBx

4) Filter characteristics

Parameter		min	typ	max	Unit
Transmission overall characteristics (See Fig.1)					
TXINO → MOD	100Hz			-40	
TC="0" EM="1"	300Hz	-12	-10.5	-9	
Relative value with 0dB gain	3kHz	8	9.5	11	dB
at 1kHz	3.4kHz	8	9.5	11	
	6kHz			-12	
Reception overall characteristics (See Fig.2)					
RXINO → EXPOUT	100Hz			-4	
TC="0" EM="1"	250Hz		12	13.5	
Relative value with 0dB gain	300Hz	9	10.5		dB
at 1kHz	3.4kHz	-12	-10.5	-9	
	5kHz			-15	

Note 1) With the external circuit shown in the application circuit example.

Note 2) Relative value with 0dB as the MOD output level at the time of input of standard input level (-10dBx) to TXINO.

Note 3) With the C-message filter.

Note 4) Relative value with 0dB as the BUFON, BUFOP output level at the time of input of standard input level (-10dBx) to RXINO.

Note 5) With the external circuit shown in the application circuit example. Further, the AMP2 gain should be -3.5dB, and MOD and RXIN should be in loop connection.

Note 6) TC="0"

Note 7) The dBx is standardized unit valid for various power supply voltages from 1.9 to 5.5V. If the voltage is 2V, 0dBx should be -5dBm. With the other voltage as X [V], 0dBx = -5 + 20 log (X/2) [dBm].

□ Filter characteristics

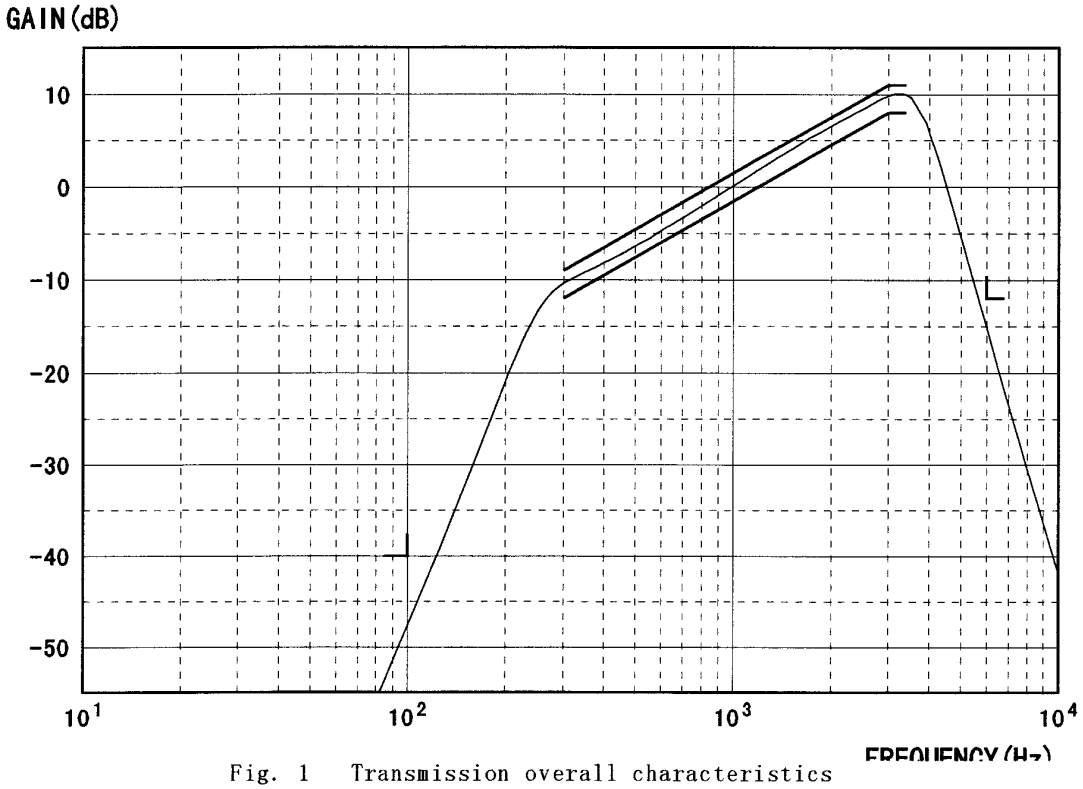


Fig. 1 Transmission overall characteristics

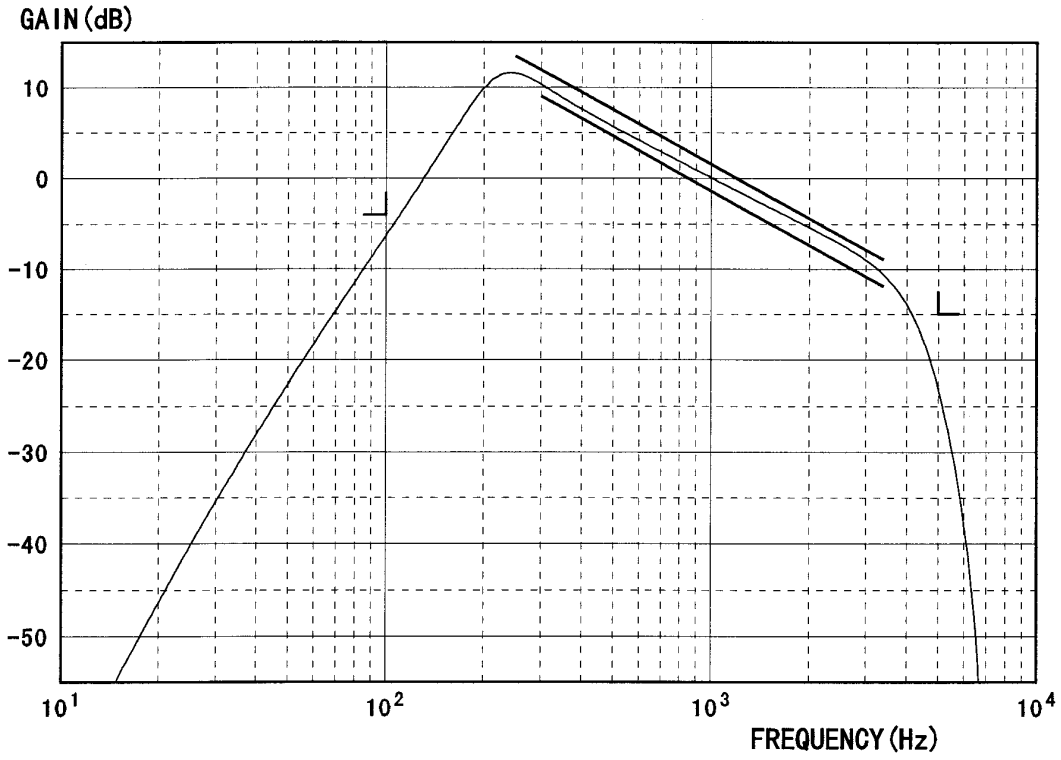
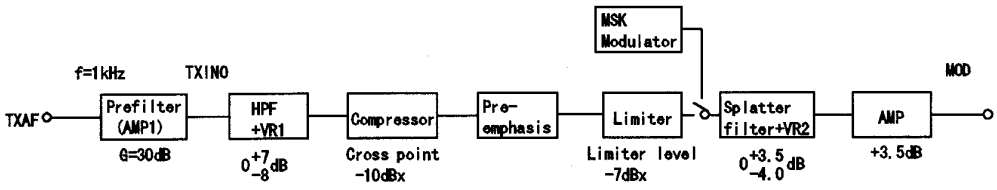
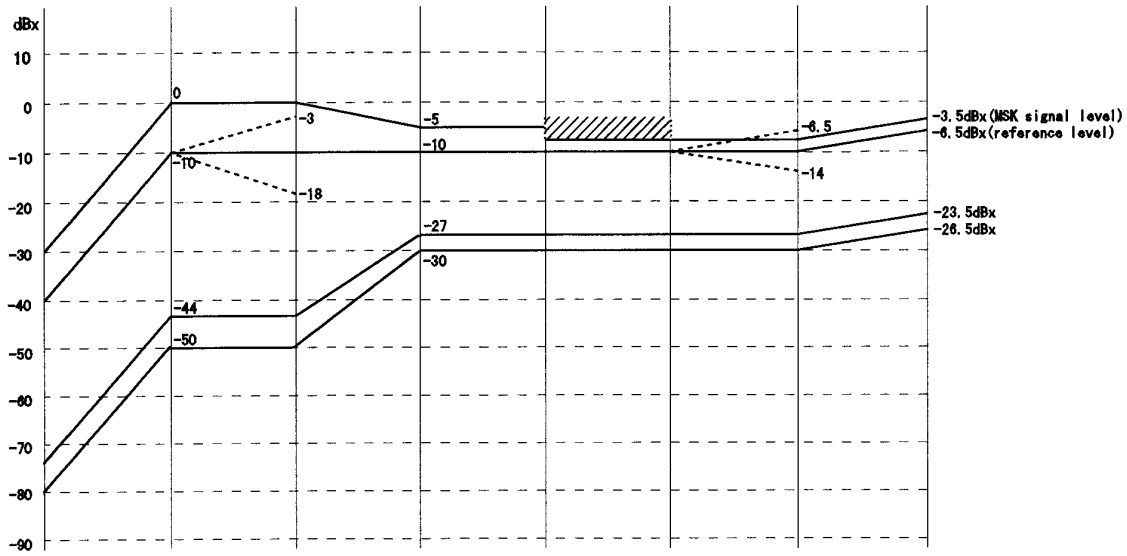


Fig. 2 Reception overall characteristics

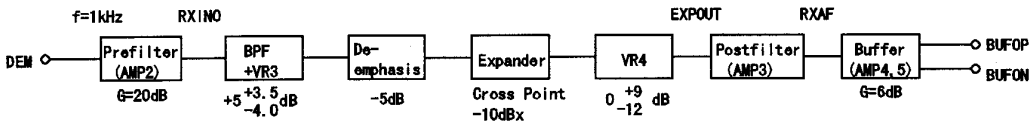
Level Diagram

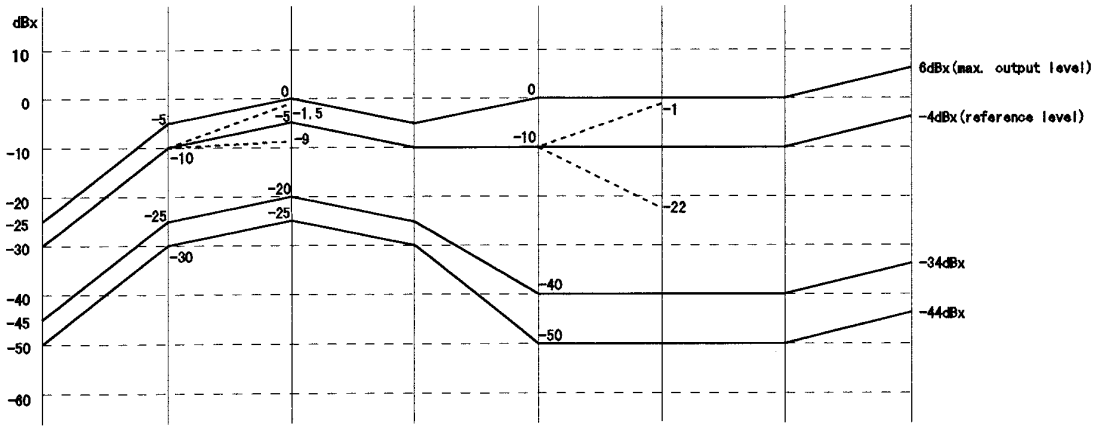
1) TX system





2) RX system





Note) The dBx is standardized unit valid for various power supply voltages from 1.9 to 5.5V. If the voltage is 2V, 0dBx should be -5dBm. With the other voltage as X [V], 0dBx = -5 + 20 log (X/2) [dBm].

Digital Characteristics

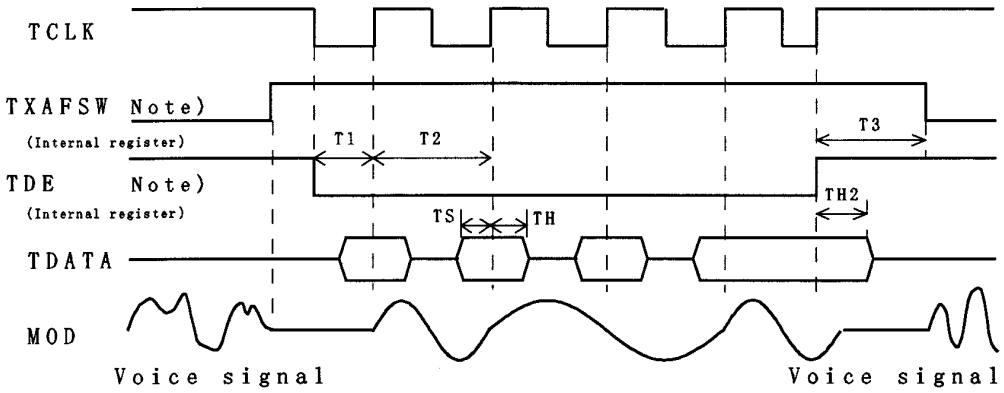
1. DC Characteristics

Parameter	Pin	Symbol	min	typ	max	Unit
High-level input voltage 1	(1)	V_{IH1}	70%VD+			V
Low-level input voltage 1	(1)	V_{IL1}			30%VD+	V
High-level input voltage 2	(2)	V_{IH2}	80%VD+			V
Low-level input voltage 2	(2)	V_{IL2}			20%VD+	V
High-level input current V_{IH}=VD+	(1)(2)	I_{IH}			10	μA
Low-level input current V_{IL}=0V	(1)(2)	I_{IL}	-10			μA
High-level output voltage I_{OH}=0.1mA	(3)	V_{OH}	90%VD+			V
Low-level output voltage I_{OL}=0.6mA	(3)	V_{OL}			0.3	V

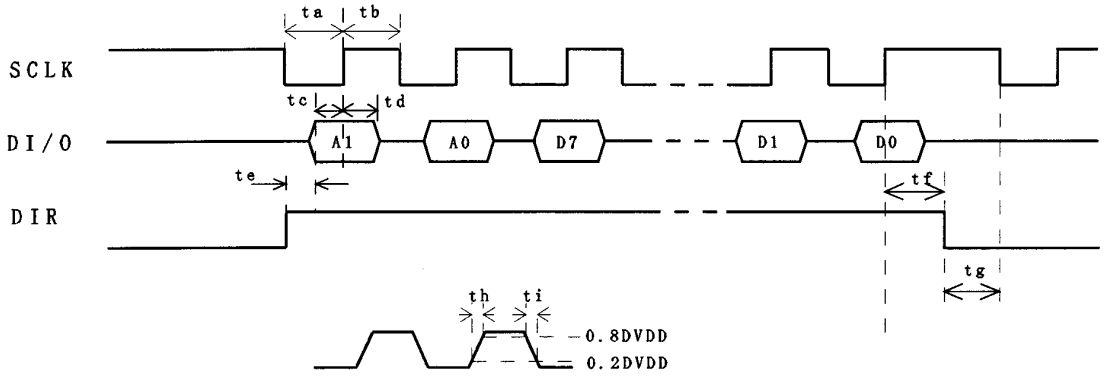
(1) TDATA, DI/O
(2) SCLK, DIR
(3) TCLK, RDF, DI/O

2. AC Characteristics

Parameter	Symbol	min	typ	max	Unit
Master clock frequency	fclk		3.579545		MHz
MSK Modulator timing					
TDE Falling to TCLK Rising	T1		208.3		μs
TCLK period	T2		416.7		μs
TDE Rising to TXAFSW Falling	T3	2			ms
TDATA Set up time	TS	1			μs
TDATA Hold time	TH	1			μs
TDATA Hold time2	TH2	2			μs
MSK Demodulator timing					
RCLK Period & FD pules width	T	402.2	416.7		μs
Serial data input timing					
Clock pulse width 1	ta	500			ns
Clock pulse width 2	tb	500			ns
SDATA Set Up time	tc	100			ns
SDATA Hold time	td	100			ns
DIR Set up time	te	100			ns
DIR Hold time	tf	100			ns
DIR falling to SCLK falling time	tg	100			ns
SCLK/DIR input rising time	th			1	μs
SCLK/DIR input falling time	ti			1	μs
RDF falling to SCLK falling time	tj	100			ns
SCLK rising to RDF falling time	tk	600			ns

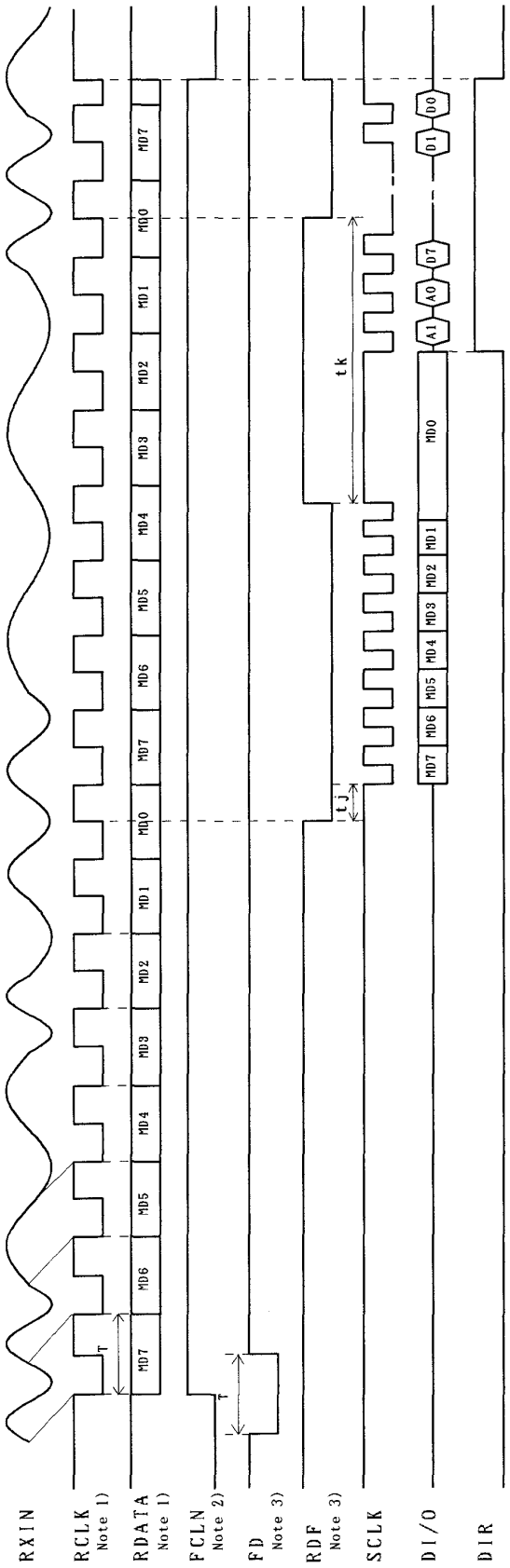


MSK modulator



SCLK/DIR input

Note) The timing to rewrite the internal registers TXAFSW and TDE is synchronized with the falling edge of DIR.



Note 1) Internal node
Note 2) Internal register
Note 3) If the internal register FSL is "0", the status of "FD" is put out from the RDF/FD pin.
If the FSL is "1", the status of "RDF" is put out from the RDF/FD pin.

MSK demodulator

Control Register Map

■ Register composition

	Address		Data							
	A1	A0	D7	D6	D5	D4	D3	D2	D1	D0
Control register 1	0	0	FSL	BS2	BS1	FCLN	-	TDE	TXAF-SW	RXAF-SW
Volume register	0	1	1	1	1	1	RECSW	VR4		
Volume register	1	0	VR2				VR1			
Control register 2 + volume register	1	1	TC	EM	FRPT	-	VR3			
Reception data register			MSK MODEM reception data							

The reception data register is a read only register, and the others are write only registers.
The reception data register has no address information proceeding to the Data.
Set the bits D4 to D7 of volume register address "01" to all "1". If they are set to except all "1", it is changed to test mode. Do not use this test mode.
If the bit D3 of address "00" and D4 of address "11" is written either "0" or "1", setting of AK2361E is not changed.

■ Register map

1) Control register 1

Address		Data							
A1	A0	D7	D6	D5	D4	D3	D2	D1	D0
0	0	FSL	BS2	BS1	FCLN	-	TDE	TXAFSW	RXAFSW
(Default)		1	1	0	0	-	1	0	0

a) Transmission signal control

TDE	TXAFSW	Transmission output
1	0	Voice signal
1	1	Mute
0	1	MSK signal

b) Reception signal control

RXAFSW	RECSW	RXAF	BUFOP/BUFON
1	—	Mute	Mute
0	1	ON	Mute
0	0	ON	ON

c) Frame detection circuit ON/OFF

FCLN	
1	The frame detection function is not used (OFF).
0	The frame detection function is used (ON).

Note) FCLN automatically changes from 0 to 1 when a synchronized frame is detected.

d) Power-down mode

BS2	BS1	Mode name	Voice system + transmission MSK	Reception MSK	Oscillator
1	1	mode 0	OFF	OFF	OFF
0	1	mode 1	OFF	OFF	ON
1	0	mode 2	OFF	ON	ON
0	0	mode 3	ON	ON	ON

e) RDF/FD selection

FSL	
1	The MSK signal reception flag (RDF) is put out from the RDF/FD pin.
0	The frame detection signal (FD) is put out from the RDF/FD pin.

2) Control register 2

Address		Data							
A1	A0	D7	D6	D5	D4	D3	D2	D1	D0
1	1	TC	EM	FRPT	-	VR3			
(Default)		1	1	0	-	1	0	0	0

Data name	Function	
FRPT	Frame detector detection pattern	"1": 1100010011010110 (base unit) "0": 1001001100110110 (portable unit)
EM	Emphasis circuit	"1": Passage (ON) "0": Bypass (OFF)
TC	COMPANDOR circuit	"1": Passage (ON) "0": Bypass (OFF)

3) Volume register

Address		Data							
A1	A0	D7	D6	D5	D4	D3	D2	D1	D0
0	1	1	1	1	1	RECSW	VR42	VR41	VR40
1	0	VR23	VR22	VR21	VR20	VR13	VR12	VR11	VR10
1	1	TC	EM	FRPT	-	VR33	VR32	VR31	VR30

a) VR1 volume control

VR13	VR12	VR11	VR10	Volume gain (dB)
0	0	0	0	−8.0
0	0	0	1	−7.0
0	0	1	0	−6.0
0	0	1	1	−5.0
0	1	0	0	−4.0
0	1	0	1	−3.0
0	1	1	0	−2.0
0	1	1	1	−1.0
1	0	0	0	0
1	0	0	1	+1.0
1	0	1	0	+2.0
1	0	1	1	+3.0
1	1	0	0	+4.0
1	1	0	1	+5.0
1	1	1	0	+6.0
1	1	1	1	+7.0

b) VR2, VR3 volume control

VR23 VR33	VR22 VR32	VR21 VR31	VR20 VR30	Volume gain (dB)
0	0	0	0	−4.0
0	0	0	1	−3.5
0	0	1	0	−3.0
0	0	1	1	−2.5
0	1	0	0	−2.0
0	1	0	1	−1.5
0	1	1	0	−1.0
0	1	1	1	−0.5
1	0	0	0	0
1	0	0	1	+0.5
1	0	1	0	+1.0
1	0	1	1	+1.5
1	1	0	0	+2.0
1	1	0	1	+2.5
1	1	1	0	+3.0
1	1	1	1	+3.5

c) VR4 volume control

VR42	VR41	VR40	Volume gain (dB)
0	0	0	−12
0	0	1	−9
0	1	0	−6
0	1	1	−3
1	0	0	0
1	0	1	+3
1	1	0	+6
1	1	1	+9

Note) By reset, the gain of all volumes are set to 0dB and RECSW bit is changed to "0".

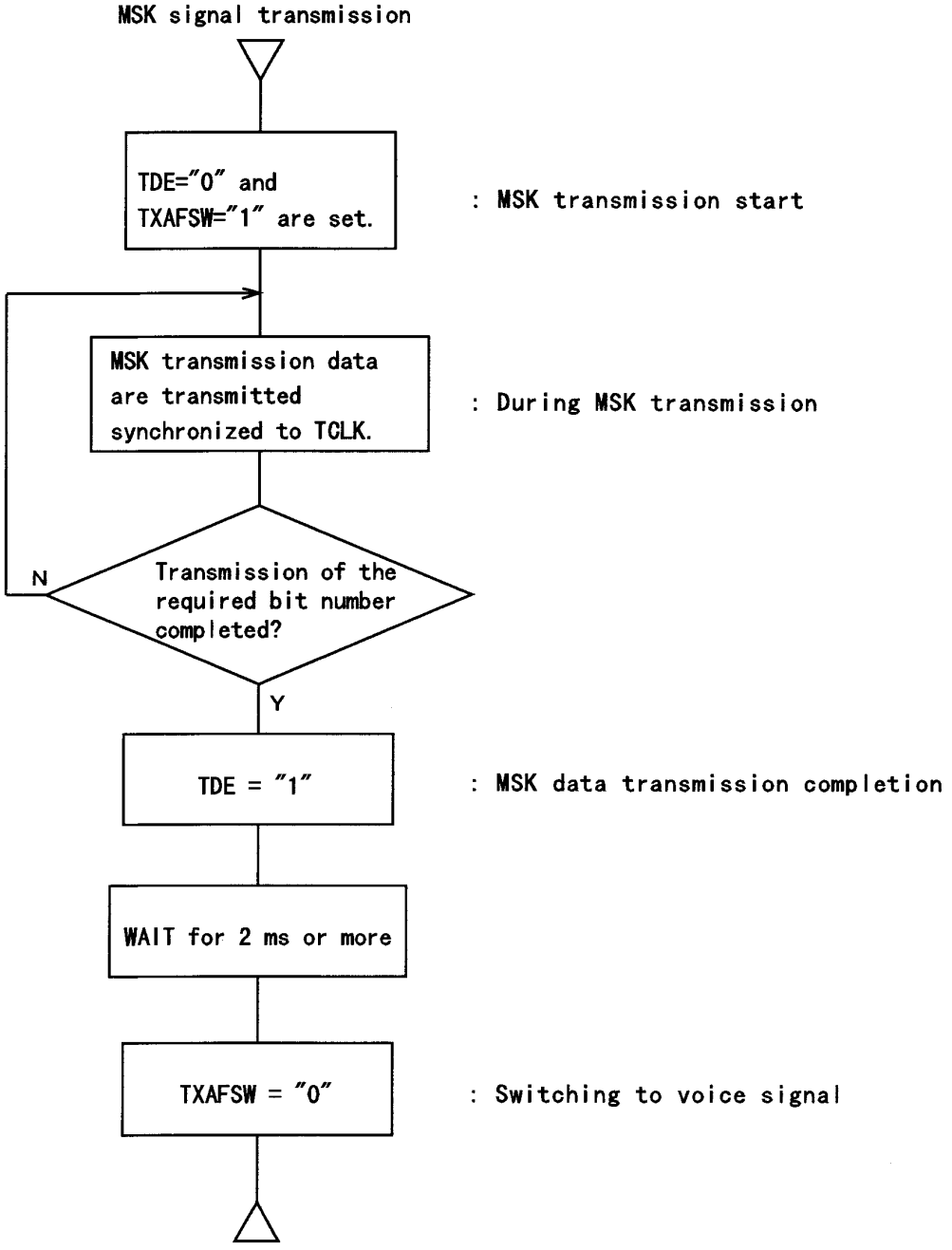
4) MSK MODEM reception data

Data							
D7	D6	D5	D4	D3	D2	D1	D0
RD7	RD6	RD5	RD4	RD3	RD2	RD1	RD0

Data name	Function
RD0	MSK reception data "1":1.2kHz
〜	"0":2.4kHz
RD7	RD7 is the first received data.

MSK Modem

MSK signal transmission flow



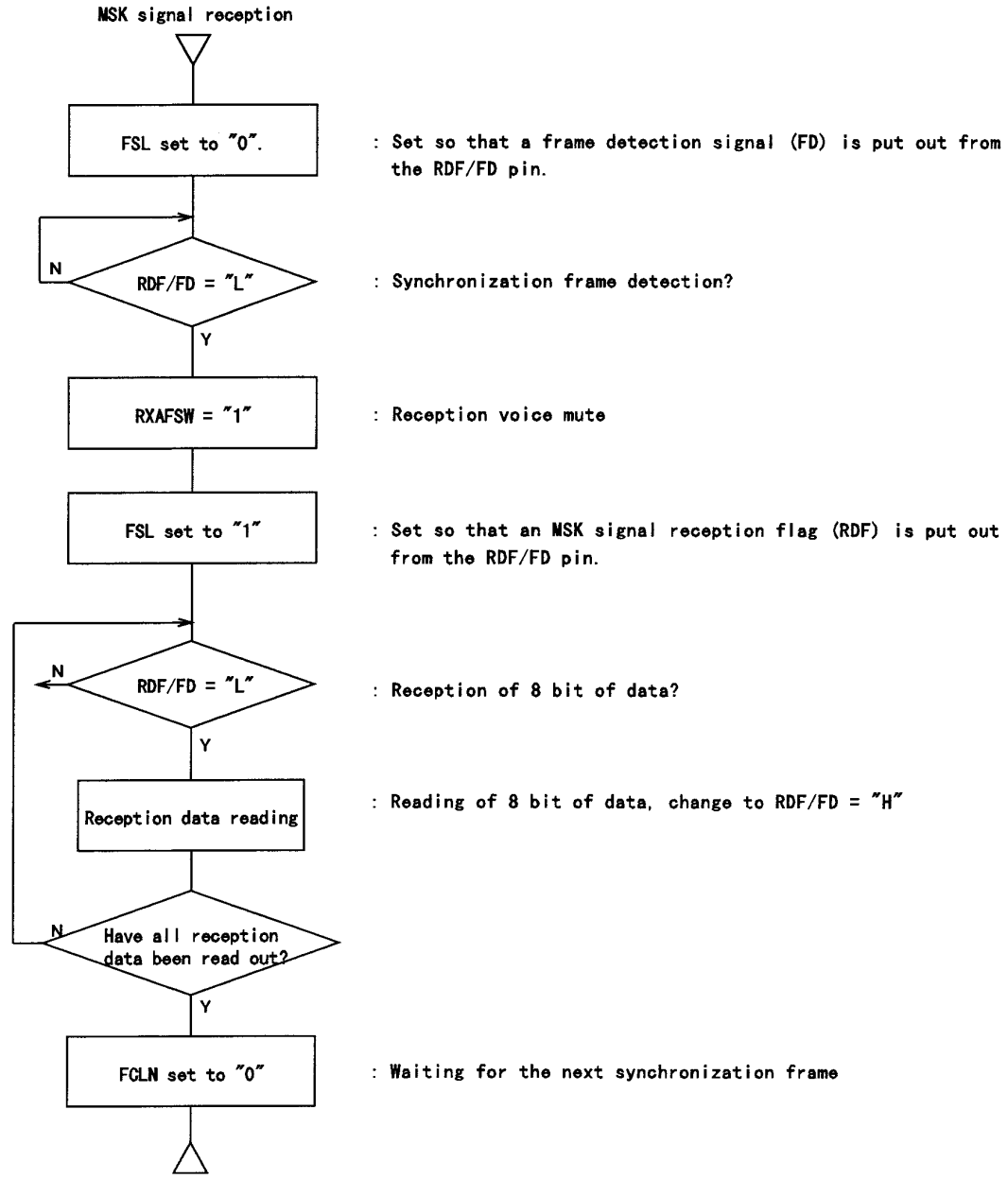
(1) Set the serial register "TDE" to "0" and "TXAFSW" to "1", so that MSK transmission state is provided.

(2) A 2400Hz clock is put out from TCLK. Synchronizing with the rising edge of TCLK, AK2361E reads the MSK transmission data from TDATA pin and put out them to MOD pin.

(3) After the transmission of the necessary number of signal bit, "TDE" of the serial register is set to "1".

(4) Afterwards, before switching to a voice signal transmission mode, wait at least 2ms after "TDE" has set to "1" to complete the MSK signal final bit transmission. Then set TXAFSW register to "0".

MSK Signal Reception



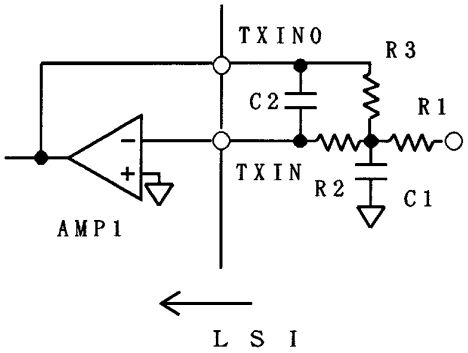
(1) If the internal register "FCLN" is "0", the internal nodes RDATA, RCLK are fixed to "1".
(2) After a synchronization frame is detected, FD goes to "L" during the period "T", then FCLN is set to "1".
(3) RDATA and RCLK put out the data following to the synchronized frame pattern, and these are stored in the internal buffer.
(4) After 8 bit of reception data have been entered to the internal buffer, RDF goes "L".
(5) After the CPU detect that RDF is "L", it puts out 8 clock bits to SCLK, then read 8 bit of reception data from the DI/O pin.
(6) With input of 8 clock bits to SCLK, RDF goes "H".
(7) Afterwards, by repeating the steps (4) and (5) the necessary data bits are read.
(8) After the necessary data have been read, DIR goes "H", "FCLN" is set to "0" via the serial interface, the internal nodes RDATA and RCLK are set to "1", then the system waits for the next synchronization frame.

Application Circuit Example

■Application Circuit

◎AMP 1

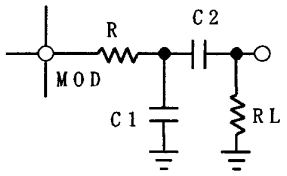
Use as a transmitting microphone amplifier. The gain should be less than 30dB. To eliminate high frequency noise component over than 100kHz from input signal, 1st order or 2nd order anti-aliasing filter is necessary. The following drawing is one example of the 2nd order anti-aliasing filter, which has 30dB gain and 10kHz cut-off frequency.



C1=2200pF
C2=33pF
R1=R2=10k Ω
R3=330k Ω

◎Smoothing filter for MOD output signal

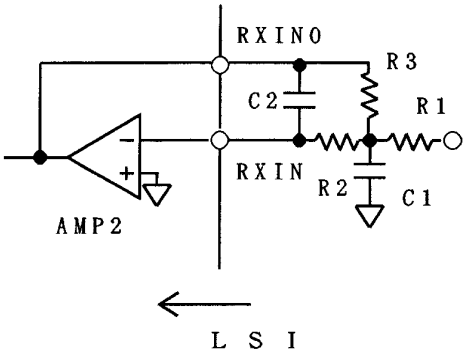
Realize low-pass filter to eliminate 112kHz clock signal component from MOD pin output signal. The following is one example of the 1st order low-pass filter which has 8.7kHz cut-off frequency. 10kΩ of the modulator load resistor(RL) provide 3.3dB signal attenuation.



R=3.9k Ω
C1=4700pF
C2=0.33 μF
RL=10k Ω (Load resistance of MOD)

◎AMP 2

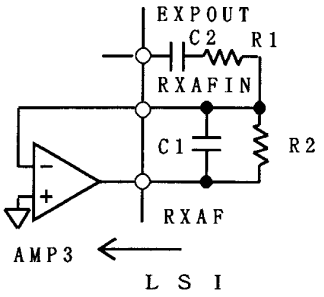
The amplifier for the receiving gain adjustment and anti-aliasing filtering to eliminate high frequency noise component over 100kHz. The gain should be less than 30dB. The following is an example of the 2nd order low pass filter, which has 20 dB gain and 40kHz cut-off frequency.



C1=560pF
C2=27pF
R1=10k Ω
R2=9.1k Ω
R3=100k Ω

◎AMP 3

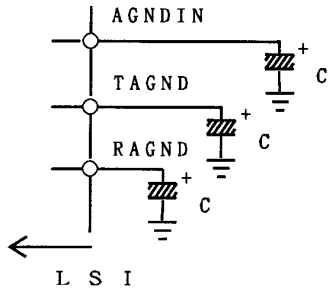
The smoothing filter to eliminate 448kHz clock component from EXPOUT signal is provided by this amplifier. Also it works to adjust the receiving gain. Adding the other pass signal may be possible. The following is one example of the 1st order low-pass filter, which has 0dB gain , 19kHz cut-off frequency.



C1=150pF
C2=0.022 μF
R1=R2=56k Ω

◎AGND stabilizing capacitor

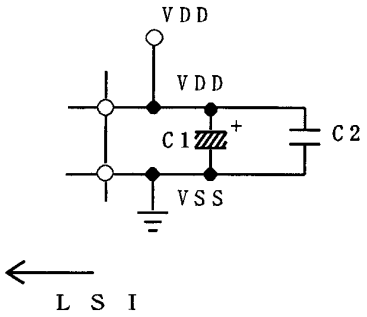
To stabilize the AGND potential, connect capacitors larger than 0.3μF between TAGND pin, RAGND pin and AVSS pin. Also between AGNDIN pin and AVSS pin some capacitor is necessary to reduce the ripple of the power.



C=1 μF

◎VDD stabilizing capacitor

To reduce the noise on VDD, connect capacitors between VDD and VSS.



C1=22 μF
(Aluminium Electrolytic Capacitor)
C2=0.1 μF (Ceramic Capacitor)

◎Crystal oscillator

- Crystal resonator , resistor and capacitors should be connected as shown Fig.3 for on-chip oscillator operation.
- For external clock operation, if the high(H) level of the input clock signal amplitude equals to or is greater than 1.5V, and the low(L) level equals to or is smaller than 0.5V, then connection should be made as shown in Fig.4.
  If the input clock signal amplitude (peak-to-peak) equals to or is smaller than 1V, and equals to or is greater than 200mV, then AC coupling should be as illustrated in Fig.5.

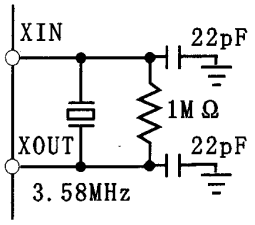


Fig.3

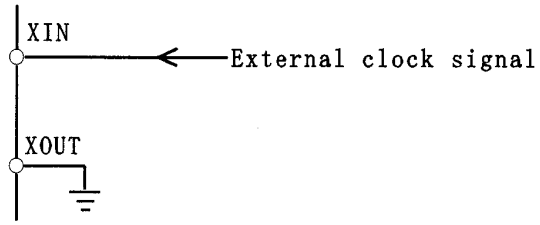


Fig.4

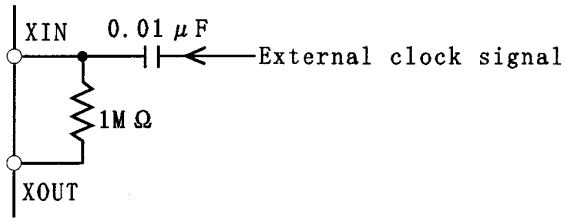
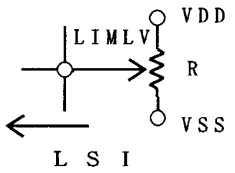


fig.5

◎Limit level adjusting resistor

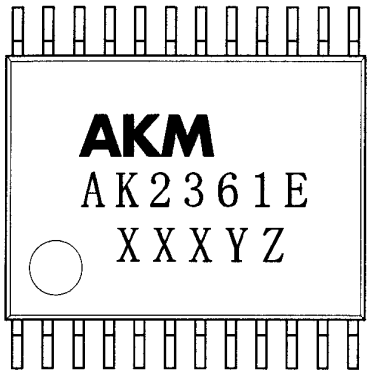
The limiting level can be controlled externally by applying DC voltage to LIMIV pin. Applied DC voltage should be larger than TAGND, then the limiting level is shown as TAGND±Va(V), while Va is the voltage between LIMIV and TAGND. Keeping LIMIV pin open provides default limit level. See following example.



R=50kΩ

Package

■ Marking

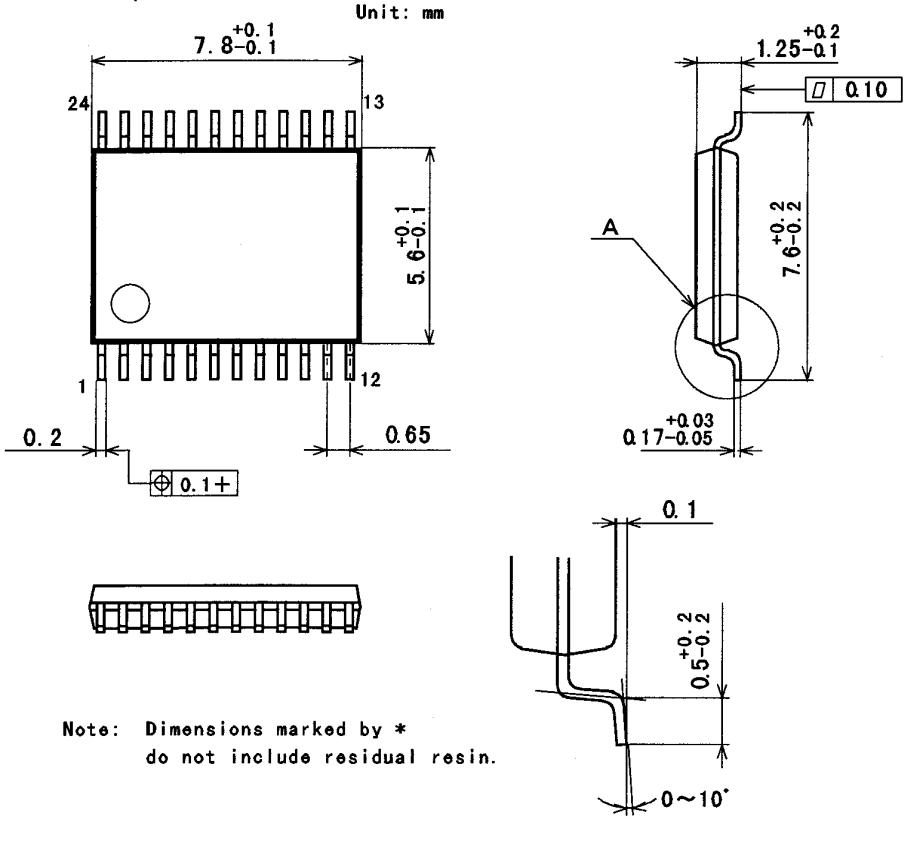


[Contents of XXXYZ]
XXX: Date of manufacture
Last digit of the year, week number of the year as 2 digits
Y: Production lot number
Z: Assembled place

■ Shape and dimensions of the package

24 pin VSOP

Unit: mm



Note: Dimensions marked by * do not include residual resin.

Detail of part A

[Material] Resin: Low-stress type epoxy resin
Lead frame: Cu

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