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**PD69204**

4 Port PSE PoE Manager

**PD69200**

PSE PoE Controller

## Description

Microsemi's™ PD69204 Power over Ethernet (PoE) Manager IC integrates power, analog, and State of the art Logic into a single 56-pin, plastic QFN package. The device is used in Ethernet switches and Midspans to allow network devices to share power and data over the same cable.

PD69204 device is an 4 ports, mixed-signal, high-voltage Power over Ethernet driver. Together with PD69200 external MCU it perform as a PSE system.

Microsemi's™ PoE controller, PD69200, is a cost-effective, pre-programmed MCU designed to implement Enhanced mode.

PD69204/PD69200 chipset supports PoE PD (Powered Device) detection, power-up, and protection according to IEEE standard as well as legacy/pre-standard PD detection.

PD69204/PD69200 chipset provides PD real time protection through the following mechanisms: overload, under-load, over-voltage, over-temperature, and short-circuit and enables operation in a stand-alone mode.

PD69204/PD69200 chipset executes all real time functions as specified in IEEE802.3at High Power ("AT") and PoH (Power Over HDbaseT) standards, including PD detection, "AF", "AT", and PoH classification; using Multiple Classification Attempts (MCA).

PD69204 supports supply voltages between 32V and 57V with no need of additional power supply sources.

A system that powers over 4 pairs can be implemented by combining 2 ports of PD69204 –

enabling an extra feature for simple and low cost high power PD device.

An on-going monitoring of system parameters for the host software is available via communication. Internal thermal protection is implemented in the chip.

PD69204 is a low power dissipation device that uses internal MOSFETs and internal 100mΩ sense resistors.

PD69200 features an ESPI bus for each PD69204

PD69200 is based on Freescale Kinetis\_L family MKL15Z128VFM4 embedded with ARM Cortex™-M0+ core.

PD69200 utilizes I<sup>2</sup>C or UART interface to the host CPU.

PD69200 is designed to support software field upgradable via the communication interface.

PD69204 is available in 56 pin, 8mm x 8mm QFN package.

PD69200 is available in 32 pin, 5mm x 5mm QFN package.

## Features

- ◆ 4 independent channels
- ◆ IEEE802.3af-2003 compliant
- ◆ IEEE802.3at-2009 compliant, including two-event classification
- ◆ Supports Three Event Classification based on PoH
- ◆ Drives 2-pairs power ports or 4-pairs ports
- ◆ Supports pre-standard PD detection
- ◆ Single DC voltage input (32V to 57V)
- ◆ Built in 3.3V and 5V regulators
- ◆ Input voltage out of range protection
- ◆ Wide ambient temperature range: -40°C to +85°C
- ◆ On-chip Over-temperature thermal protection and monitoring
- ◆ Low power dissipation (0.1Ω sense resistor and 0.2Ω MOSFET R<sub>dson</sub> per channel)
- ◆ Includes Reset command pin
- ◆ 4 x direct address configuration pins
- ◆ Continuous port monitoring and system data
- ◆ Configurable load current setting
- ◆ Configurable AT/AF modes
- ◆ Power soft start mechanism
- ◆ Voltage monitoring/protection
- ◆ Internal power on reset
- ◆ Emergency power management supporting four configurable power bank I/Os
- ◆ Advance System Power Management algorithm supports up to 96 physical ports
- ◆ Can be cascaded to up to 12 PoE devices (96 ports)
- ◆ Easy system implementation of PD69204 and PD69208 for multiplications of 4 ports systems. i.e. 12 ports system (consist of 1xPD69208 and 1xPD69204)
- ◆ Supports both UART and I<sup>2</sup>C interfaces to Host CPU
- ◆ Backwards compatible with Microsemi communication protocol used at prior generations
- ◆ LED stream support
- ◆ System OK indication
- ◆ Software download via I<sup>2</sup>C or UART
- ◆ Detailed port status
- ◆ Programmable threshold temperature alarm limit
- ◆ Interrupt out pin for system and port events
- ◆ Forced port power ON function
- ◆ Port power limit setting
- ◆ Port matrix and priority
- ◆ Automatic PoE device type detection
- ◆ MSL3, RoHS compliant

## Applications

- Power over Ethernet (all IEEE compliant 2-pair modes)
- support 4-pair, UPOE (Universal PoE), IEEE802.3bt draft 2.0 Type3 and POH
- Switches/Routers/Midspans
- Industrial automation
- PoE for LED lighting



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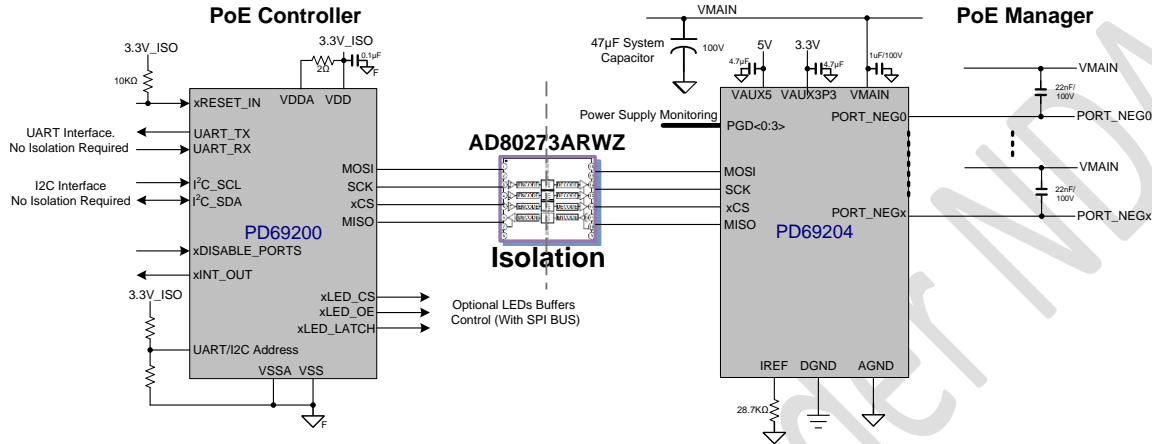
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**Typical Application**



**Figure 1: Typical PoE Application**

**Note:** Fuses per port are not required for use in circuits with total power level of up to 3kW as the PD69204 designed to fulfill limited power source (LPS) requirements per the latest editions of IEC60950-1 and EN60950-1

**PD69204 Absolute maximum ratings**

POE performance is not guaranteed when exceeding the recommended rating . Exposure to any stress in the range between the recommended rating (listed given in the Electrical Characteristics table) and the absolute maximum rating should be limited to a short time period. Exceeding these ratings may impact long-term operating reliability.

**Table 1**

	<b>Min</b>	<b>Max</b>	<b>Units</b>
Supply Input Voltage ( $V_{MAIN}$ ) <sup>(1) (2)</sup>	-0.3	72	V
PORT_NEG[0..3] pins	-0.3	$V_{MAIN}+0.5$	V
VAUX5	-0.3	5.5	V
DRV_VAUX5	-0.3	$V_{MAIN}$	V
VAUX3P3, DVDD	-0.3	4	V
Digital pins: MISO, MOSI, SCK, CS_N, ADDR[3:0], PGD[3:0], RESET_N	-0.3	3.6	V
Junction Temperature		150	°C
Lead Soldering Temperature (40s, reflow)		260	°C
Storage Temperature	-65	150	°C
ESD rating	HBM	2	kV
Surge <sup>(3)</sup>	-1	1	kV



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- Note:**
- (1) Power Sequence Requirement: Vmain>VAUX5>VAUX3P3, DVDD
  - (2) PD69204 EPAD is connected by copper plane on PCB to AGND. AGND is ground for IC.
  - (3) System level common mode 10/700 according to IEC61000-4-5 without external components

For a detailed electrical specification of PD69200 refer to the following datasheets at [www.freescale.com](http://www.freescale.com)

- **Manufacturer:** Freescale
- **Manufacturer part number:** MKL15Z128VFM4

### Applicable Documentation

- ◆ IEEE 802.3at-2009 standard, DTE Power via MDI
- ◆ Microsemi, Serial communication protocol user guide , Catalog Number: PD69200\_UG\_COMM\_PROT
- ◆ Microsemi , Designing 48-port Enhanced PoE System (802.3af/802.3at Compliant) application note, Catalog Number: PD69208\_AN\_211
- ◆ Microsemi , Software Download Algorithm technical note (TN-140) , Catalog Number: 06-0024-081
- ◆ Microsemi , PoE LED stream technical note, Catalog Number: PD69100\_TN\_201
- ◆ Microsemi , PD69208 and PD69200 datasheet, Catalog Number: DS\_PD69208\_PD69200
- ◆ Freescale , Kinetis\_L MKL15Z128VFM4 datasheet
- ◆ Freescale package drawings 98ASA00473D



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**Pin Configuration and Pinout**

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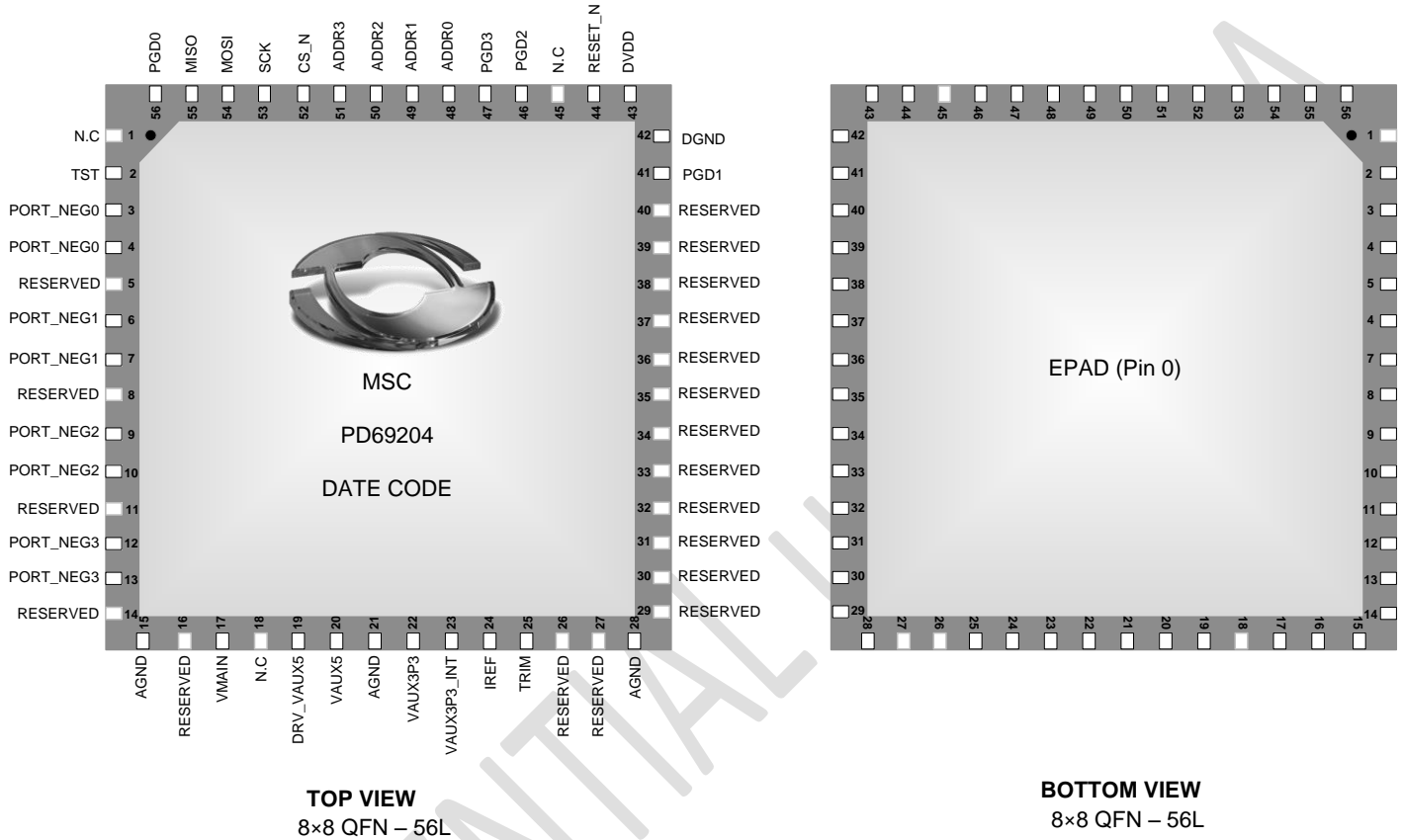


Figure 2: PD69204 Pinout

**Ordering Information**

Table 2

Ambient Temperature	Type	Package	Part Number	Packaging Type	Part Marking
-40 to 85°C	RoHS compliant, Pb-free,MSL3	Plastic QFN 8 mm x 8 mm (56 lead)	PD69204ILQ-TR	Tape and Reel	Microsemi Logo MSC PD69204 YYWWL*
-40 to 85°C	RoHS compliant, Pb-free,MSL3	Plastic QFN 8 mm x 8 mm (56 lead)	PD69204ILQ-TR	Tape and Reel	Microsemi Logo PD69204 F R e4** YYWWAZZ***



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\* YYWWL

YY = Year

WW = Week

L = Lot number

\*\* F R e4

F = FAB Code

R = Product revision code

e4 = 2<sup>nd</sup> level interconnect

\*\*\* YYWWAZZ

YY = Year

WW = Week

A = Assembly location

ZZ = Assembly Lot sequence code

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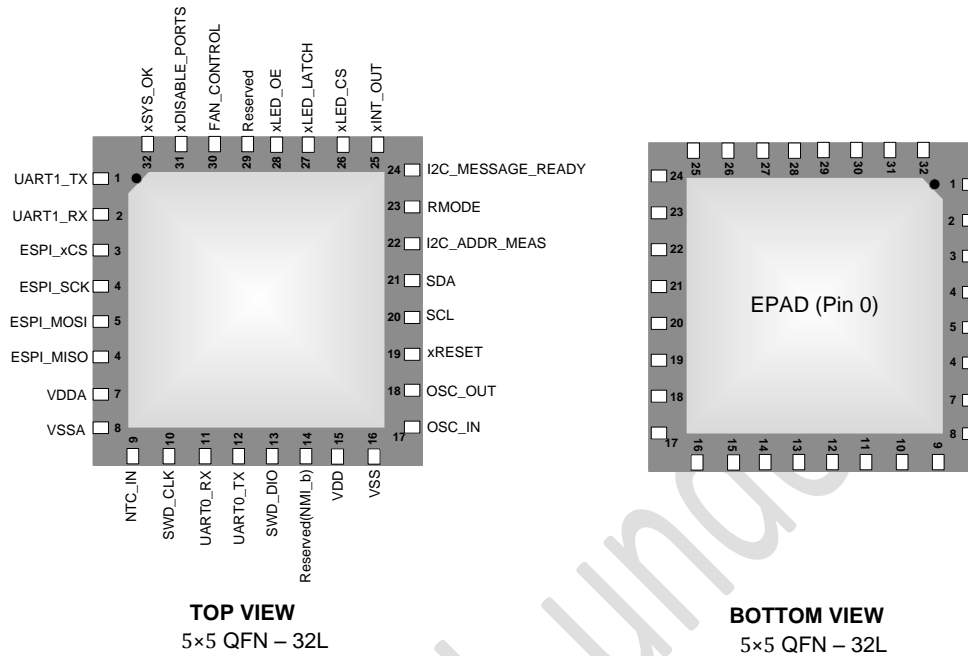


Figure 3: PD69200 Pinout

**Ordering Information**

Table 3

Ambient Temperature	Type	Package	Part Number	Packaging Type	Part marking	Tray Marking
-40 to 85°C	RoHS compliant, Pb-free,MSL3	Plastic QFN 5 mm x 5 mm (32 lead)	PD69200D-VVVVSS	Tray	Microsemi Logo Freescale Logo 69200 M15M7V** XXXXX*** YYYYY****	PD69200-VVVVSS PD-000OG3bb* YYWW

- Note:**
- \*MKTG Product Type / Version / SW Parameters / Operation P/N
  - For latest firmware version available, refer to Microsemi's website or Customer Care Support.
  - Initial burning of controller's firmware is performed in factory. Firmware upgrades can be performed by users using communication interface (see TN-140 ,Catalog Number: 06-0024-081).
  - \*\* Short part number, \*\*\* Mask set, \*\*\*\* Date code



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**PD69204 Pin Description**

Table 4

Pin Number	Pin Designator	Pin Type	Description
0	EPAD		Exposed PAD: Connect to analog ground. A decent ground plane should be deployed around this pin whenever possible (refer to PD69208 Layout Design Guidelines in the HW app note, Catalog Number: PD69208_AN_211)
1	N.C	N/A	Not connected; do not connect externally (leave floating)
2	TST	Digital Input	Test pin for production use only. Keep connected to DGND.
3	VPORT_NEG0	Analog I/O	Negative port0 output
4	VPORT_NEG0	Analog I/O	Negative port0 output
5	RESERVED	N/A	Reserved Pin. do not connect externally
6	VPORT_NEG1	Analog I/O	Negative port1 output
7	VPORT_NEG1	Analog I/O	Negative port1 output
8	RESERVED	N/A	Reserved Pin. do not connect externally
9	VPORT_NEG2	Analog I/O	Negative port2 output
10	VPORT_NEG2	Analog I/O	Negative port2 output
11	RESERVED	N/A	Reserved Pin. do not connect externally
12	VPORT_NEG3	Analog I/O	Negative port3 output
13	VPORT_NEG3	Analog I/O	Negative port3 output
14	RESERVED	N/A	Reserved Pin. do not connect externally
15	AGND	Power	Analog ground
16	RESERVED	N/A	Reserved Pin. do not connect externally
17	VMAIN	Power	Main High Voltage Supply voltage. A low ESR 1 $\mu$ F (or higher) bypass capacitor, connected to AGND, should be placed as close as possible to this pin through low resistance traces
18	N.C	N/A	not connected. do not connect externally
19	DRV_VAUX5	Power	Driven outputs for 5 V external regulation; if internal regulation is used, connect to pin 20. If an external NPN is used to regulate the voltage, connect this pin to "Base".





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20	VAUX5	Power	Regulated 5 V output voltage source; A 4.7 $\mu$ F or higher filtering capacitor should be connected between this pin and AGND. If an external NPN is used to regulate the voltage, connect this pin to the "Emitter" (the "collector" should be connected to V <sub>main</sub> )
21	AGND	Power	Analog ground
22	VAUX3P3	Power	Regulated 3.3V output voltage source. A 4.7 $\mu$ F or higher filtering capacitor should be connected between this pin and AGND. When an external 3.3 V regulator is used, connect it to this pin to supply the chip.
23	VAUX3P3_INT	Power	Connected to VAUX3P3 (pin 22) if internal 3.3 V regulator is used. Leave unconnected (Floating) if external 3.3V regulator is used
24	IREF	Analog Input	Reference resistor pin. Connect a 28.7k $\Omega$ 1% resistor to AGND Use 0.1% resistor in PoH applications
25	TRIM	Test Input	Test Input pin; Keep Connected to VAUX3P3
26	RESERVED	N/A	Reserved Pin. do not connect externally
27	RESERVED	N/A	Reserved Pin. do not connect externally
28	AGND	Power	Analog ground
29	RESERVED	N/A	Reserved Pin. do not connect externally
30	RESERVED	N/A	Reserved Pin. do not connect externally
31	RESERVED	N/A	Reserved Pin. do not connect externally
32	RESERVED	N/A	Reserved Pin. do not connect externally
33	RESERVED	N/A	Reserved Pin. do not connect externally
34	RESERVED	N/A	Reserved Pin. do not connect externally
35	RESERVED	N/A	Reserved Pin. do not connect externally
36	RESERVED	N/A	Reserved Pin. do not connect externally
37	RESERVED	N/A	Reserved Pin. do not connect externally
38	RESERVED	N/A	Reserved Pin. do not connect externally
39	RESERVED	N/A	Reserved Pin. do not connect externally
40	RESERVED	N/A	Reserved Pin. do not connect externally
41	PGD1	Digital I/O	Power good input from system power supply
42	DGND	Power	Digital Ground



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43	DVDD	Power In	Regulated 3.3V for digital circuitry. Connect voltage from pin VAUX3P3 or from external power supply source if used. A 1 $\mu$ F or higher filtering capacitor should be connected between this pin and DGND.
44	RESET_N	Digital Input	Reset input – active low ('0' = reset) An external 10K pull-up resistor should be connected between this pin and DVDD.
45	N.C	N/A	not connected. do not connect externally
46	PGD2	Digital Input	Power good input from system power supply
47	PGD3	Digital Input	Power good input from system power supply
48	ADDR0	Digital Input	SPI Address Bit 0 to set chip address
49	ADDR1	Digital Input	SPI Address Bit 1 to set chip address
50	ADDR2	Digital Input	SPI Address Bit 2 to set chip address
51	ADDR3	Digital Input	SPI Address Bit 3 to set chip address
52	CS_N	Digital Input	SPI bus, chip select
53	SCK	Digital Input	SPI bus, Serial clock Input
54	MOSI	Digital Input	SPI bus, Master Data out/slave in
55	MISO	Digital Output	SPI bus, Master Data in/slave out
56	PGD0	Digital Input	Power good input from system power supply

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**PD69200 Pin Description**

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Table 5

Pin Number	Pin Designator	PIN TYPE	PIN DESCRIPTION
0	EPAD	Thermal	Isolated Thermal PAD, recommended to tie to GND
1	UART1 TX	OUT***	Reserved UART
2	UART1 RX	IN***	Reserved UART
3	ESPI_xCS	OUT	ESPI Bus to PoE Manager SPI chip select (Active Low). CS will be asserted during all SPI frame
4	ESPI_SCK	OUT	ESPI Bus to PoE Manager SPI clock output to PD6920x, and LED stream clock output, set to 1MHz
5	ESPI_MOSI	OUT	ESPI Bus to PoE Manager SPI Master Out Slave In SPI packets will be transmitted on this line
6	ESPI_MISO	IN	ESPI Bus to PoE Manager SPI Master In Slave Out SPI packets will be received on this line
7	VDDA	Supply	Main Supply 3.3v
8	VSSA	GND	Analog ground
9	Analog Input	Analog_IN	Spare Analog input
10	SWD_CLK	DEBUG	Serial Debug Data Bus Clock
11	UART0_RX	IN***	UART receive from host 15 byte protocol commands are received on this line. The baud rate is set to 19200bps. (For more information refer to the Serial Communication Protocol User Guide document - Catalog Number: PD69200_UG_COMM_PROT)
12	UART0_TX	OUT***	UART transmit to host 15 byte protocol reply / telemetry are transmitted on this line. The baud rate is set to 19200bps. (For more information refer to the Serial Communication Protocol User Guide document - Catalog Number: PD69200_UG_COMM_PROT)
13	SWD_DIO	DEBUG	Serial Debug Data Bus
14	PTA4 (NMI_b)	IRQ_Input	Spare, Ext Pull Up must be connected
15	VDD	Supply	Main Supply 3.3v
16	VSS	GND	Digital ground



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Pin Number	Pin Designator	PIN TYPE	PIN DESCRIPTION
17	EXTALO	Oscillator*	Oscillator input - Reserved
18	XTALO	Oscillator*	Oscillator output - Reserved
19	xRESET	IN/OUT**	<p>Host Reset input (Active Low)</p> <ul style="list-style-type: none"> <li>The shortest reset pulse from the host that is required for the PD69200 application is 150uSec.</li> <li>PD69200 can generate self-reset. In this case xRESET pin is driven low by the PD69200 for about 100uSec.</li> <li>It is recommended to connect this pin to a host open drain output with 10Kohm pullup.</li> <li>An 47nF filter capacitor should be connected between this pin to GND, close to the PD69200 device.</li> <li>If this pin is connected to a push/pull driver, a serial resistor of 1.5Kohm must be connected instead of the pullup. The required shortest reset pulse in this case is 300uSec.</li> </ul> <p>For more information about this pin connectivity refer to HW app note, Catalog Number: PD69208_AN_211</p>
20	I2C0_SCL	IN/OUT**	I <sup>2</sup> C Clock from host master. Speed is limited to 400KHz and clock stretching functionality must be implemented in the Host Master. (If the PD69200 is busy it will hold the clock line)
21	I2C0_SDA	IN/OUT**	I <sup>2</sup> C bidirectional data. 15 byte protocol messages are transmitted on this line (For more information refer to the Serial Communication Protocol User Guide document - Catalog Number: PD63000_UG)
22	I2C_ADDR_Meas	Analog_IN	I <sup>2</sup> C address of PD69200 Analog input to determine I <sup>2</sup> C address or UART operation. See I <sup>2</sup> C address selection in Table 12
23	Analog Input	Analog_IN	Reserved Analog input connect to GND
24	xI2C_Message_Ready	OUT	I <sup>2</sup> C Message Ready for read by the Host. PD69200 will assert low this line when it has an answer to the host. This way, the host can poll this line and initiate I <sup>2</sup> C read cycle only when the message is ready. (This pin is active low)



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Pin Number	Pin Designator	PIN TYPE	PIN DESCRIPTION
25	xInt_Out	OUT **	Interrupt output indication This line is asserted low when a pre-configured event is happening. The host configure (through 15 bytes protocol) which event will generate an interrupt. When this event occurs, the xInt_Out is asserted. (This pin is active low).
26	xLed_CS	OUT	Chip select signal for LED stream (This pin is active low)
27	xLED_Latch	OUT	Latch signal for LED stream (This pin is active low)
28	xLED_OE	OUT	Output enable signal for LED stream (This pin is active low)
29	Reserved	IN	Reserved for MPRPD counter (future support). If not used, Connect to VDD.
30	Fan_Control	OUT	Optional FAN control to operate a FAN in case that any PD69204 device temperature is above the temperature alarm threshold. (This pin is active high)
31	xDisable_Ports	IN	Disable all PoE Ports. When this input is asserted low, the PD69200 shutdown all the PoE ports in the system. This pin contains software filter of 400mSec to reject noise and false disable scenarios.
32	xSys_OK / LED System OK	OUT	System validity indication, when system is OK pin state is low. The behavior of this output is controlled by software mask register settings (Mask 0x28). The mask default settings is 0, means this pin indicates valid software and Vmain is in Range. (For more information refer to the Serial Communication Protocol User Guide document - Catalog Number: PD69200_UG_COMM_PROT) (This pin is active low)

**Note:**

1. \*The oscillator pins are reserved and unused. The MCU uses internal clock source set to 47.972MHz +/- 1.5%(max)
2. \*\* Open drain output, requires external pullup. Refer to HW app note : PD69208\_AN\_211 document
3. \*\*\* Weak pullup is recommended. Refer to PD69208\_AN\_211 document
4. All I/Os in this application can sink or source 3mA maximum
5. Initial "x" indicate pin active low



Table 6

Thermal Resistance	Typ	Units	Notes
$\theta_{JA}$	25	°C/W	Mount on PCB of 76x114mm
$\theta_{JL}$	0.5	°C/W	Junction to thermal pad
$\theta_{JC}$	1	°C/W	Junction to top case

**Note:**  $\theta_{Jx}$  numbers assume no forced airflow. Junction Temperature is calculated using  $T_J = T_A + (P_D \times \theta_{JA})$ . In particular,  $\theta_{JA}$  is a function of PCB construction. Stated number above is for a four-layer board in accordance with JESD-51 (JEDEC).

### PD69204 Electrical Characteristics

Unless otherwise specified under conditions, the Min and Max ratings stated below apply over the entire specified operating ratings of the device. Typ values stated are either by design or by production testing at 25°C ambient.

Table 7

Symbol	Parameter	Conditions	Min	Typ	Max	Units
$V_{MAIN}$	Main Supply Voltage	Supports Full IEEE802.3 AF and AT functionality	32		57	V
$V_{PORT\_NEGx}$	Port Output	$V_{MAIN} - V_{PORT\_NEGx}$	0		57	V
$I_Q$	Quiescent Current	$V_{MAIN} \leq 8V$			100	µA
$I_{MAIN}$		Main Power Supply Current @ Operating Mode. $V_{MAIN} = 55V$		14		mA
$V_{AUX5}$	5V Output Voltage	$V_{AUX5} - AGND$	4.5	5	5.5	V
$V_{AUX3P3}$	3.3V Output Voltage	$V_{AUX3P3} - AGND$	3	3.3	3.6	V
$I_{AUX3P3}$	3.3V Output Current	Without external NPN			5	mA
		With external NPN transistor on VAUX5			30	mA
$V_{AUX3P3\_IN}$	3.3V Input Voltage	$V_{AUX3P3} - AGND$	3	3.3	3.6	V
$DV_{DD}$	Digital 3.3V Input Voltage	$DV_{DD} - DGND$	3	3.3	3.6	V
$POR_{TP}$	Power On Reset $DV_{DD}$ Trip Point	$DV_{DD} - DGND$	2.575	2.775	2.975	V



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<b>POR<sub>HYS</sub></b>	Power On Reset DV <sub>DD</sub> Hysteresis	POR <sub>TP</sub> -DGND	0.2	0.25	0.3	V
<b>R<sub>CH_ON</sub></b>	Total Channel Resistance	R <sub>ds_on</sub> + R <sub>sense</sub> + R <sub>bonding</sub>		0.34		Ω
<b>Detection</b>						
<b>V<sub>Oc</sub></b>	Pre Detection Voltage, Open Circuit Voltage	V <sub>MAIN</sub> - V <sub>PORT_NEGx</sub> , open port			7.8	V
<b>V<sub>VALID</sub></b>	Detection Voltage	V <sub>MAIN</sub> - V <sub>PORT_NEGx</sub> , for IEEE802.3 compliant signature resistance (R <sub>SIG</sub> <33K)			9.3	V
<b>I<sub>sc</sub></b>	Short Circuit Current	V <sub>MAIN</sub> - V <sub>PORT_NEGx</sub> =0V		388	408	μA
<b>R<sub>SIG_LOW</sub></b>	Minimum Valid Detection Resistance		15.5		17	KΩ
<b>R<sub>SIG_HIGH</sub></b>	Maximum Valid Detection Resistance		27		32	KΩ
<b>Classification</b>						
<b>V<sub>CLASS</sub></b>	Class Event Output Voltage	V <sub>MAIN</sub> - V <sub>PORT_NEGx</sub> ; 0mA ≤ I <sub>PORT</sub> ≤ 50mA	15.5	18	20.5	V
<b>V<sub>MARK</sub></b>	Mark Event Output Voltage	V <sub>MAIN</sub> - V <sub>PORT_NEGx</sub> ; 0.1mA ≤ I <sub>PORT</sub> ≤ 5mA	7	8.5	10	V
<b>I<sub>CLASS_LIM</sub></b>	Class event current limitation	V <sub>MAIN</sub> - V <sub>PORT_NEGx</sub> =0V	51	70	100	mA
<b>I<sub>MARK_LIM</sub></b>	Mark event current limitation	V <sub>MAIN</sub> - V <sub>PORT_NEGx</sub> =0V	51	70	100	mA
	Classification Current Thresholds	Class 0 Class 1 Class 2 Class 3 Class 4 Class Error	0 8 16 25 35 51		5 13 21 31 45 100	mA
<b>Port Real Time Protection</b>						
<b>T<sub>RISE</sub></b>	Turn on rise time	From 10 % to 90 % of the voltage difference at the V <sub>PORT_NEGx</sub> in POWER_ON state from the beginning of POWER_UP	15			μS



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<b>I<sub>INRUSH</sub></b>	Output current in POWER_UP state	$C_{LOAD} \leq 180\mu F$ (Note 1)	400	425	450	mA
<b>T<sub>INRUSH</sub></b>	Inrush Time				65	mS
<b>I<sub>PORT</sub></b>	Output Operating Current	802.3af 802.3at PoH	10 10 10		360 627 967	mA
<b>I<sub>CUT</sub></b>	Overload Current	802.3af 802.3at PoH (Note 2)	360 627 967	375 645 995	390 663 1023	mA
<b>T<sub>CUT</sub></b>	Overload Time Limit		62	64	66	mS
<b>I<sub>LIM</sub></b>	Port Current Limit	802.3af 802.3at PoH	400 702 990	425 850 1150	450 892 1200	mA
<b>T<sub>LIM</sub></b>	Port Current Limit Time	$V_{MAIN} - V_{PORT\_NEGx} < 30V$	1	2	3	mS
<b>I<sub>UDL</sub></b>	DC Disconnect Under-load Current	2 Pairs	5	7.5	10	mA
		4 Pairs (for each 2 pair)	2.5	3.75	5	mA
<b>T<sub>MPDO</sub></b>	PD Maintain Power Signature Dropout Time Limit		322	324	326	mS
<b>T<sub>MPS</sub></b>	PD Maintain Power Signature Time For Validity		46	48	50	mS
<b>T<sub>OFF</sub></b>	Turn Off Time	From $V_{MAIN}$ to 2.8V			500	mS
<b>Port Current Monitoring</b>						
	Resolution	Reported as 14 Bits		10		Bits
	LSB			122.07		$\mu A$
	Measurement Period			16		mS
	Accuracy	$I_{PORT} < 350mA$ $I_{PORT} > 600mA$			3.5 2.8	%
<b>Port Voltage Monitoring</b>						
	Resolution			10		Bits
	LSB			58.6		mV
	Measurement Period			3		mS
	Accuracy				3.3	%





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**Main Voltage Monitoring**

	Resolution			10		Bits
	LSB			58.6		mV
	Measurement Period			3		mS
	Accuracy				2	%

**Temperature Monitoring**

	Resolution			8		Bits
	LSB	Temperature=(DATA x 1.92)-273		1.92		°C
	Measurement Period			3		mS
	Accuracy		-3		3	°C

**Digital Interface**

<b>V<sub>IH</sub></b>	Input Logic High Voltage	RESET_N, MOSI, MISO, SCK, CS_N, PGD[0..3], ADDR[0..3]	2.2			V
<b>V<sub>IL</sub></b>	Input Logic Low Voltage	RESET_N, MOSI, MISO, SCK, CS_N, PGD[0..3], ADDR[0..3]			0.8	V
<b>Hyst</b>	Input Logic Hysteresis Voltage	RESET_N, MOSI, MISO, SCK, CS_N, PGD[0..3], ADDR[0..3]	0.4	0.6	0.8	V
<b>I<sub>IH</sub></b>	Input Logic High Current	RESET_N, MOSI, MISO, SCK, CS_N, PGD[0..3], ADDR[0..3]	-10		10	μA
<b>I<sub>IL</sub></b>	Input Logic Low Current	RESET_N, MOSI, MISO, SCK, CS_N, PGD[0..3], ADDR[0..3]	-10		10	μA
<b>V<sub>OH</sub></b>	Output Logic High Voltage	RESET_N, MOSI, MISO, SCK, CS_N, PGD[0..3], ADDR[0..3] I <sub>OH</sub> = -1mA	2.4			V
<b>V<sub>OL</sub></b>	Output Logic Low Voltage	RESET_N, MOSI, MISO, SCK, CS_N, PGD[0..3], ADDR[0..3] I <sub>OH</sub> = 1mA			0.4	V

**Note:**

1. Can be override by communication command.
2. Port Power is limited to maximum 100W according to UL's LPS requirements. (Port Power= IPORT x VMAIN)



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## PD69200 Electrical Characteristics

In this application PD69200 consumption is ~20mA.

For a detailed electrical specification refer to the following datasheets at [www.freescale.com](http://www.freescale.com)

- **Manufacturer:** Freescale
- **Manufacturer part number:** MKL15Z128VFM4
- Maximum pull-ups consumption based on PD69200 application is 2mA.  
Refer to HW app note document : catalog number PD69208\_AN\_211

**PD69204**

4 Port PSE PoE Manager

**PD69200**

PSE PoE Controller

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**PD69200 Main Features Description**

**PD69204**

4 Port PSE PoE Manager

**PD69200**

PSE PoE Controller

**Table 8**

Function	Description
Supports up to 12 PoE devices – 48 physical ports (24 logical)	Up to 12 PoE devices can be cascaded, fitting into a 48 physical port PoE system that utilizes one PoE controller (PD69200). PD69200 can support up to 24 logical ports. A logical port can be built from 2xPhysical ports or 1xPhysical port.
Power Management	The system supports three power management modes: Class (LLDP) mode, Dynamic mode and Static mode.
Threshold Configuration	Configure overvoltage and under-voltage thresholds for disconnection purposes.
High power ports, 2 pairs or 4 pairs	PoE devices can be configured (both hardware and software) to enable higher current through ports (up to ~950mA) or double power at the RJ in case of 4 pairs.
Communication	Supports both I <sup>2</sup> C and UART interfaces with Host CPU.
Legacy (Reduced capacitance) Detection	Enables detection and powering of pre-standard devices (PDs) up to 11uF.
LED Stream	Direct SPI interface to an external LED stream circuitry. Enables designers to implement a simple LED circuit that does not require a software code. (LED stream clock frequency is 1MHz)
System OK Indication	Digital output pin to Host. System validity indication, when system is OK pin state is low. The behavior of this output is controlled by software mask register settings (Mask 0x28). The mask default settings is 0, means this pin indicates valid software and V <sub>main</sub> is in Range. (For more information refer to the Serial Communication Protocol User Guide document - Catalog Number: PD63000_UG) (This pin is active low)
System and Port Measurements	Measurements of the following parameters: Current (mA), Power Consumption (W), V <sub>main</sub> (V), Port Voltage (V), PD Class (0-4).
Detailed Port Status	Port statuses are received from PoE managers. Statuses such as 'port on' and 'port off' due to disconnection or due to overload.
Interrupt Pin	Interrupt out from PoE controller indicating events such as: port on, port off, port fault, PoE device fault, voltage out of range, and more. For a full list of interrupt events refer to For more information refer to the Serial Communication Protocol User Guide document - Catalog Number: PD63000_UG)
Port Power Limit	Configurable port power limit; when a port exceeds the limit, it is automatically disconnected
Port Matrix Control	Enables layout designers to connect all physical ports to logical ports whenever required.
'Power Good' Interrupt from Power Supply directly to POE Drivers.	For systems comprising more than a single power supply, in case one power supply fails, a fast port disconnection mechanism is executed to maintain operation and prevent collapse of other power supplies.



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PD69204 Package Outline Drawing 56 Pin QFN 8x8 mm

**PD69204**

4 Port PSE PoE Manager

**PD69200**

PSE PoE Controller

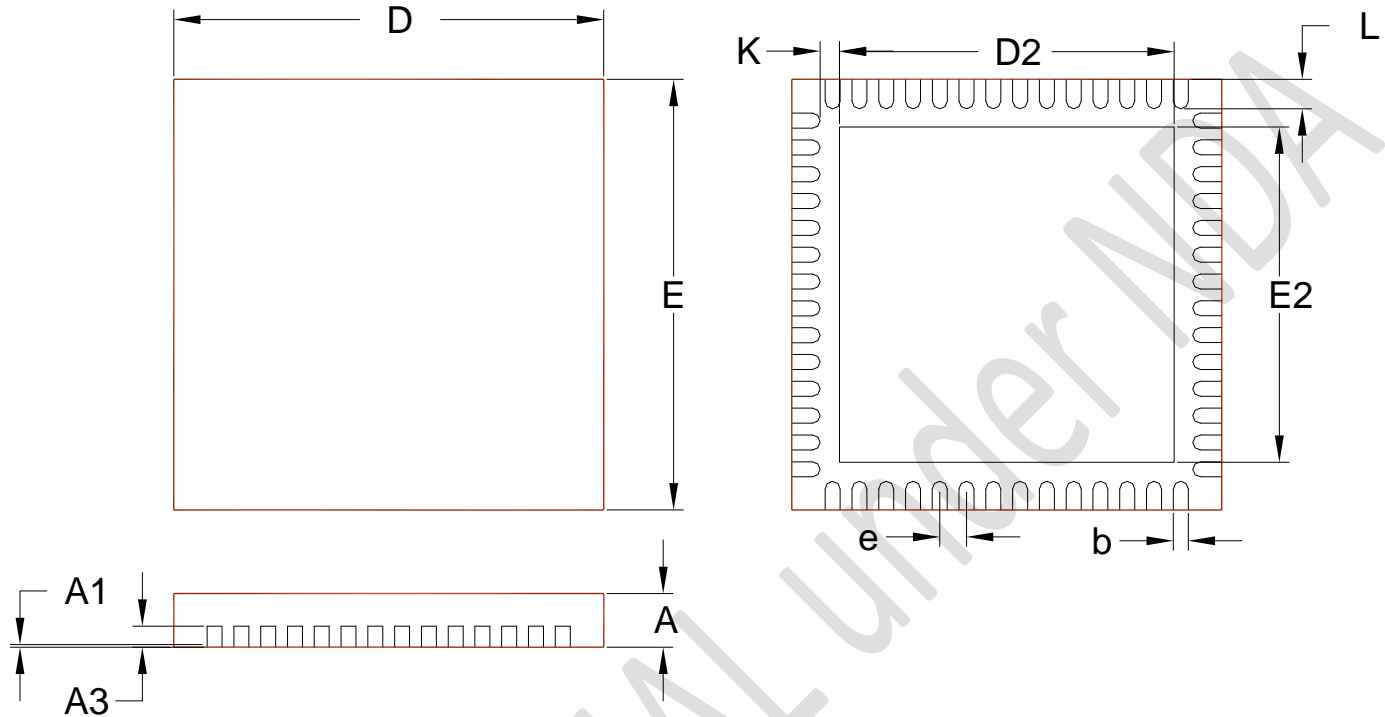


Figure 4 : PD69204 Package Outline Drawing

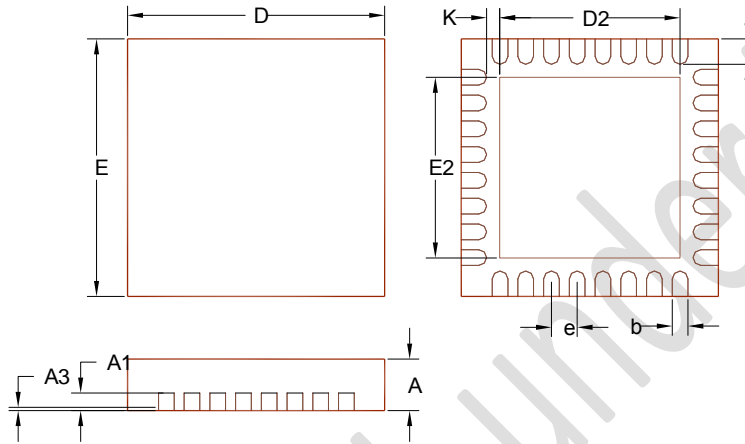
Table 9

Dim	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	0.80	1.00	0.031	0.039
A1	0.00	0.05	0	0.002
A3	0.20 REF		0.008 REF	
K	0.20 MIN		0.008 MIN	
e	0.50 BSC		0.02 BSC	
L	0.30	0.50	0.012	0.02
b	0.18	0.30	0.007	0.012
D2	6.50	6.75	0.256	0.267
E2	6.50	6.75	0.256	0.267
D	8.00 BSC		0.315 BSC	
E	8.00 BSC		0.315 BSC	

**Note:**

1. Dimensions do not include protrusions; these shall not exceed 0.155mm (.006") on any side. Lead dimension shall not include solder coverage.
2. Dimensions are in millimeters, inches for reference only.

**PD69200 Package Outline Drawing 32 Pin QFN 5x5 mm**



**Figure 5 : PD69200 Package Outline Drawing**

**Table 10**

Dim	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	0.80	1.00	0.031	0.039
A1	0.00	0.05	0	0.002
A3	0.20 REF		0.008 REF	
K	0.20 MIN		0.008 MIN	
e	0.50 BSC		0.02 BSC	
L	0.30	0.50	0.012	0.02
b	0.18	0.30	0.007	0.012
D2	3.50	3.70	0.138	0.147
E2	3.50	3.70	0.138	0.147
D	5.00 BSC		0.197 BSC	
E	5.00 BSC		0.197 BSC	

**Note:**

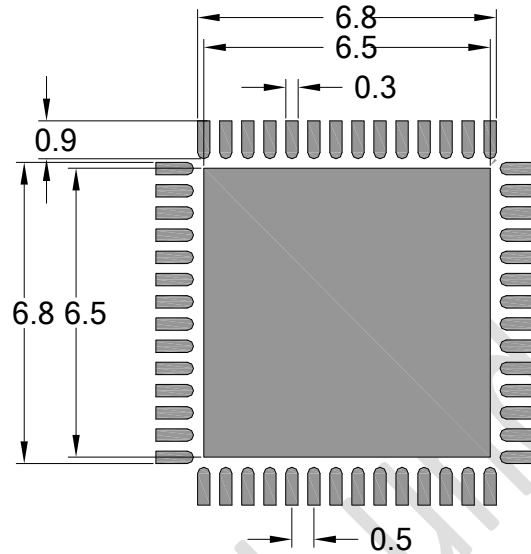
1. Dimensions do not include protrusions; these shall not exceed 0.155mm (.006") on any side. Lead dimension shall not include solder coverage.
2. Dimensions are in millimeters, inches for reference only.



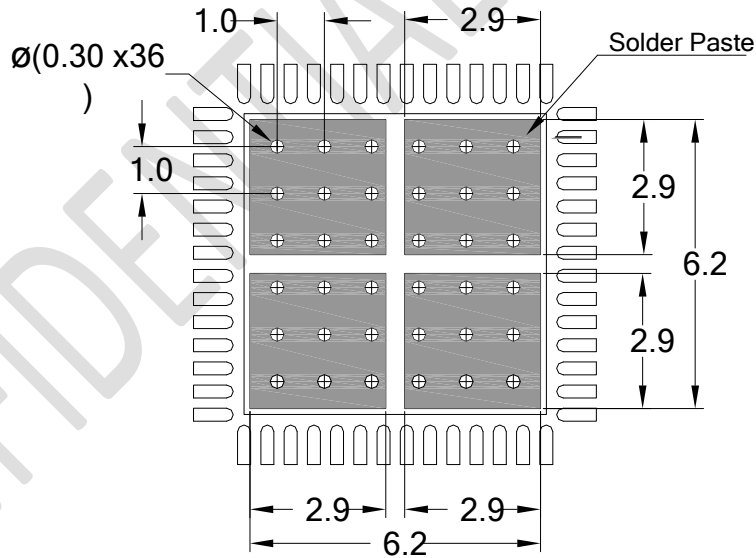
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**PD69204 Recommended PCB layout for 56 Pin QFN 8x8 mm**

Recommended PCB layout pattern for PD69204 is described in the following three figures.



**Figure 6: PD69204 Top layer Copper Recommended PCB Layout (mm)**



**Figure 7: PD69204 Top layer Solder Paste and Vias Recommended PCB Layout for Thermal Pad Array (mm)**

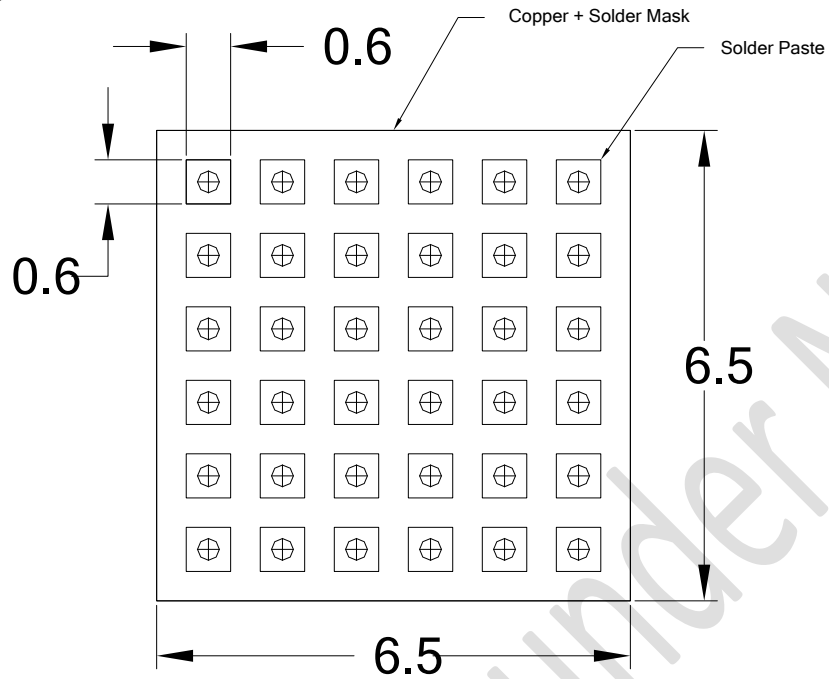


Figure 8: PD69204 Bottom layer Copper and Solder Paste Recommended PCB Layout for Thermal Pad Array (mm)



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4 Port PSE PoE Manager

**PD69200**

PSE PoE Controller

**PD69200 Recommended PCB layout for 32 Pin QFN 5x5 mm**

Recommended PCB layout pattern for PD69200 is described in the following two figures.

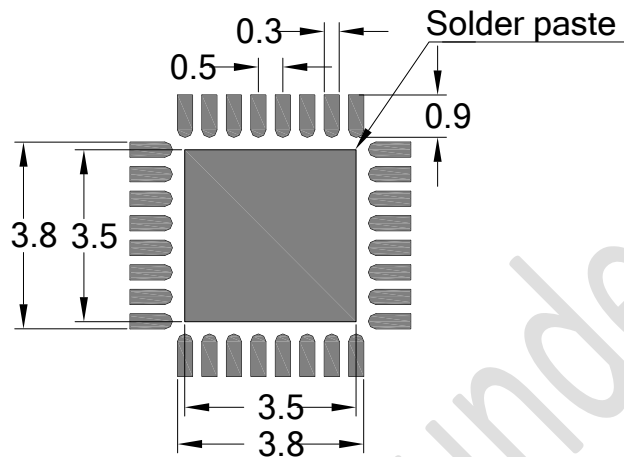


Figure 9: PD69200 Top layer Copper Recommended PCB Layout (mm)

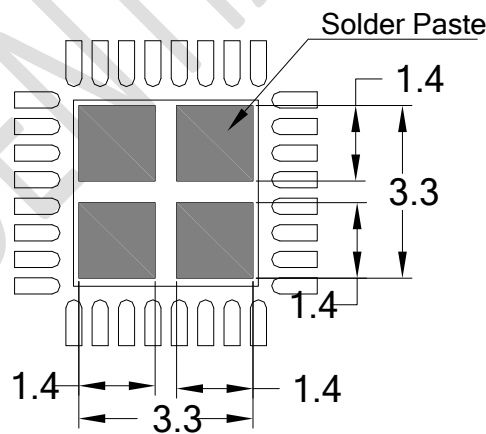


Figure 10: PD69200 Top layer Solder Paste and Vias Recommended PCB Layout for Thermal Pad Array (mm)





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**Recommended Solder Reflow Information**

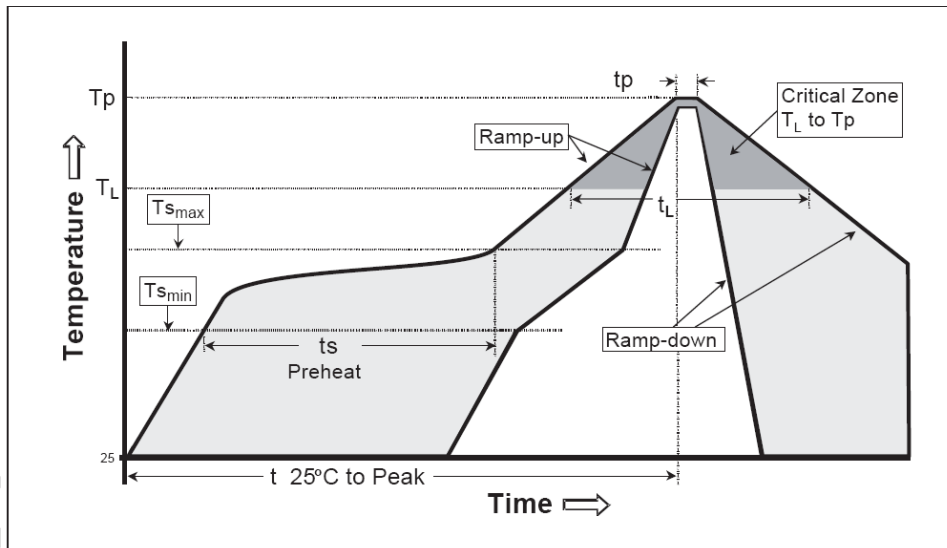
RoHS 6/6

Pb-free 100% Matte Tin Finish

Package Peak Temperature for Solder Reflow      260°C (+0°C, -5°C)  
 (40 seconds maximum exposure)

Profile Feature	Classification Reflow Profiles	
	Sn-Pb Eutectic Assembly	Pb-Free Assembly
Average Ramp-Up Rate (T <sub>Smax</sub> to T <sub>p</sub> )	3 °C/second max.	3° C/second max.
<b>Preheat</b>		
– Temperature Min (T <sub>Smin</sub> )	100 °C	150 °C
– Temperature Max (T <sub>Smax</sub> )	150 °C	200 °C
– Time (t <sub>Smin</sub> to t <sub>Smax</sub> )	60-120 seconds	60-180 seconds
Time maintained above:		
– Temperature (T <sub>L</sub> )	183 °C	217 °C
– Time (t <sub>L</sub> )	60-150 seconds	60-150 seconds
Peak/Classification Temperature (T <sub>p</sub> )	See Table 4.1	See Table 4.2
Time within 5 °C of actual Peak Temperature (t <sub>p</sub> )	10-30 seconds	20-40 seconds
Ramp-Down Rate	6 °C/second max.	6 °C/second max.
Time 25 °C to Peak Temperature	6 minutes max.	8 minutes max.

**Note 1:** All temperatures refer to topside of the package, measured on the package body surface.



Classification Reflow Profile

**Pb-free Process – Package Classification Reflow Temperatures**

Package Thickness	Volume mm <sup>3</sup> <350	Volume mm <sup>3</sup> 350 - 2000	Volume mm <sup>3</sup> >2000
<1.6 mm	260 +0 °C *	260 +0 °C *	260 +0 °C *
1.6 mm - 2.5 mm	260 +0 °C *	250 +0 °C *	245 +0 °C *
≥2.5 mm	250 +0 °C *	245 +0 °C *	245 +0 °C *

\* Tolerance: The device manufacturer/supplier **shall** assure process compatibility up to and including the stated classification temperature (this means Peak reflow temperature +0 °C. For example 260 °C+0°C) at the rated MSL level.

**Note:** Exceeding these ratings may cause damage to the device.

## Application Information

PD69204 performs IEEE802.3af and IEEE802.3at functionality, as well as legacy (capacitor) and pre standard PDs detection. Moreover it includes additional protections such as short circuit and dV/dT protection upon startup.

### PD Detection

The PD Detection feature detects a valid AF or AT load, as specified in the AF / AT standard. PD detection is based on four different voltage levels generated over PD (the load) as illustrated in Figure 12.

### Legacy (Reduced Capacitor) Detection

In cases where legacy is set, PD Detection mechanism detects and powers up legacy PDs as well as AF/AT compliant PDs. This mechanism is designed to detect and power up pre standard legacy PDs.

### Classification

The classification process takes place immediately after PD detection is successfully completed. The

goal of the classification process is to detect PD class, as specified in IEEE802.3AF and AT standards.

In AF mode, the classification mechanism is based on a single voltage level (single event).

In AT mode, the classification mechanism is based on two voltage levels (dual events) as defined in IEEE802.3at-2009.

In PoH mode, the classification mechanism is based on three events classification as defined in HDBaseT standard.

### Port Start Up

Upon a successful detection and classification process, power is applied to the load via a controlled Start Up mechanism.

During this period inrush current is limited to 425mA for a typical duration of 65mS, which allows PD load to charge and allow steady state power condition.

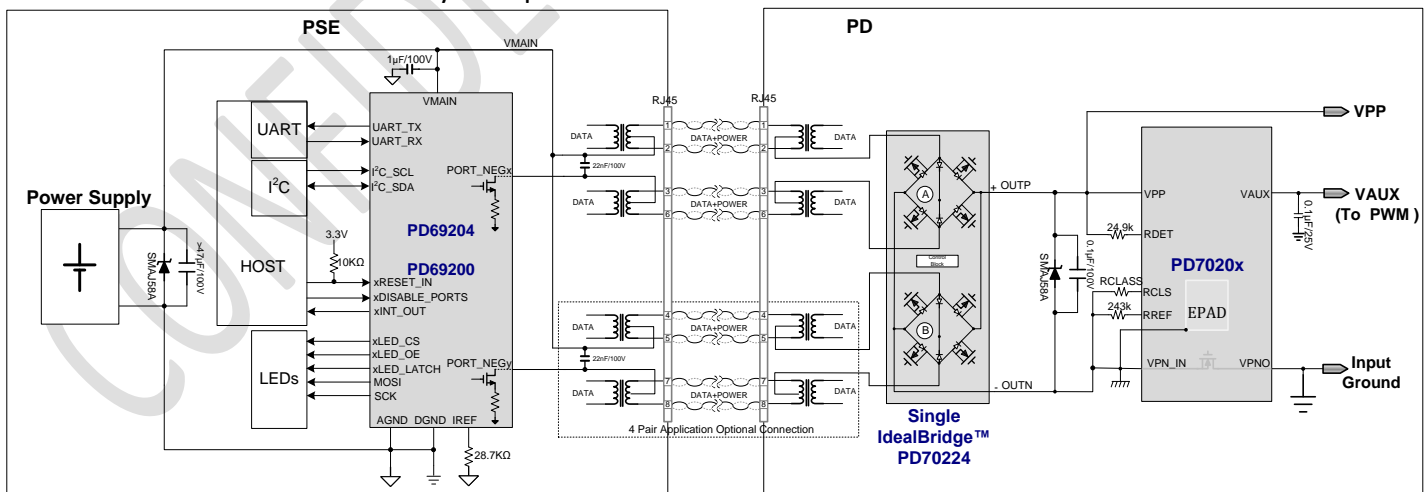
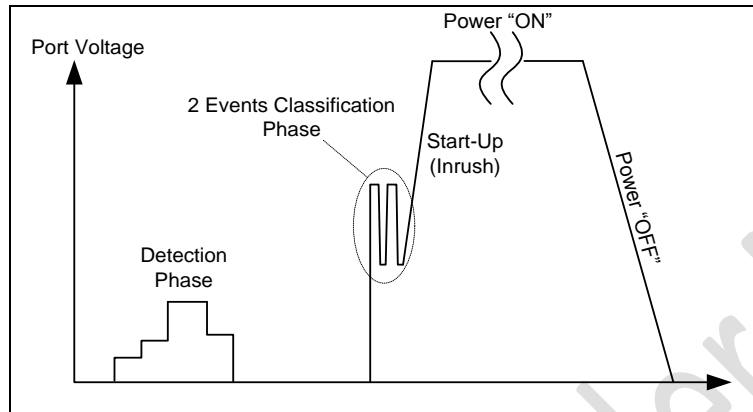


Figure 11:4-Pairs PoE System Diagram



**Figure 12: Typical IEEE802.3at Port PoE Voltage Diagram**

**Over-Load Detection and Port Shut Down**

After power up, PD69204 automatically initializes its internal protection mechanisms. These are utilized to monitor and disconnect power from the PD in cases where extreme conditions occur, as specified in IEEE802.3AF/AT standard. These conditions include over-current or short ports terminals scenario.

**Disconnect Detection**

PD69204 supports DC Disconnect Function as per IEEE802.3AF/AT standard.

This mechanism continuously monitors load current and disconnects power in cases where load current is below 7.5mA (typical) for more than 324mS.

**IC Thermal monitoring**

The PD69204 contain a thermal sensor that is sampled by the PD69200 every 20mS so the PD69204 die temperature is monitored at all times.

In case the die exceeds the 150°C the system ports will be disconnected to protect the PD69204 ICs.

An temperature alarm threshold can be set by PD69200 controller to send interrupt indication by the xINT\_OUT pin before ports disconnects.

The temperature can be read and monitored by the host as well, if required.

**Over-Temperature Protection**

In addition to the die thermal sensor there are thermal sensors on each MOSFET that continuously monitor per port main MOSFETs junction temperature and will shut down the port load power in cases where temperature exceeds 200°C.

**V<sub>MAIN</sub> Out of Range Protection**

The system will automatically disconnect ports power in cases where V<sub>MAIN</sub> exceeds pre configure over-voltage and under-voltage thresholds.



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**PD69204**

4 Port PSE PoE Manager

**PD69200**

PSE PoE Controller

#### 4-Pairs Ports

In order to have the ability to deliver to the PD more than 30w, 4 pairs powering is used.

4 pairs powering utilizes all 8 RJ45 wires for delivering the power.

It is implemented by utilizing as 2 physical ports of (1 logical port) PD69204 with 2 separate front-ends, each delivers maximum AT power, enabling delivery of 60W over 4 pairs.

The 2 ports drive separate 2 pairs and connect together inside the PD after the serial diodes as shown in Figure 11.

The 2 ports will be managed by PD69200 with certain rules.

In this case, PD69200 can support up to 48 logical 4 pairs ports (96 physical ports)

- The 2 ports that compound the 4 pairs port is predefine prior the system startup. 4 pairs port can be built from combination of any 2 ports in the system, same PD69204 or separate ones. Ports status is unified (the two ports will have the same status)
- Line detection:
  - In case one port fails Pre-Detection, port will turn-on as 2 pair port.
  - In case both pairs pass Pre-Detection and fail Line Detection, port will not power-on.
- Classification:
  - PD should have mechanism that counts the number of class events and determines PSE type.
    - 2 class events – PSE is 2 pairs AT.
    - 4 class events – PSE is 4 pairs AT/UPoE.
    - 6 class events – PSE is 4 pairs PoH.
  - When one of the classes (or both) is "class error", both ports will not turn on.
  - When 2 ports have different class level, port will not turn on any of the pairs.

- Startup:

- Startup of the ports is done simultaneously with maximum gap of 100 $\mu$ S.

- Port disconnection:

In case one of the ports disconnects due to fault (OVL, UDL, OVT, SC, TLIM), second port will immediately follow it and also disconnect.

#### Power Management

System supports three power management modes:

- Class (LLDP) mode
- Dynamic mode
- Static mode.

#### PPL (Port Power Limit)

Configurable port power limit; when a port exceeds the limit, it is automatically disconnected



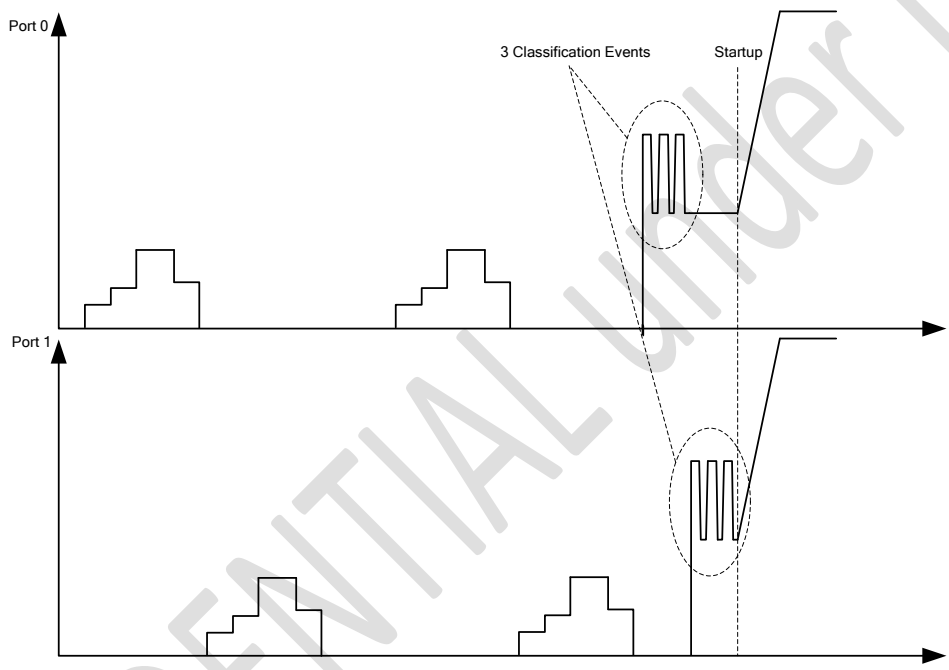
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**PoH – Power over HDBaseT**

PoH powering enables PSE to provide 95W power. Detection, powering, and disconnection are same as 4 pairs powering.

- Power:
  - According to PoH standard, minimal power on PSE output should be 95W.

- Due to UL restriction, maximum power on PSE output is limited to 100W.
- Classification:
  - Each port classification will have 3 class events so that PD will detect 6 events.



**Figure 13 – 4 pairs PoH detection diagram**

**Reset Pin**

xRESET pin is Digital Host Reset input (Active Low). The shortest pulse that is guaranteed to be recognized is 100nSec. PD69200 can generate self-reset. In this case xRESET pin is driven low by PD69200 for at least 128 bus clock cycles and until flash Initialization has completed. It is recommended to connect this pin to a host open drain output with pull-up in a range of 4.7Kohm to 10Kohm.

If this pin is connected to a push/pull driver, a serial resistor of 4.7Kohm must be connected instead of pull-up. For more information about this pin connectivity refer to HW app note, Catalog Number: PD69208\_AN\_211.

**System OK Indication**

Digital output pin to Host is used as System validity indication. When system is OK pin state is low. The behavior of this output is controlled by software mask register settings (Mask 0x28).



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The mask default settings is 0, means this pin indicates valid software and Vmain is in Range. (For more information refer to the Serial Communication Protocol User Guide document - Catalog Number: PD63000\_UG)

(This pin is active low).

### **Interrupt Pin**

Interrupt out from PoE controller, indicating events such as: port on, port off, port fault, PoE device fault, voltage out of range, and more. For a full list of interrupt events refer to the Serial Communication Protocol User Guide document - Catalog Number: PD63000\_UG). This pin is active low.

### **Port Matrix Control**

Enables layout designers to ascribe each physical port in the system to required logical port if required.

### **'Power Good' Interrupt**

Interrupt from Power Supply directly to PD69204 manager.

For systems comprising more than a single power supply, in case one power supply fails, a port

shading mechanism is executed to maintain operation and prevent collapse of other power supplies.

When function is used, PGD0, PGD1, PGD2, and PGD3 should be connected to main power supplies status indication pin. Any change of at least 1 $\mu$ S on these lines will trigger a pre-defined disconnection matrix. This matrix is defined by PD69200 system power parameters.

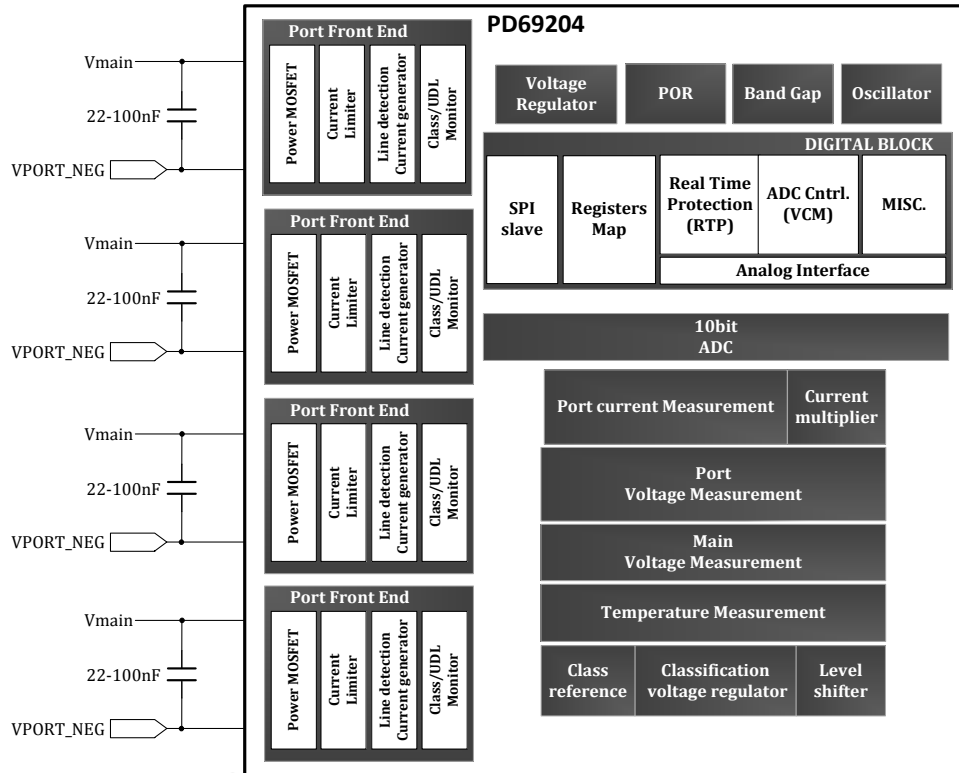
The port shading function reacts within 2  $\mu$ S to any Power Good event.

### **LED Stream**

Direct SPI interface to an external LED stream circuitry, that can drive LEDs directly without the host intervention. Enables designers to implement a simple LED circuit that does not require a software code. (LED stream clock frequency is 1MHz).

For more detailed information please refer to AN-201, catalog number PD69100\_TN\_201.

**PD69204/PD69200 Product Overview**



**Figure 14: PD69204 Block Diagram**



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### Digital Block Module

Logic Main Control Block includes Digital Timing Mechanisms and State Machines synchronizing and activating PoE functions according to PD69200 control commands, such as:

- Real Time Protection (RTP)
- Start Up Macro (DVDT)
- Load Signature Detection (RES DET)
- Classification Macro (CLASS)
- Voltage and Current Monitoring (VCM)
- ADC Interfacing
- Direct Digital Signals with Analog Block
- SPI Communication Block
- Registers

### PD Detection Generator

Upon request from PD69200 to Main Control Module, PD Detection Generator generates four different voltage levels to ensure a robust AF / AT PD Detection functionality.

### Classification Generator

Upon request from PD69200 to Main Control Module, State Machine applies a regulated Class Event and Mark Event voltage to ports, as required by IEEE standard.

### Current Limiter

This circuit continuously monitors the current of powered ports and limits the current to a specific value, according to pre-defined limits as set by AF/AT/PoH. In cases where current exceeds this specific level, system starts measuring elapsed time. If this time period is greater than a preset threshold, port is disconnected.

### Main Power MOSFET

Main power switching FET, used to control PoE current into load.

### ADC

A 10-Bit Analog to Digital converter, used to convert analog signals into digital registers for Logic Control Module.

### Power on Reset (POR)

Monitors the internal 3.3V voltage DC levels; if this voltage drops below specific thresholds, a reset signal is generated and PD69204 is reset.

### Voltage Regulator

Voltage regulator generates 3.3V and 5V for internal circuitry. These voltages are derived from  $V_{MAIN}$  supply.

To use internal voltage regulator connect:

- VAUX5 to DRV\_VAUX5
- VAUX3P3 to VAUX3P3\_INT

There are three options to reduce PD69204 power dissipation by regulating voltage outside the chip:

- Use an external NPN transistor to regulate the 5V.  
In this setup, the configuration of regulators pins should be:
  - DRV\_VAUX5 is connected to NPN BASE
  - VAUX5 is connected to NPN EMITTER  
(Connect Collector to  $V_{MAIN}$ )
  - VAUX3P3 is connected to VAUX3P3\_INT
- Supply PD69204 with an external 5V voltage regulator.  
In this setup, regulators pins configuration should be:
  - VAUX3P3 is connected to VAUX3P3\_INT
  - DRV\_VAUX5 is not connected (left open)
  - VAUX5 is connected to external 5 V





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- Supply PD69204 with an external 3.3V voltage regulator.

In this setup, regulators pins configuration should be:

- VAUX5 is connected to DRV\_VAUX5
- VAUX3P3\_INT is not connected (left open)
- VAUX3P3 is connected to external 3.3 V

The options can be implemented simultaneously.

**CLK**

CLK is an internal 8 MHz clock oscillator

**SPI Communication**

PD69204 uses SPI communication in order to communicate with PD69200 MCU.

SPI acts as an SPI slave mode only.

Each PD69204 has an address determined by ADDR0-ADDR3 pins. Up to 12 ICs can be supported.

Actual frequency between PD69200 and PD69204 ICs is 1MHz.

Packets structure is as follows:

Control byte Selects PD69204 According to the address	R/W bit	Internal Register Address	Number of words (only in read access)	Data Written to IC (in write access) Read from IC (in read access)
8 bits	R(0)/W(1)	8 bits	8 bits	bits 16

PD69204 SPI Addressing

PD69204 Operates in 8 bit address and 16 bit data

PD69204 responds to SPI transaction if the first SPI byte (IC address byte bits[7:1]) complies with the following:

3bits:'000'	4bits: address input pin	1bit: r/w
-------------	--------------------------	-----------

Broadcast:

- A broadcast command is intended to instruct all connected PD69204 ICs to perform a specific operation.
- Broadcast command is a write command with the standard packet structure. In case of a broadcast read operation the read data is not valid and the read operation has no impact.

3bits:'001'	4bits: '0000'	1bit: w
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SPI Detailed Timing Information

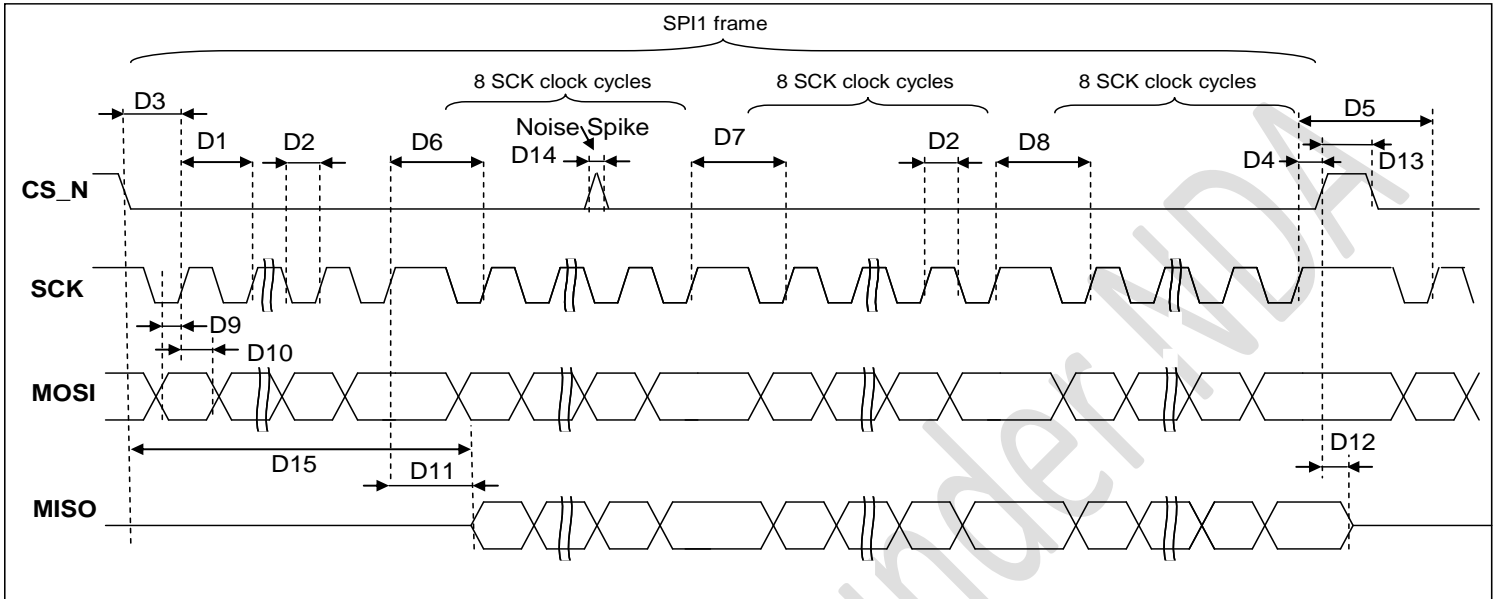


Figure 15 : SPI Detailed Timing Diagram

Table 11

Name	Min Delay	Max Delay	Description
D1		714ns	SPI clock period
D2	45	55	SPI duty cycle
D3	340 ns		SPI_CS setup to SPI clock Positive Edge (delay after SPI_CS active signal)
D4	340 ns		SPI_CS hold to SPI clock Positive Edge (delay before SPI_CS inactive Signal)
D5	2 spi clock cycles		Delay between last SCK in eSPI1 frame and first SCK at adjacent eSPI1 frame
D6	1 spi clock cycles		Between byte 0 (IC addr) and byte 1(addr)
D7	1 spi clock cycles		Between byte 1 (addr) and byte 2(data).
D8	1 SPI clock cycles		Between byte 2 (MS data byte) and byte 3(LS data byte).
D9	340 ns		MOSI setup time
D10	210 ns		MOSI hold time



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Name	Min Delay	Max Delay	Description
D11		140ns	MISO tri-state to valid data from clock positive edge
D12		300ns	MISO valid data to tri-state from SPI_CS positive edge
D13	1 SPI clock cycles		SPI_CS width (Delay eSPI1 frame to adjacent eSPI1 frame)
D14		60ns	Filtered Glitch Width
D15	D3 + 15.5 SPI clock cycles	D3+23.75 SPI clock cycles	MISO tri-state from SPI_CS Negative Edge to valid data

**PD69200 I<sup>2</sup>C Address Selection**

I<sup>2</sup>C interface between Host CPU and a specific PD69200 requires setting PD69200 address; this is done by applying a specific voltage level to pin #22 (I2C\_ADDR\_MEAS) as shown below:

Table 12

I2C_ADDR VOLTAGE LEVEL	I <sup>2</sup> C ADDRESS (HEXADECIMAL)
0.00 to 0.21V <sub>DC</sub>	UART
0.21 to 0.41V <sub>DC</sub>	0x4
0.41 to 0.62V <sub>DC</sub>	0x8
0.62 to 0.83V <sub>DC</sub>	0xC
0.83 to 1.03V <sub>DC</sub>	0x10
1.03 to 1.24V <sub>DC</sub>	0x14
1.24 to 1.44V <sub>DC</sub>	0x18
1.44 to 1.65V <sub>DC</sub>	0x1C
1.65 to 1.86V <sub>DC</sub>	0x20
1.86 to 2.06V <sub>DC</sub>	0x24
2.06 to 2.27V <sub>DC</sub>	0x28
2.27 to 2.48V <sub>DC</sub>	0x2C
2.48 to 2.68V <sub>DC</sub>	0x30
2.68 to 2.89V <sub>DC</sub>	0x34
2.89 to 3.09V <sub>DC</sub>	0x38
3.09 to 3.30V <sub>DC</sub>	0x3C

**Note:** UART communications configuration:

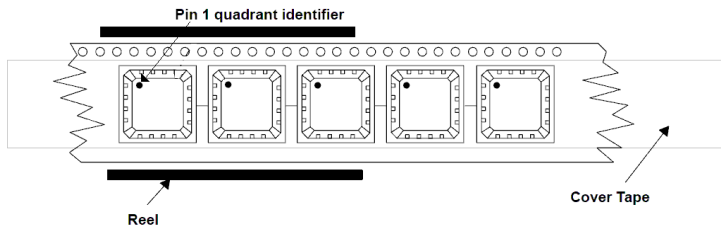
- Bits per second: 19,200 bps
- Data bits: 8
- Parity: None
- Stop bits: 1
- Flow control: None



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**Tape and Reel – Packaging Information**

**Table 13**

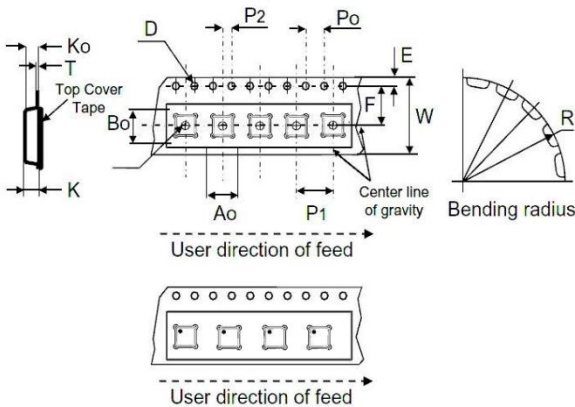


**Pin-1 Orientation of QFN Packages**

**Figure 16 : Tape and Reel Pin-1 Oreintation**

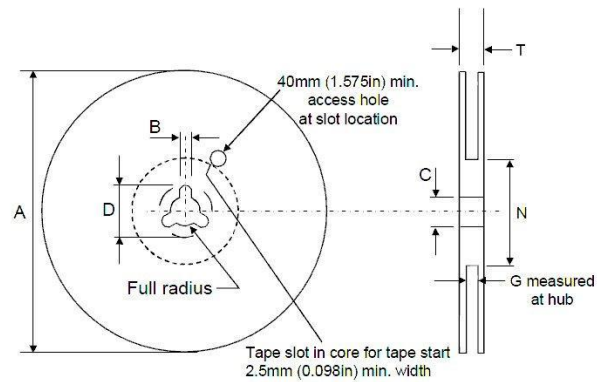
REEL MECHANICAL DATA		
	mm.	inch
Tape size	16.00 ±0.3	0.630 ±0.012
A max.	330	13"
B max.	1.5	0.059
C	13.0 ±0.20	0.512 ±0.008
D min.	20.2	0.795
N min.	50	1.968
G	16.4+2.0/-0.0	0.645+0.079/-0.0
T max.	29	1.142
BASE QUANTITY	2000 pcs.	

**TAPE & REEL SHIPMENT INFORMATION  
TAPE SPECIFICATIONS**



**Figure 18 : Tape and Reel Tape specifications**

**TAPE & REEL SHIPMENT INFORMATION  
REEL SPECIFICATIONS**



**Figure 17 : Tape and Reel Reel specifications**



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**PD69204**

4 Port PSE PoE Manager

**PD69200**

PSE PoE Controller

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**Revision History**

Revision Level / Date	Para. Affected	Description
1.0 / June 2014	-	Official Release
1.01 / June 2014		Wording updates; parameter update
1.02 / Nov 2014		Typical Application change port capacitors to 22-100nF
1.03 / Feb 2015		Adding PD69200 T&R ordering option
1.04 / July 2015	Typical application	Adding note that fuses per port are not required for use in circuits with total power level of up to 3kW
1.05 / July 2016	<ul style="list-style-type: none"> <li>Page 2</li> <li>Page 5</li> <li>Page 6</li> </ul>	<ul style="list-style-type: none"> <li>Feature list → Change MSL1 of PD69208 to MSL3</li> <li>Ordering information → Change MSL1 of PD69208 to MSL3</li> <li>PD69200 MSL class update (Typo)</li> <li>PD69200 marking information update</li> <li>General updates</li> </ul>
1.06 / August 2016	<ul style="list-style-type: none"> <li>Page 5</li> <li>Page 16</li> </ul>	<ul style="list-style-type: none"> <li>According to PCN155881, qualification of UTAC Thailand assembly for PD6920X. Parts from UTAC will be identified by different marking that was added on page 5.</li> <li>Match 802.3af ILIM and IINRUSH levels to IEEE standard levels.</li> <li>Match 802.3at &amp; PoH ILIM low level to IEEE standard level.</li> </ul>

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For support contact: [PoEsupport@microsemi.com](mailto:PoEsupport@microsemi.com)

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