# GTL2034

## 4-bit GTL to GTL buffer

Rev. 1.1 — 20 December 2021 | Product data sheet

## 1 General description

The GTL2034 is a 4-bit GTL-/GTL/GTL+ bus buffer.

The GTL2034 GTL inputs and outputs operate up to 3.6 V, allowing the device to be used in higher voltage open-drain output applications.

## 2 Features

- Operates as a 4-bit GTL-/GTL/GTL+ to GTL-/GTL/GTL+ bus buffer
- 3.0 V to 3.6 V operation
- GTL input and output 3.6 V tolerant
- $V_{ref}$ adjustable from 0.5 V to $V_{CC}$ / 2
- Partial power-down permitted
- ESD protection exceeds 2000 V HBM per JESD22-A114, 200 V MM per JESD22-A115, and 1000 V CDM per JESD22-CC101
- Latch-up protection exceeds 500 mA per JESD78
- Package offered: TSSOP14

## 3 Quick reference data

**Table 1. Quick reference data**

*$T_{amb}$ = 25 °C*

| Symbol | Parameter | Conditions | | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|---|
| $t_{PLH}$ | LOW-to-HIGH propagation delay | GTL; BIn to BOn; $C_L$ = 50 pF; $V_{CC}$ = 3.3 V | | - | 3.1 | 8 | ns |
| $t_{PHL}$ | HIGH-to-LOW propagation delay | | | - | 4.1 | 10 | ns |
| $C_i$ | input capacitance | GTL; outputs disabled; $V_{I/O}$ = 0 V or 3.0 V | | - | 4.5 | - | pF |

## 4 Ordering information

**Table 2. Ordering information**

| Type number | Topside marking | Package | | |
|---|---|---|---|---|
| | | Name | Description | Version |
| GTL2034PW | GTL2034 | TSSOP14 | plastic thin shrink small outline package; 14 leads; body width 4.4 mm | SOT402-1 |

### 4.1 Ordering options

**Table 3. Ordering options**

| Type number | Orderable part number | Package | Packing method [1] | Minimum order quantity | Temperature |
|---|---|---|---|---|---|
| GTL2034PW | GTL2034PW,118 [2] | TSSOP14 | REEL 13" Q1/T1 NDP | 2500 | $T_{amb}$ = -40 °C to +85 °C |
| | GTL2034PWZ | TSSOP14 | REEL 13" Q1/T1 NDP SSB [3] | 2500 | $T_{amb}$ = -40 °C to +85 °C |

[1] Standard packing quantities and other packaging data are available at www.nxp.com/packages/.
[2] Discontinued in 202111031DN; drop in replacement is GTL2034PWZ
[3] This packing method uses a Static Shielding Bag (SSB) solution. Material should be kept in the sealed bag between uses.

## 5 Functional diagram

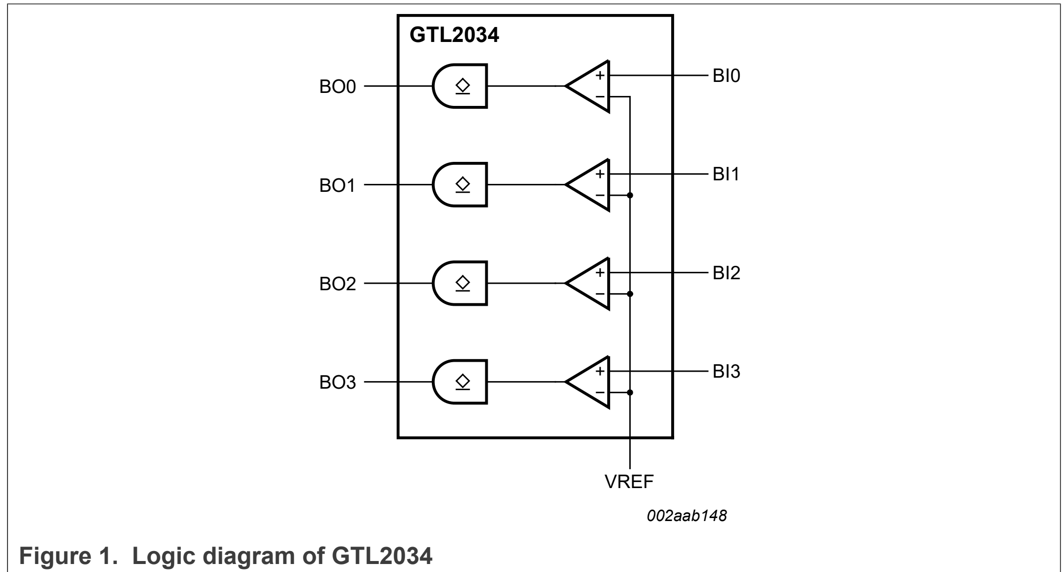


**Figure 1. Logic diagram of GTL2034**

## 6 Pinning information

### 6.1 Pinning

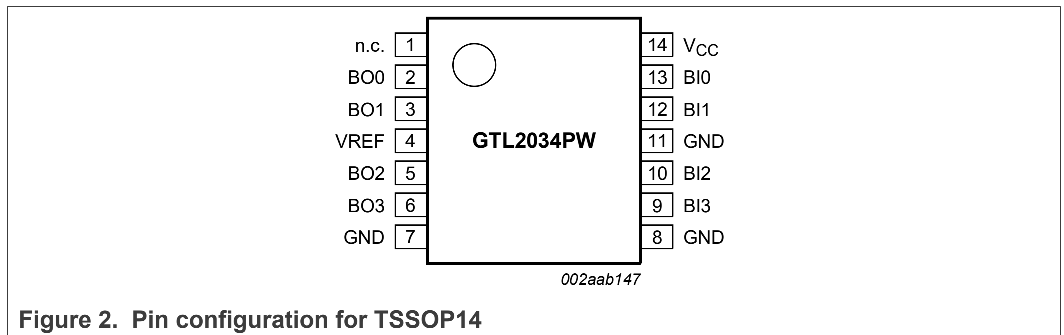


**Figure 2. Pin configuration for TSSOP14**


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### 6.2 Pin description

**Table 4. Pin description**

| Symbol | Pin | Description |
|---|---|---|
| n.c. | 1 | not connected |
| BO0 | 2 | data outputs (GTL) |
| BO1 | 3 | |
| BO2 | 5 | |
| BO3 | 6 | |
| BI0 | 13 | data inputs (GTL) |
| BI1 | 12 | |
| BI2 | 10 | |
| BI3 | 9 | |
| VREF | 4 | GTL reference voltage |
| GND | 7, 8, 11 | ground (0 V) |
| $V_{CC}$ | 14 | positive supply voltage |

## 7 Functional description

Refer to Figure 1.

### 7.1 Function table

**Table 5. Function table**

| Input/output | |
|---|---|
| **BIn (GTL)** | **BOn (GTL)** |
| Input | BOn = BIn |

## 8 Limiting values

**Table 6. Limiting values**

*In accordance with the Absolute Maximum Rating System (IEC 60134).* [1]

*Voltages are referenced to GND (ground = 0 V).*

| Symbol | Parameter | Conditions | | Min | Max | Unit |
|---|---|---|---|---|---|---|
| $V_{CC}$ | supply voltage | | | -0.5 | +4.6 | V |
| $I_{IK}$ | input clamping current | $V_I < 0$ V | | - | -50 | mA |
| $V_I$ | input voltage | B port | | -0.5[2] | +4.6 | V |
| $I_{OK}$ | output clamping current | $V_O < 0$ V | | - | -50 | mA |
| $V_O$ | output voltage | output in OFF or HIGH state; B port | | -0.5[2] | +4.6 | V |
| $I_{OL}$ | LOW-state output current[3] | B port | | - | 80 | mA |
| $T_{stg}$ | storage temperature | | [4] | -60 | +150 | °C |



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[1] Stresses beyond those listed may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under Section 9 is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
[2] The input and output negative voltage ratings may be exceeded if the input and output clamp current ratings are observed.
[3] Current into any output in the LOW state.
[4] The performance capability of a high-performance integrated circuit in conjunction with its thermal environment can create junction temperatures which are detrimental to reliability. The maximum junction temperature of this integrated circuit should not exceed 150 °C.

# 9 Recommended operating conditions

**Table 7. Recommended operating conditions**

*Unused inputs must be held HIGH or LOW to prevent them from floating.*

| Symbol | Parameter | Conditions | | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|---|
| $V_{CC}$ | supply voltage | | | 3.0 | - | 3.6 | V |
| $V_{TT}$ | termination voltage[1] | GTL- | | 0.85 | 0.9 | 0.95 | V |
| | | GTL | | 1.14 | 1.2 | 1.26 | V |
| | | GTL+ | | 1.35 | 1.5 | 1.65 | V |
| $V_{ref}$ | reference voltage | overall | | 0.5 | $\frac{2}{3}V_{TT}$ | $V_{CC}$ / 2 | V |
| | | GTL- | | 0.5 | 0.6 | 0.63 | V |
| | | GTL | | 0.76 | 0.8 | 0.84 | V |
| | | GTL+ | | 0.87 | 1.0 | 1.10 | V |
| $V_I$ | input voltage | B port | | 0 | $V_{TT}$ | 3.6 | V |
| $V_{IH}$ | HIGH-state input voltage | B port | | $V_{ref}$ + 0.050 | - | - | V |
| $V_{IL}$ | LOW-state input voltage | B port | | - | - | $V_{ref}$ - 0.050 | V |
| $I_{OL}$ | LOW-state output current | B port | | - | - | 40 | mA |
| $T_{amb}$ | ambient temperature | operating in free air | | -40 | - | +85 | °C |

[1] $V_{TT}$ maximum of 3.6 V with resistor sized so $I_{OL}$ maximum is not exceeded.

# 10 Static characteristics

**Table 8. Static characteristics**

*Recommended operating conditions; voltages are referenced to GND (ground = 0 V). $T_{amb}$ = -40 °C to +85 °C*

| Symbol | Parameter | Conditions | | Min | Typ[1] | Max | Unit |
|---|---|---|---|---|---|---|---|
| $V_{OL}$ | LOW-state output voltage | B port; $V_{CC}$ = 3.0 V; $I_{OL}$ = 40 mA | [2] | - | 0.2 | 0.4 | V |
| $I_I$ | input current | B port; $V_{CC}$ = 3.6 V; $V_I$ = $V_{TT}$ or GND | | - | - | ±1 | μA |
| $I_{LO}$ | output leakage current | B port; $V_{CC}$ = 3.6 V; $V_O$ = $V_{TT}$ | | - | - | ±1 | μA |
| $I_{CC}$ | quiescent supply current | B port; $V_{CC}$ = 3.6 V; $V_I$ = $V_{CC}$ or GND; $I_O$ = 0 mA | | - | 4 | 8 | mA |
| $C_i$ | input capacitance | port BIn; $V_O$ = $V_{TT}$ or 0 V | | - | 4.5 | - | pF |
| $C_o$ | output capacitance | port BOn; $V_O$ = $V_{TT}$ or 0 V | | - | 5.5 | - | pF |

[1] All typical values are measured at $V_{CC}$ = 3.3 V and $T_{amb}$ = 25 °C.
[2] The input and output voltage ratings may be exceeded if the input and output current ratings are observed.


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### 10.1 Performance curves

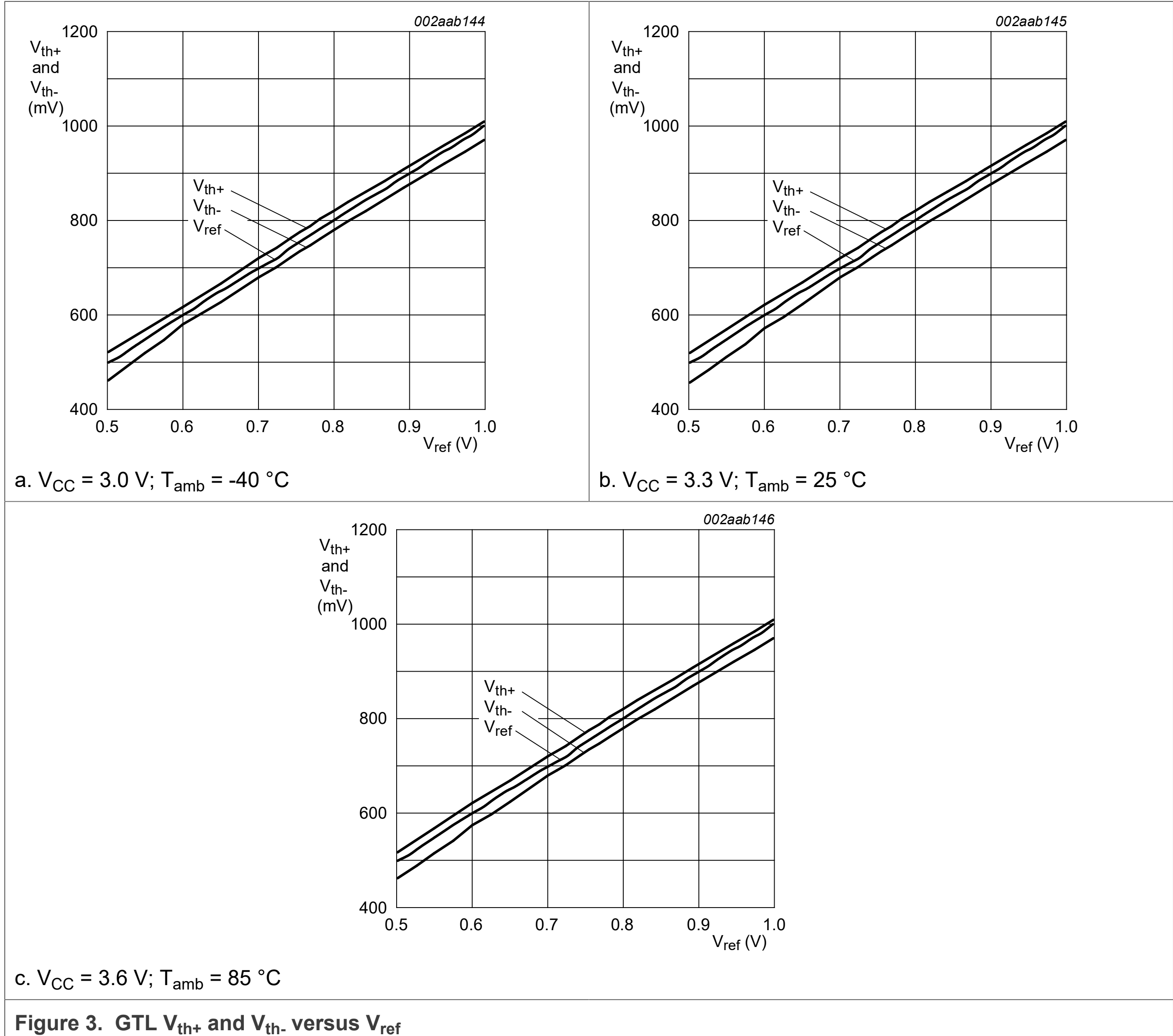


**Figure 3. GTL $V_{th+}$ and $V_{th-}$ versus $V_{ref}$**

## 11 Dynamic characteristics

**Table 9. Dynamic characteristics**

*$V_{CC}$ = 3.3 V ± 0.3 V*

| Symbol | Parameter | Conditions | | Min | Typ[1] | Max | Unit |
|---|---|---|---|---|---|---|---|
| **GTL-; $V_{ref}$ = 0.6 V; $V_{TT}$ = 0.9 V** | | | | | | | |
| $t_{PLH}$ | LOW-to-HIGH propagation delay | BIn to BOn; see Figure 4 | | - | 2.8 | 8 | ns |
| $t_{PHL}$ | HIGH-to-LOW propagation delay | | | - | 5.2 | 10 | ns |
| **GTL; $V_{ref}$ = 0.8 V; $V_{TT}$ = 1.2 V** | | | | | | | |



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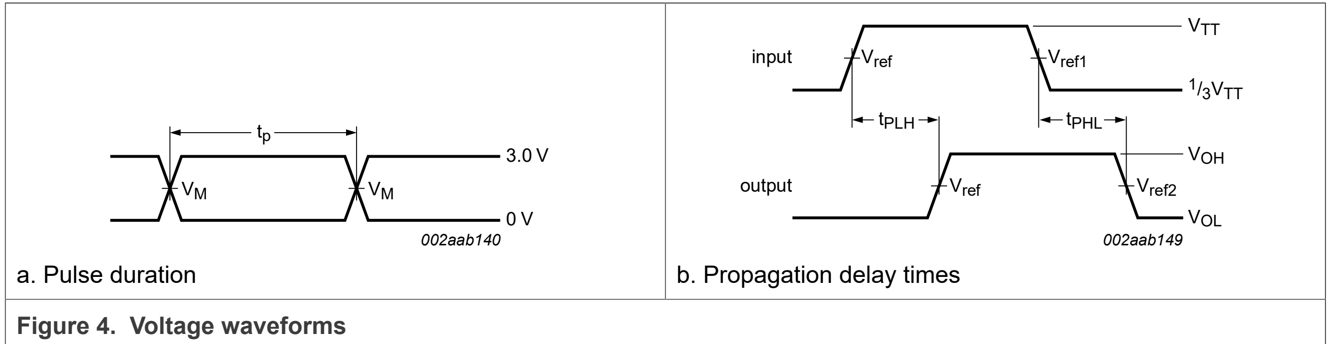
**Table 9. Dynamic characteristics**...*continued*
*$V_{CC}$ = 3.3 V ± 0.3 V*

| Symbol | Parameter | Conditions | | Min | Typ[1] | Max | Unit |
|---|---|---|---|---|---|---|---|
| $t_{PLH}$ | LOW-to-HIGH propagation delay | BIn to BOn; see Figure 4 | | - | 3.1 | 8 | ns |
| $t_{PHL}$ | HIGH-to-LOW propagation delay | | | - | 4.1 | 10 | ns |
| **GTL+; $V_{ref}$ = 1.0 V; $V_{TT}$ = 1.5 V** | | | | | | | |
| $t_{PLH}$ | LOW-to-HIGH propagation delay | BIn to BOn; see Figure 4 | | - | 3.3 | 8 | ns |
| $t_{PHL}$ | HIGH-to-LOW propagation delay | | | - | 3.6 | 10 | ns |

[1] All typical values are measured at $V_{CC}$ = 3.3 V and $T_{amb}$ = 25 °C.

### 11.1 Waveforms

$V_M = V_{ref}$ for B ports.

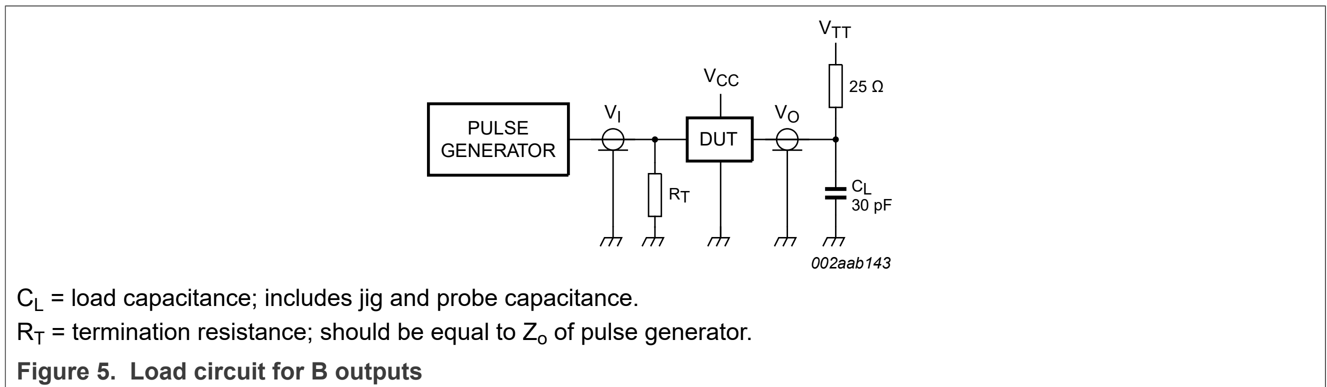



a. Pulse duration

b. Propagation delay times

**Figure 4. Voltage waveforms**

## 12 Test information




$C_L$ = load capacitance; includes jig and probe capacitance.
$R_T$ = termination resistance; should be equal to $Z_o$ of pulse generator.

**Figure 5. Load circuit for B outputs**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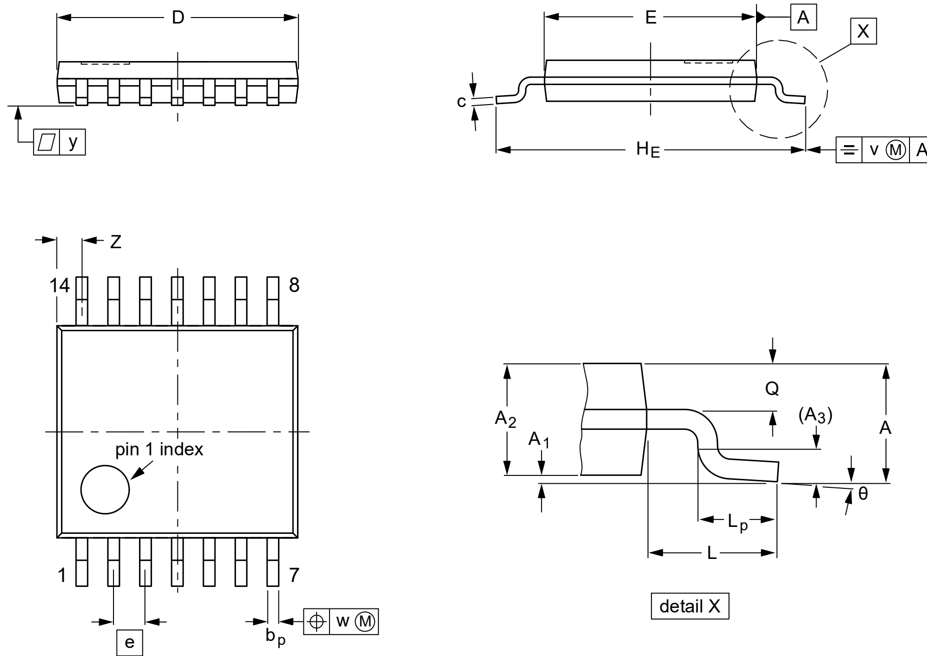
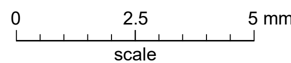
## 13 Package outline

**TSSOP14: plastic thin shrink small outline package; 14 leads; body width 4.4 mm** **SOT402-1**




**DIMENSIONS (mm are the original dimensions)**

| UNIT | A max. | $A_1$ | $A_2$ | $A_3$ | $b_p$ | c | D (1) | E (2) | e | $H_E$ | L | $L_p$ | Q | v | w | y | Z (1) | θ |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| mm | 1.1 | 0.15<br>0.05 | 0.95<br>0.80 | 0.25 | 0.30<br>0.19 | 0.2<br>0.1 | 5.1<br>4.9 | 4.5<br>4.3 | 0.65 | 6.6<br>6.2 | 1 | 0.75<br>0.50 | 0.4<br>0.3 | 0.2 | 0.13 | 0.1 | 0.72<br>0.38 | 8°<br>0° |

**Notes**

1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.
2. Plastic interlead protrusions of 0.25 mm maximum per side are not included.

| OUTLINE VERSION | REFERENCES | | | | EUROPEAN PROJECTION | ISSUE DATE |
|---|---|---|---|---|---|---|
| | IEC | JEDEC | JEITA | | | |
| SOT402-1 | | MO-153 | | | | ~~99-12-27~~<br>03-02-18 |

Figure 6. Package outline SOT402-1 (TSSOP14)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# 14 Soldering

This text provides a very brief insight into a complex technology. A more in-depth account of soldering ICs can be found in Application Note *AN10365 “Surface mount reflow soldering description”*.

## 14.1 Introduction to soldering

Soldering is one of the most common methods through which packages are attached to Printed Circuit Boards (PCBs), to form electrical circuits. The soldered joint provides both the mechanical and the electrical connection. There is no single soldering method that is ideal for all IC packages. Wave soldering is often preferred when through-hole and Surface Mount Devices (SMDs) are mixed on one printed wiring board; however, it is not suitable for fine pitch SMDs. Reflow soldering is ideal for the small pitches and high densities that come with increased miniaturization.

## 14.2 Wave and reflow soldering

Wave soldering is a joining technology in which the joints are made by solder coming from a standing wave of liquid solder. The wave soldering process is suitable for the following:

- Through-hole components
- Leaded or leadless SMDs, which are glued to the surface of the printed circuit board

Not all SMDs can be wave soldered. Packages with solder balls, and some leadless packages which have solder lands underneath the body, cannot be wave soldered. Also, leaded SMDs with leads having a pitch smaller than ~0.6 mm cannot be wave soldered, due to an increased probability of bridging.

The reflow soldering process involves applying solder paste to a board, followed by component placement and exposure to a temperature profile. Leaded packages, packages with solder balls, and leadless packages are all reflow solderable.

Key characteristics in both wave and reflow soldering are:

- Board specifications, including the board finish, solder masks and vias
- Package footprints, including solder thieves and orientation
- The moisture sensitivity level of the packages
- Package placement
- Inspection and repair
- Lead-free soldering versus SnPb soldering

## 14.3 Wave soldering

Key characteristics in wave soldering are:

- Process issues, such as application of adhesive and flux, clinching of leads, board transport, the solder wave parameters, and the time during which components are exposed to the wave
- Solder bath specifications, including temperature and impurities

## 14.4 Reflow soldering

Key characteristics in reflow soldering are:


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- Lead-free versus SnPb soldering; note that a lead-free reflow process usually leads to higher minimum peak temperatures (see Figure 7) than a SnPb process, thus reducing the process window
- Solder paste printing issues including smearing, release, and adjusting the process window for a mix of large and small components on one board
- Reflow temperature profile; this profile includes preheat, reflow (in which the board is heated to the peak temperature) and cooling down. It is imperative that the peak temperature is high enough for the solder to make reliable solder joints (a solder paste characteristic). In addition, the peak temperature must be low enough that the packages and/or boards are not damaged. The peak temperature of the package depends on package thickness and volume and is classified in accordance with Table 10 and Table 11

**Table 10. SnPb eutectic process (from J-STD-020D)**

| Package thickness (mm) | Package reflow temperature (°C) | |
|---|---|---|
| | Volume (mm³) | |
| | < 350 | ≥ 350 |
| < 2.5 | 235 | 220 |
| ≥ 2.5 | 220 | 220 |

**Table 11. Lead-free process (from J-STD-020D)**

| Package thickness (mm) | Package reflow temperature (°C) | | |
|---|---|---|---|
| | Volume (mm³) | | |
| | < 350 | 350 to 2000 | > 2000 |
| < 1.6 | 260 | 260 | 260 |
| 1.6 to 2.5 | 260 | 250 | 245 |
| > 2.5 | 250 | 245 | 245 |

Moisture sensitivity precautions, as indicated on the packing, must be respected at all times.

Studies have shown that small packages reach higher temperatures during reflow soldering, see Figure 7.



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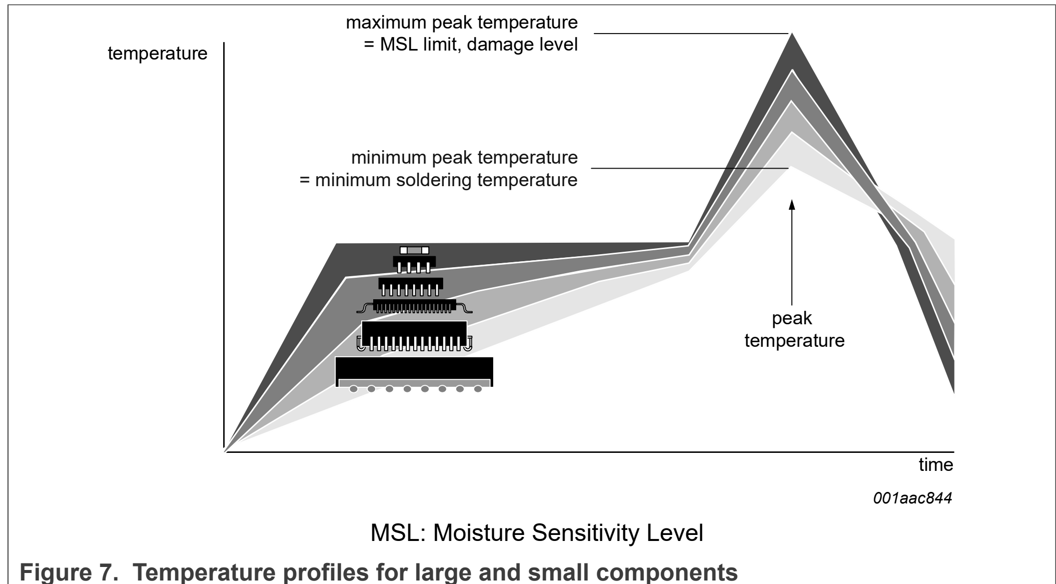


MSL: Moisture Sensitivity Level

**Figure 7. Temperature profiles for large and small components**

For further information on temperature profiles, refer to Application Note *AN10365 “Surface mount reflow soldering description”*.

## 15 Abbreviations

**Table 12. Abbreviations**

| Acronym | Description |
|---|---|
| CDM | Charged Device Model |
| ESD | ElectroStatic Discharge |
| GTL | Gunning Transceiver Logic |
| HBM | Human Body Model |
| TTL | Transistor-Transistor Logic |

## 16 Revision history

**Table 13. Revision history**

| Document ID | Release date | Data sheet status | Change notice | Supersedes |
|---|---|---|---|---|
| GTL2034 v.1.1 | 20211220 | Product data sheet | - | DOC_ID v.1.0 |
| Modifications | • The format of this data sheet has been redesigned to comply with the new identity guidelines of NXP Semiconductors. Legal texts have been adapted to the new company name where appropriate.<br>• Added orderable part number GTL2034PWZ. | | | |
| GTL2034 v.1.0 | 20051111 | Product data sheet | - | - |


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**Date of release: 20 December 2021**
**Document identifier: GTL2034**