

FHP3392 — Fixed-Gain, ±5V, Triple 2:1, High-Speed Video Multiplexer

Features

- 0.1dB gain flatness to 102MHz at 2V_{PP}
- 9ns channel switching time
- <0.02%/0.03° differential gain/phase error
- 750MHz large signal -3dB bandwidth
- 2,600V/μs slew rate
- 60mA output current (easily drives two video loads)
- 70dB channel to channel isolation
- 25mA supply current
- 7mA supply current when disabled
- Fully specified at ±5V supplies
- Lead-free TSSOP-24 package

Applications

- RGB video switchers and routers
- Multiple input HDTV switching
- Picture-in-picture video switch
- Multi-channel ADC Driver

Description

The FHP3392 (G=2) is a triple 2:1 analog multiplexer designed for high-speed video applications. The output amplifiers offer a fixed gain of 6dB and stellar large signal performance of 335MHz -3dB bandwidth and 80MHz 0.1dB bandwidth. The 2V_{PP} bandwidth performance and 1,600V/μs slew rate exceed the requirements of high-definition television (HDTV) and other multimedia applications. The output amplifier provides ample output current to drive multiple video loads.

The FHP3392 may be operated with dual power supplies from ±2.5V to ±6V.

The FHP3392 consumes only 25mA of supply current and offer disable capability. While disabled, it consumes only 7mA and the outputs become high impedance, allowing multiplexer expansion with multiple FHP3392s.

Ordering Information

| Part Number | Pb-Free | Gain | Operating Temperature Range | Package | Packing Method |
|----------------|---------|------|-----------------------------|--|----------------|
| FHP3392IMTC24X | Yes | 6dB | -40°C to +85°C | 24-Lead, Thin Shrink Outline Package, JEDEC MO-153, 4.4mm Wide | Tape and Reel |

Moisture sensitivity level for all parts is MSL-1.

Block Diagram and Pin Configuration

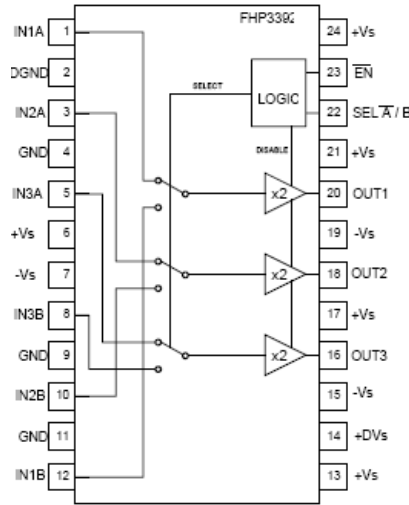


Figure 1. Block Diagram and Pin Configuration

Pin Definitions

| Pin # | Name | Description |
|-------|---------|---|
| 1 | IN1A | 1st Input Channel A |
| 2 | DGND | Digital Ground, must be connected to ground |
| 3 | IN2A | 2nd Input Channel A |
| 4 | GND | Must be connected to ground |
| 5 | IN3A | 3rd Input Channel A |
| 6 | +Vs | Positive supply |
| 7 | -Vs | Negative supply |
| 8 | IN3B | 3rd Input Channel B |
| 9 | GND | Must be connected to ground |
| 10 | IN2B | 2nd Input Channel B |
| 11 | GND | Must be connected to ground |
| 12 | IN1B | 1st Input Channel B |
| 13 | +Vs | Positive supply |
| 14 | +DVs | Digital positive supply |
| 15 | -Vs | Negative supply |
| 16 | OUT3 | 3rd output |
| 17 | +Vs | Positive supply |
| 18 | OUT3 | 2nd output |
| 19 | -Vs | Negative supply |
| 20 | OUT1 | 1st Output |
| 21 | +Vs | Logic input; "0" = Channel A, "1" = Channel B |
| 22 | SEL A/B | Enable pin; "0" = Enable, "1" = Disable; Enabled if left floating or grounded |
| 23 | EN | Enable Pin: "0" = Channel A, "1" = Channel B |
| 24 | +Vs | Positive supply |

Truth Table

| SEL A/B | EN | OUT |
|---------|----|-----------|
| 0 | 0 | Channel A |
| 1 | 0 | Channel B |
| X | 1 | Disable |

Absolute Maximum Ratings

Stresses exceeding the absolute maximum ratings may damage the device. The device may not function or be operable above the recommended operating conditions and stressing the parts to these levels is not recommended. In addition, extended exposure to stresses above the recommended operating conditions may affect device reliability. The absolute maximum ratings are stress ratings only.

| Symbol | Parameter | Min. | Max. | Unit |
|----------|---------------------|--------------|---------------|------|
| V_{CC} | Supply Voltage | 0 | 13.3 | V |
| V_{IN} | Input Voltage Range | $-V_S - 0.5$ | $+V_S + 0.5V$ | V |

Electrostatic Discharge Protection

| Symbol | Parameter | Min. | Max. | Unit |
|--------|----------------------------|------|------|------|
| ESD | Human Body Model (HBM) | | 3 | kV |
| | Charged Device Model (CDM) | | 12 | kV |

Reliability Information

| Symbol | Parameter | Min. | Typ. | Max. | Unit |
|---------------|----------------------|------|------|------|------|
| T_J | Junction Temperature | | | 150 | °C |
| T_{STG} | Storage Temperature | -65 | | 150 | °C |
| T_{RF} | Reflow Temperature | | | 260 | °C |
| θ_{JA} | Thermal Resistance | | 87 | | °C/W |

Note:

1. Thermal Resistance (θ_{JA}) JEDEC standard, multi-layer test boards, in still air.

Recommended Operating Conditions

The Recommended Operating Conditions table defines the conditions for actual device operation. Recommended operating conditions are specified to ensure optimal performance to the datasheet specifications. Fairchild does not recommend exceeding them or designing to Absolute Maximum Ratings.

| Symbol | Parameter | Min. | Typ. | Max. | Unit |
|----------|-----------------------------|------|------|------|------|
| T_A | Operating Temperature Range | -40 | | +85 | °C |
| V_{CC} | Supply Voltage Range | ±2.5 | ±5.0 | ±6.0 | V |

Electrical Characteristics at ±5V

$T_A = 25^\circ\text{C}$, $V_S = \pm 5\text{V}$, $R_L = 150\Omega$; unless otherwise noted.

| Symbol | Parameter | Conditions | Min. | Typ. | Max. | Units |
|------------------------------------|--|---|------|------|------|------------------|
| Frequency Domain Response | | | | | | |
| BW_{SS} | -3dB Bandwidth | $V_{OUT} = 0.2V_{PP}$ | | 750 | | MHz |
| BW_{LS} | Large Signal Bandwidth | $V_{OUT} = 2.0V_{PP}$ | | 560 | | MHz |
| $BW_{0.1dBSS}$ | 0.1dB Gain Flatness | $V_{OUT} = 0.2V_{PP}$ | | 117 | | MHz |
| $BW_{0.1dBLS}$ | 0.1dB Gain Flatness | $V_{OUT} = 2.0V_{PP}$ | | 102 | | MHz |
| Time Domain Response | | | | | | |
| t_s | Settling Time to 0.1% | $V_{OUT} = 2\text{V step}$ | | 4 | | ns |
| SR | Slew Rate | 4V step | | 2600 | | V/ μs |
| Distortion / Noise Response | | | | | | |
| HD2 | Second Harmonic Distortion | $2V_{PP}$, 5MHz | | -85 | | dBc |
| HD3 | Third Harmonic Distortion | $2V_{PP}$, 5MHz | | -90 | | dBc |
| THD | Total Harmonic Distortion | $2V_{PP}$, 5MHz | | -84 | | dB |
| | | $2V_{PP}$, 22MHz | | -72 | | dB |
| DG | Differential Gain | NTSC (3.58MHz) | | 0.04 | | % |
| DP | Differential Phase | NTSC (3.58MHz) | | 0.01 | | ° |
| e_n | Input Voltage Noise | >1MHz | | 6.75 | | nV/Hz |
| i_n | Input Current Noise | >1MHz | | 22 | | pA/Hz |
| SNR | Signal-to-Noise Ratio | NTC-7 weighting, 4.2MHz LP filter, 100kHz PH filter | | 90 | | dB |
| X_{talk} | All Hostile Crosstalk | $V_{OUT} = 2V_{PP}$, ch-to-ch, 5MHz | | -59 | | dB |
| | | $V_{OUT} = 2V_{PP}$, ch-to-ch, 30MHz | | -56 | | |
| DC Performance | | | | | | |
| V_{OS} | Output Offset Voltage ⁽²⁾ | $V_{IN} = 0$ | -18 | 2 | 18 | mV |
| I_b | Input Bias Current ⁽²⁾ | | -30 | 4 | 30 | μA |
| G | Gain ⁽²⁾ | DC | 1.9 | 2.0 | 2.1 | V/V |
| GM | Gain Matching | Channel-to-channel, DC | | 0.05 | | % |
| PSRR | Power Supply Rejection Ratio ⁽²⁾ | DC, $V_{CM} = 0$, input referred, SEL = X | 54 | 62 | | dB |
| I_S | Supply Current ⁽²⁾ | No load, $\overline{EN} = 0$ | | 25 | 30 | mA |
| I_{EN} | Disable Supply Current ⁽²⁾ | $\overline{EN} = 1$ | | 7 | 10 | mA |
| Switching Characteristics | | | | | | |
| T_S | Switching Time 50% Logic to: | Channel-to channel | | | | |
| | 90% Output (10% Output Setting) ⁽³⁾ | Ch A inputs = +0.5V Ch B inputs = -0.5V | | 17.3 | | ns |
| | 99% Output (1% Output Setting) ⁽³⁾ | Ch A inputs = +0.5V Ch B inputs = -0.5V | | 36 | | ns |
| V_{SW} | Channel Switching Transient (Glitch) | All inputs grounded | | 34 | | mV _{PP} |

Notes:

- 100% tested at 25°.
- EN pin is grounded, channel A inputs = 0.5V, channel B inputs = -0.5V. Switching time is the transition time from 50% of SEL input value (+2.5V) to the time at which the switched channel is at 90% (or 99%) of its final value.

Electrical Characteristics at ±5V (Continued)T_A = 25°C, V_S = ± 5V, R_L = 150Ω; unless otherwise noted.

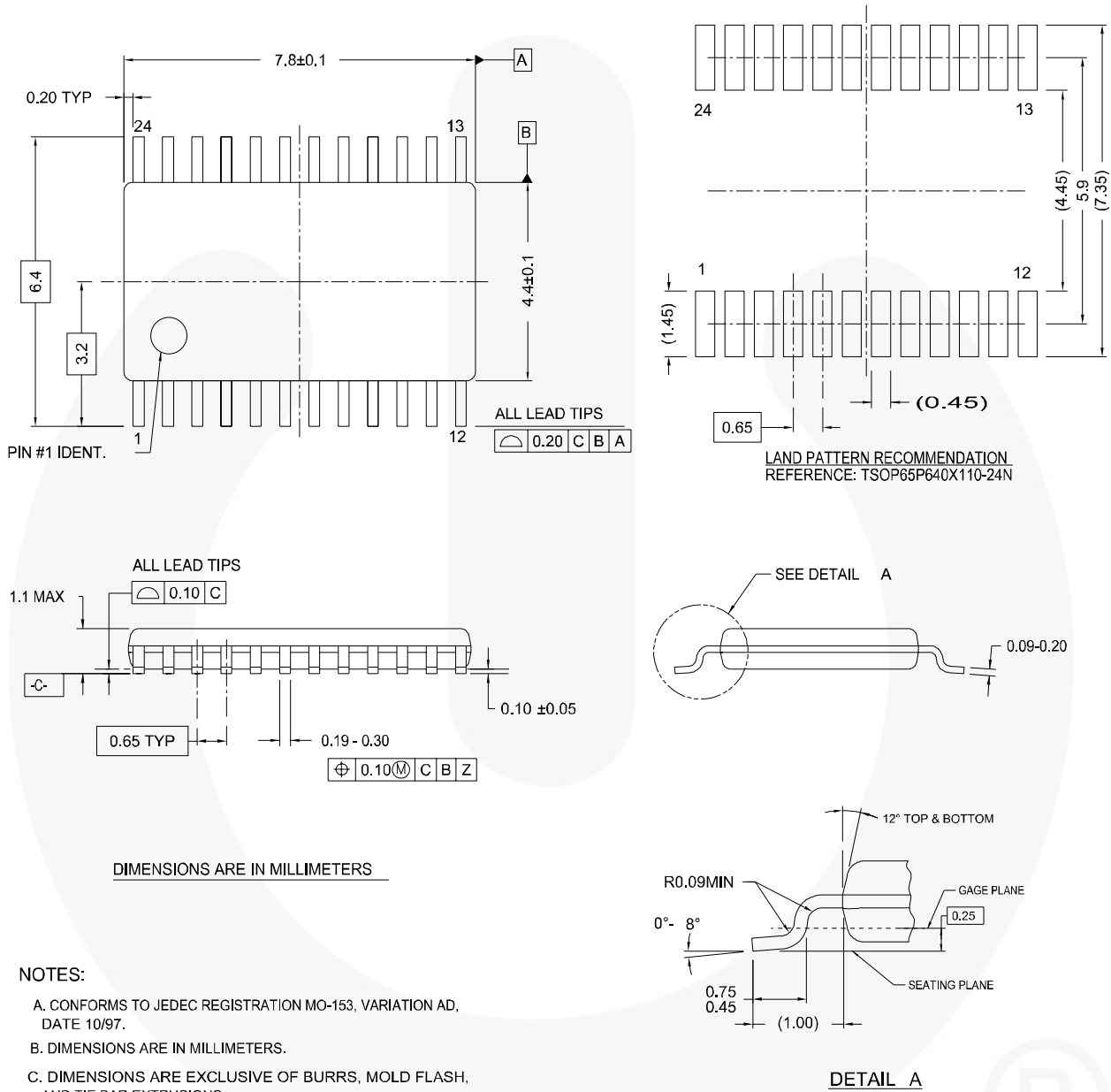
| Symbol | Parameter | Conditions | Min. | Typ. | Max. | Units |
|--------------------------------|--------------------------------|--|------|------|------|-------|
| Digital Inputs | | | | | | |
| V _{IH} | Logic HIGH Threshold | SEL and $\overline{\text{EN}}$ pins ⁽⁴⁾ | 2.0 | | | V |
| V _{IL} | Logic LOW Threshold | SEL and $\overline{\text{EN}}$ pins ⁽⁴⁾ | | | 0.8 | V |
| I _{IH} | Logic Pin Input Current HIGH | SEL and $\overline{\text{EN}}$ pins; Logic Input = 2V | | 27 | | μA |
| I _{IL} | Logic Pin Input Current LOW | SEL and $\overline{\text{EN}}$ pins; Logic Input = 0V | | 0 | | μA |
| Disable Characteristics | | | | | | |
| EN _{ISO} | Disable Isolation | 5MHz, V _{IN} = 1V _{PP} , EN = 1 | | -81 | | dB |
| | | 30MHz, V _{IN} = 1V _{PP} , EN = 1 | | -66 | | dB |
| CH _{ISO} | Channel-to-Channel Isolation | 5MHz | | -71 | | dB |
| ENT _{ON} | Turn-on-Time (Disable to ON) | V _{IN} = 0.5V | | 30 | | ns |
| ENT _{OFF} | Turn-off-Time (ON to Disable) | V _{IN} = 0.5V | | 65 | | ns |
| Input Characteristics | | | | | | |
| R _{IN} | Input Resistance | | | 115 | | kΩ |
| C _{IN} | Input Capacitance | | | 10 | | pF |
| V _{IN} | Input Voltage Range | | | ±2 | | V |
| Output Characteristics | | | | | | |
| V _O | Output Voltage Swing | R _L = 2kΩ | | ±4 | | V |
| | | R _L = 150Ω ⁽⁴⁾ | ±3.2 | ±3.7 | | V |
| I _{OUT} | Linear Output Current | | | ±95 | | mA |
| I _{SC} | Short Circuit Output Current | V _O = GND | | ±100 | | mA |
| R _{OUT} | Output Resistance, Closed Loop | Enabled, $\overline{\text{EN}}$ = 1, 100kHz | | 0.17 | | Ω |
| | | Disabled, $\overline{\text{EN}}$ = 1, 100kHz | | 675 | | Ω |
| C _{OUT} | Output Capacitance | Disabled, $\overline{\text{EN}}$ = 1, 100kHz | | 2.7 | | pF |

Note:

4. 100% tested at 25°.

Physical Dimensions

Dimensions are in millimeters unless otherwise noted.



NOTES:

- A. CONFORMS TO JEDEC REGISTRATION MO-153, VARIATION AD, DATE 10/97.
- B. DIMENSIONS ARE IN MILLIMETERS.
- C. DIMENSIONS ARE EXCLUSIVE OF BURRS, MOLD FLASH, AND TIE BAR EXTRUSIONS.
- D. DIMENSIONS AND TOLERANCES PER ANSI Y14.5M, 1994
- E. DRAWING FILE NAME: MTC24REV4

MTC24REV4

Figure 2. 24-Lead, Thin Shrink Outline Package, JEDEC MO-153, 4.4mm Wide



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Rev. 130