ADSANTEC
Ultra High-Speed Mixed Signal ASICs

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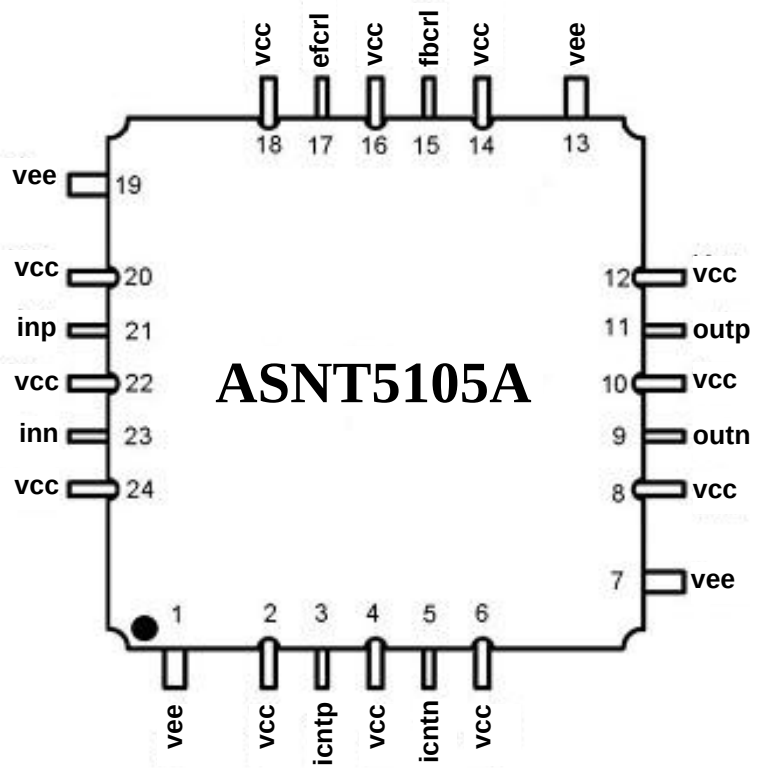
# ASNT5105A-KMC
# DC-50*Gbps*/32*GHz* Signal Phase Shifter

- Broadband (DC-50*Gbps* / 32*GHz*) tunable data / clock phase shifter
- Delay adjustment range up to 110*ps*
- On-chip automatic common mode offset compensation circuitry
- Manual frequency response adjustment for jitter minimization
- Limited temperature variation over industrial temperature range
- 1*GHz* of bandwidth for the phase adjustment tuning port
- Fully differential CML input interface
- Fully differential CML output interface with 450*mV* single-ended swing
- Single +3.3*V* or -3.3*V* power supply
- Power consumption: 1.25*W*
- Fabricated in SiGe for high performance, yield, and reliability
- Custom CQFP 24-pin package



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# DESCRIPTION

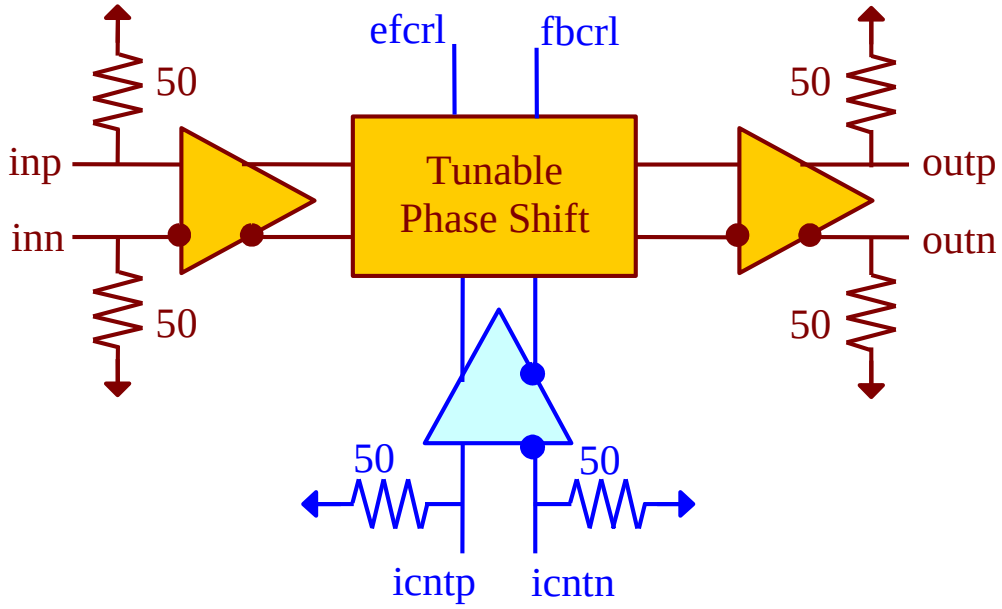


*Fig. 1. Functional Block Diagram*

ASNT5105A-KMC is a data/clock variable delay line fabricated in SiGe technology. The IC shown in Fig. 1 provides an adjustable delay of its differential output signal outp/outn in relation to its broadband input signal inp/inn. The delay is controlled through a wide-band differential tuning port icntp/icntn. The chip incorporates an automatic common-mode offset cancellation circuit that operates with either clock signals or data signals with balanced patterns. In case of non-balanced data patterns, the circuit should be disabled through control port fbcrl. The single-ended control port efcrl can be used to manipulate internal peaking in the delay block in order to adjust the part's frequency response and thus improve output eye diagrams for various data rates and operating conditions.

The part's I/Os support the CML logic interface with on chip 50*Ohm* termination to vcc and may be used differentially, AC/DC coupled, single-ended, or in any combination (see also POWER SUPPLY CONFIGURATION). In the DC-coupling mode, the input signal's common mode voltage should comply with the specifications shown in ELECTRICAL CHARACTERISTICS. In the AC-coupling mode, the input termination provides the required common mode voltage automatically. The differential DC signaling mode is recommended for optimal performance.

## Feedback Control Port

This part has two internal duty cycle correction feedback loops. In case of non-balanced data pattern with a different average numbers of logic "0"s and logic "1"s, the feedbacks may be set to lower gain or disabled completely. This is achieved by adjustment of currents inside feedback amplifiers through single-ended tuning port fbcrl. Higher control voltages result in higher amplifier currents and higher total feedback gain. If the port is left not connected, it defaults to vcc that corresponds to the maximum feedback gain.

For normal operation with either a balanced data or clock signal, fbcrl should be left not connected or connected to vcc. For normal operation with a non-balanced code, fbcrl should be connected to vee.

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## Internal Peaking Control Port

Depending on the data rate and operational conditions, excessive peaking in the internal delay stages may lead to output signal degradation that results, for example, in additional jitter. At the same time, insufficient peaking may lead to the part's speed degradation. Internal peaking can be adjusted by varying currents of internal emitter followers through a single-ended port efcrl. Higher control voltages result in higher emitter follower currents, and higher internal peaking. If this port is left not connected, it defaults to an internal level of vcc-0.75*V* that corresponds to a medium level of peaking.

Generally, lower control voltages result in lower jitter and lower speed. Thus, higher input data rates require higher efcrl voltage levels as shown in Table 1 for sinusoidal input signal.

*Table 1. Recommended efcrl Settings for Sinusoidal Input Signal*

| F input, *GHz* | Min voltage, *V* | Max voltage, *V* |
|---|---|---|
| <24 | vcc-0.72 | vcc |
| 24-26 | vcc-0.72 | vcc |
| 26-28 | vcc-0.6 | vcc |
| 28-29 | vcc-0.6 | vcc |
| >29 | vcc-0.4 | vcc |

## Delay Control Port

The delay is controlled through a wide-band differential tuning port icntp/icntn. The measured delay control diagram is shown in Fig. 2.

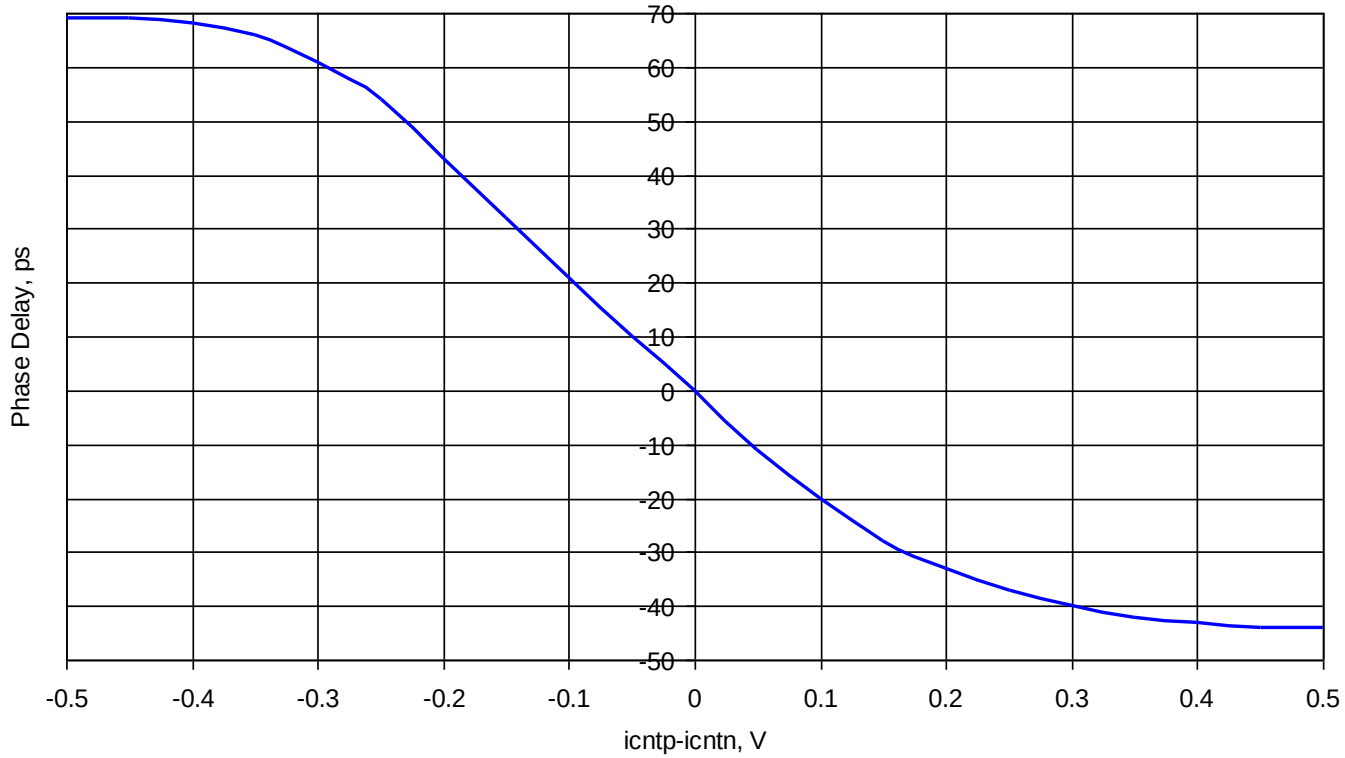


*Fig. 2. Measured Delay Control Diagram*

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# POWER SUPPLY CONFIGURATION

The part can operate with either a negative supply (vcc = 0.0*V*=ground and vee = -3.3*V*), or a positive supply (vcc = +3.3*V* and vee = 0.0*V*=ground). In case of the positive supply, all I/Os need AC termination when connected to any devices with 50*Ohm* termination to ground. Different PCB layouts will be needed for each different power supply combination.

**All the characteristics detailed below assume vcc = 0.0*V* and vee = -3.3*V*.**

# ABSOLUTE MAXIMUM RATINGS

Caution: Exceeding the absolute maximum ratings shown in Table 2 may cause damage to this product and/or lead to reduced reliability. Functional performance is specified over the recommended operating conditions for power supply and temperature only. AC and DC device characteristics at or beyond the absolute maximum ratings are not assumed or implied. All min and max voltage limits are referenced to ground (assumed vcc).

*Table 2. Absolute Maximum Ratings*

| Parameter | Min | Max | Units |
|---|---|---|---|
| Supply Voltage (vee) | | -3.6 | *V* |
| Power Consumption | | 1.4 | *W* |
| RF Input Voltage Swing (SE) | | 1.0 | *V* |
| Case Temperature | | +90 | *ºC* |
| Storage Temperature | -40 | +100 | *ºC* |
| Operational Humidity | 10 | 98 | *%* |
| Storage Humidity | 10 | 98 | *%* |

# TERMINAL FUNCTIONS

| TERMINAL | | | DESCRIPTION |
|---|---|---|---|
| **Name** | **No.** | **Type** | |
| **High-Speed I/Os** | | | |
| inp | 21 | CML input | Differential high-speed signal inputs with internal SE 50*Ohm* termination to vcc |
| inn | 23 | | |
| icntp | 3 | Input | Differential low-speed control inputs with internal SE 50*Ohm* termination to vcc |
| icntn | 5 | | |
| outp | 11 | CML output | Differential high-speed signal outputs with internal SE 50*Ohm* termination to vcc. Require external SE 50*Ohm* termination to vcc |
| outn | 9 | | |
| **Digital Controls** | | | |
| fbcrl | 15 | Input | SE DC control input terminated to vcc. (In most cases should be left not connected or connected to vcc) |
| efcrl | 17 | Input | SE DC control input terminated to internal resistive divider between vee and vcc |

| **Supply And Termination Voltages** | | |
|---|---|---|
| **Name** | **Description** | **Pin Number** |
| vcc | Positive power supply (+3.3*V* or 0) | 2, 4, 6, 8, 10, 12, 14, 16, 18, 20, 22, 24 |
| vee | Negative power supply (0*V* or -3.3*V*) | 1, 7, 13, 19 |

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# ELECTRICAL CHARACTERISTICS

| PARAMETER | MIN | TYP | MAX | UNIT | COMMENTS |
|---|---|---|---|---|---|
| **General Parameters** | | | | | |
| vee | -3.1 | -3.3 | -3.5 | *V* | ±6% |
| vcc | | 0.0 | | *V* | External ground |
| *I*vee | | 380 | | *mA* | efcrl at max |
| | | 270 | | *mA* | efcrl at min |
| Power consumption | | 1.25 | | *W* | efcrl at max |
| | | 890 | | *mW* | efcrl at min |
| Junction temperature | -25 | 50 | 125 | *°C* | |
| **HS Input Data/Clock (inp/inn)** | | | | | |
| Data Rate | DC | | 50 | *Gbps* | |
| Frequency | DC | | 32 | *GHz* | For clock signals |
| Swing | 0.05 | | 1.0 | *V* | Differential or SE, p-p |
| CM Voltage Level | vcc-0.8 | | vcc | *V* | Must match for both inputs |
| **HS Output Data/Clock (outp/outn)** | | | | | |
| Data Rate | DC | | 50 | *Gbps* | |
| Frequency | DC | | 32 | *GHz* | For clock signals |
| Logic “1” level | | vcc | | *V* | |
| Logic “0” level | | vcc-0.45 | | *V* | With external 50*Ohm* DC termination |
| Rise/Fall times | 9 | | 11 | *ps* | 20%-80% |
| Output Jitter | | | 1.5 | *ps* | Peak-to-peak |
| Duty cycle | 45 | 50 | 55 | *%* | For clock signal |
| **DC Offset Cancellation Control (fbcrl)** | | | | | |
| Logic “1” level | | vcc | | *V* | |
| Logic “0” level | | vee | | *V* | |
| **Output-to-Input Delay** | | | | | |
| Phase shift | 0 | | 110 | *ps* | For the full range of icntp/icntn signals |
| Phase shift stability | -12 | | 12 | *ps* | 0-125°C |
| Absolute delay stability | -14 | | 14 | *ps* | 0-125°C |
| **Tuning port (icntp/icntn)** | | | | | |
| Bandwidth | DC | | 1000 | *MHz* | |
| SE voltage level | vcc-500 | | vcc | *mV* | Half control range when the opposite pin is at vcc |
| SE voltage level | vcc-1000 | | vcc | *mV* | Full control range when the opposite pin is at vcc-0.6*V* |
| Differential swing | 0 | | 1000 | *mV* | Peak-peak. Full control range |
| CM Level | vcc-(Diff. swing)/4 | | | *V* | In differential mode |
| **Tuning port (fbcrl)** | | | | | |
| Control voltage range | vee | | vcc | *mV* | Default voltage is vcc |
| **Tuning port (efcrl)** | | | | | |
| Control voltage range | vcc-1500 | | vcc | *mV* | Default voltage is vcc-0.75V |

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# PACKAGE INFORMATION

The chip die is housed in a custom 24-pin CQFP package shown in Fig. 3. The package provides a center heat slug located on its back side to be used for heat dissipation. ADSANTEC recommends for this section to be soldered to the vcc plain, which is ground for a negative supply, or power for a positive supply.

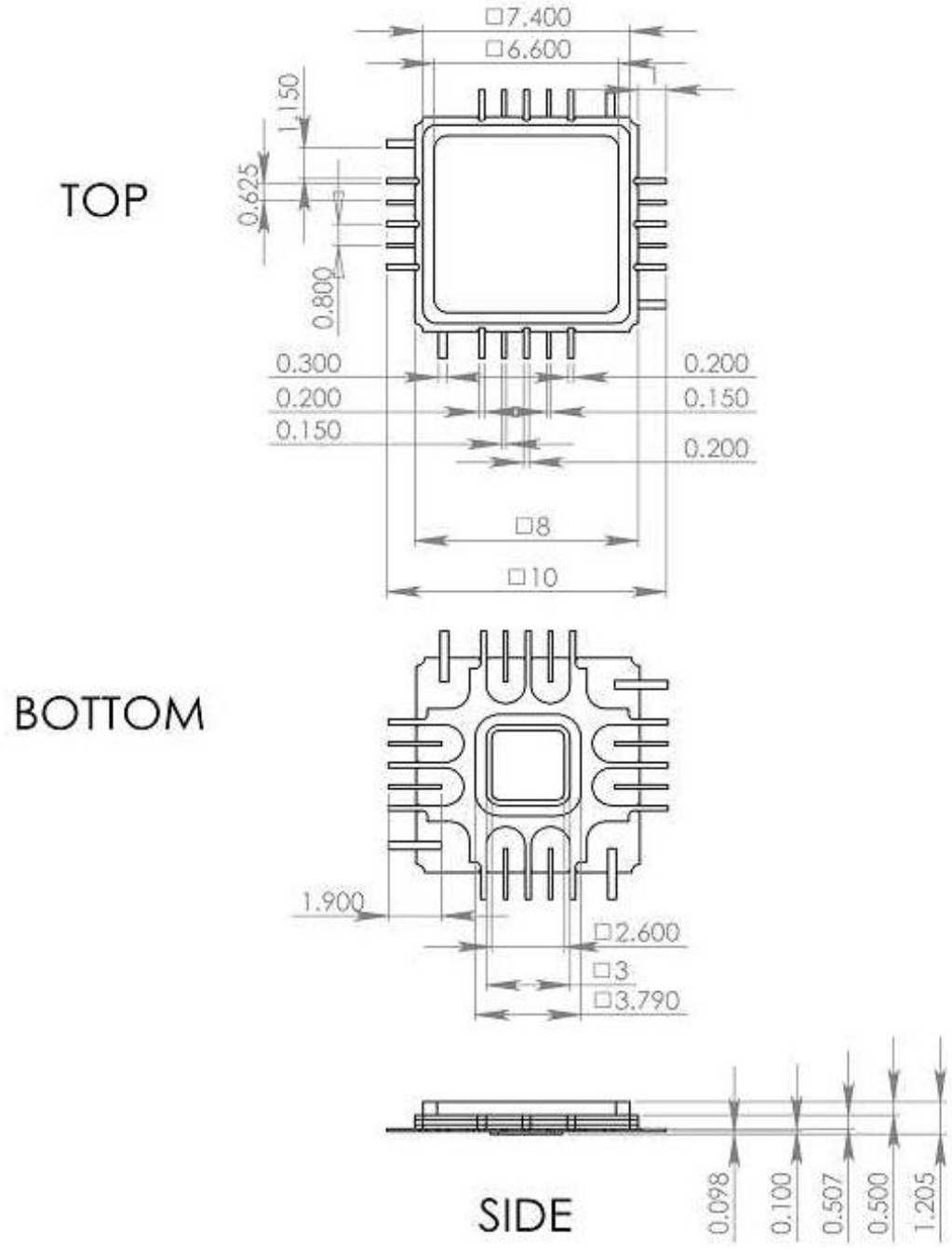


*Fig. 3. CQFP 24-Pin Package Drawing (All Dimensions in mm)*

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The part's identification label is ASNT5105A-KMC. The first 9 characters of the name before the dash identify the bare die including general circuit family, fabrication technology, specific circuit type, and part version while the 3 characters after the dash represent the package's manufacturer, type, and pin out count.

This device complies with the Restriction of Hazardous Substances (RoHS) per 2011/65/EU for all ten substances.

# REVISION HISTORY

| Revision | Date | Changes |
|---|---|---|
| 1.3.2 | 01-2020 | Updated Package Information |
| 1.2.2 | 07-2019 | Updated Letterhead |
| 1.2.1 | 08-2018 | Added efcrl settings (Table 1) |
| 1.1.1 | 09-2015 | Revised operating frequency range<br>Revised title<br>Revised description<br>Revised electrical characteristics section |
| 1.0.1 | 06-2015 | First release |