Mercury CA1 FPGA Module

User Manual

Purpose

The purpose of this document is to present the characteristics of Mercury CA1 FPGA module to the user, and to provide the user with a comprehensive guide to understanding and using the Mercury CA1 FPGA module.

Summary

This document first gives an overview of the Mercury CA1 FPGA module followed by a detailed description of its features and configuration options. In addition, references to other useful documents are included.

Product Information	Code	Name
Product	ME-CA1	Mercury CA1 FPGA Module

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Copyright Reminder

Document History

Version	Date	Author	Comment
06	16.02.2021	DIUN	Cleaned-up product variants, added information on Mercury heatsinks, added Mercury+ ST1 to accesories section, added information on FPGA fuses and warranty, on differential I/Os, on voltage monitoring outputs, other style updates
05	25.07.2019	DIUN	Added information on power supplies and heat sink, updated DDR memory and SPI flash types, other style updates. Added information on R6.1 modules.
04	21.08.2018	DIUN	Minor corrections and style updates
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02	04.05.2017	DIUN	Updated EEPROM map, block diagram and footprint information
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1 Overview

1.1 General

1.1.1 Introduction

The Mercury CA1 FPGA module combines the low-cost Intel® Cyclone® IV FPGA device with DDR2 SDRAM, FTDI USB 2.0 controller, Gigabit Ethernet, LVDS I/Os, forming a high-performance and low-cost processing system ideal for high-speed and DSP applications.

The use of the Mercury CA1 FPGA module, in contrast to building a custom FPGA hardware, significantly simplifies system design and thus shortens time to market and decreases the development effort of your product.

Together with Mercury base boards, the Mercury CA1 FPGA module allows the user to quickly build a system prototype and start with application development.

1.1.2 Warranty

Please refer to the General Business Conditions, available on the Enclustra website [1].

Warning!

Please note that the warranty of an Enclustra module is voided if the FPGA fuses are blown. This operation is done at own risk, as it is irreversible. Enclustra cannot test the module in case of a warranty product return.

1.1.3 RoHS

The Mercury CA1 FPGA module is designed and produced according to the Restriction of Hazardous Substances (RoHS) Directive (2011/65/EC).

1.1.4 Disposal and WEEE

The Mercury CA1 FPGA module must be properly disposed of at the end of its life.

The Waste Electrical and Electronic Equipment (WEEE) Directive (2002/96/EC) is not applicable for the Mercury CA1 FPGA module.

1.1.5 Safety Recommendations and Warnings

Mercury modules are not designed to be "ready for operation" for the end-user. These can only be used in combination with suitable base boards. Proper configuration of the hardware before usage is required.

Ensure that the power supply is disconnected from the board before inserting or removing the Mercury CA1 FPGA module, connecting interfaces, or connecting jumpers.

Touching the capacitors of the DC-DC converters can lead to voltage peaks and permanent damage; overvoltage on power or signal lines can also cause permanent damage to the module.

Warning!

It is possible to mount the Mercury CA1 FPGA module the wrong way round on the base board - always check that the mounting holes on the base board are aligned with the mounting holes of the Mercury CA1 FPGA module.

The base board and module may be damaged if the module is mounted the wrong way round and powered up.

1.1.6 Electrostatic Discharge

Electronic boards are sensitive to electrostatic discharge (ESD). Please ensure that the product is handled with care and only in an ESD-protected environment.

1.1.7 Electromagnetic Compatibility

The Mercury CA1 FPGA module is a Class A product (as defined in IEC 61000-3-2 standard) and is not intended for use in domestic environments. The product may cause electromagnetic interference, for which appropriate measures must be taken.

1.2 Features

- Intel Cyclone IV 60 nm FPGA EP4CE30/EP4CE75/EP4CE115, FBGA 484 package
- Up to 168 user I/Os up to 3.3 V, available in one of the following combinations:
  - 25 differential pairs and 98 single-ended I/Os
  - 146 single-ended I/Os
  - 168 single-ended I/Os (in custom configuration where the differential input termination resistors are removed)
- Up to 256 MB DDR2 SDRAM
- 16 MB SPI flash
- Gigabit Ethernet
- FTDI USB 2.0 device controller
- Real-time clock
- Power and current monitor
- Small form factor (56 × 54 mm)
- 5 to 15 V supply voltage

1.3 Deliverables

- Mercury CA1 FPGA module
- Mercury CA1 FPGA module documentation, available via download:
  - Mercury CA1 FPGA Module User Manual (this document)
  - Mercury CA1 FPGA Module Reference Design [2]
  - Mercury CA1 FPGA Module IO Net Length Excel Sheet [3]
  - Mercury CA1 FPGA Module FPGA Pinout Excel Sheet [4]
  - Mercury CA1 FPGA Module User Schematics (PDF) [5]
  - Mercury CA1 FPGA Module Known Issues and Changes [6]
  - Mercury CA1 FPGA Module Footprint (Altium, Eagle, Orcad and PADS) [7]
  - Mercury CA1 FPGA Module 3D Model (PDF) [8]
  - Mercury CA1 FPGA Module STEP 3D Model [9]
  - Mercury Mars Module Pin Connection Guidelines [10]
  - Mercury Master Pinout [11]
  - Mercury Heatsink Application Note [15]

1.4 Accessories

1.4.1 Reference Design

The Mercury CA1 FPGA module reference design features an example configuration for the Cyclone IV FPGA device, together with an example top level HDL file for the user logic.

A number of software applications are available for the reference design, that show how to initialize the peripheral controllers and how to access the external devices. Pre-compiled binaries are included in the archive, so that the user can easily check that the hardware is functional.

The reference design can be downloaded from the Enclustra download page [2].

1.4.2 Enclustra Heat Sink

For Mercury modules an Enclustra heat sink is available for purchase along with the product. Please refer to section 2.10.6 for further information on the available cooling options.

1.4.3 Mercury+ PE1 Base Board

- 168-pin Hirose FX10 module connectors (PE1-200: 2 connectors; PE1-300/400: 3 connectors)
- System controller
- Power control
- System monitor (PE1-300/400)
- Current sense (PE1-300/400)
- Low-jitter clock generator (PE1-300/400)
- microSD card holder
- User EEPROM
- eMMC managed NAND flash (PE1-300/400)
- PCIe ×4 interface
- USB 3.0 device connector
- USB 2.0 host connector (PE1-200: 1 connector; PE1-300/400: 4 connectors)
- Micro USB 2.0 device (UART, SPI, I2C, JTAG) connector
- 2 × RJ45 Gigabit Ethernet connectors
- mPCIe/mSATA card holder (USB only) (PE1-300/400)
- SIM card holder (optional, PE1-300/400 only)
- SMA clock and data in/out (optional, PE1-300/400 only)
- 1 × FMC LPC connector (PE1-200)
- 1 × FMC HPC connector (PE1-300)
- 2 × FMC LPC connector (PE1-400)
- 2 × 40-pin Anios pin header
- 3 × 12-pin IO headers
- 5 to 15 V DC supply voltage
- USB bus power (with restrictions)

Please note that the available features depend on the equipped Mercury module type and on the selected base board variant.

1.4.4 Mercury+ ST1 Base Board

- 168-pin Hirose FX10 module connectors (3 connectors)
- 2 × MIPI D-PHY connectors: CSI and CSI/DSI (requires FPGA support)
- Mini DisplayPort connector (requires FPGA support)
- HDMI connector (requires FPGA support)
- SFP+ connector
- Low-jitter clock generator
- USB 3.0 device connector

- USB 3.0 host connector
- FTDI USB 2.0 device controller with micro USB device connector (UART, SPI, I2C, JTAG)
- 2 × RJ45 Gigabit Ethernet connectors
- 1 × FMC HPC connector (note: not all pins are available)
- 2 × 40-pin Anios pin header
- 3 × 12-pin IO headers
- microSD card holder
- 5 to 15 V DC supply voltage
- Form factor: 100 × 120 mm

Please note that the available features depend on the equipped Mercury module type.

1.5 Intel Tool Support

The FPGA devices equipped on the Mercury CA1 FPGA module are supported by the Quartus Prime Lite Edition (or Quartus II Web Edition, for older software versions), which is available free of charge. Please contact Intel for further information.

2 Module Description

2.1 Block Diagram

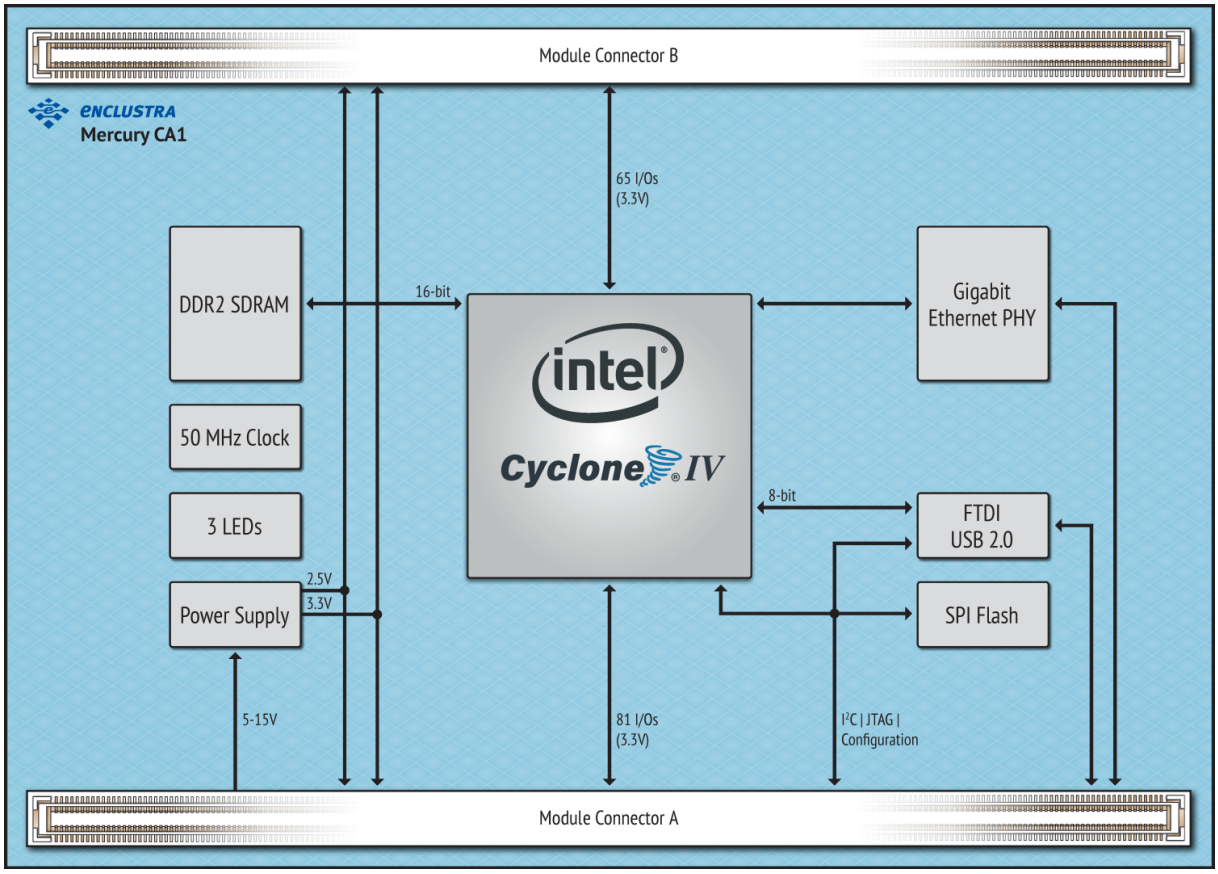

Figure 1: Hardware Block Diagram

The main component of the Mercury CA1 FPGA module is the Intel Cyclone IV FPGA device. Most of its I/O pins are connected to the Mercury module connectors, making 25 differential pairs and 98 single-ended user I/Os or 146 single-ended user I/Os (168 in custom configuration where the differential input termination resistors are removed) available to the user.

The FPGA device can be configured with a bitstream residing in the on-board SPI flash, via FTDI USB 2.0 controller fitted on the module, via an external microcontroller or via the JTAG interface connected to Mercury module connector.

The memory subsystem is built from a 16 MB SPI flash and 128 or 256 MB DDR2 SDRAM in the standard configuration.

Further, the module is equipped with a Gigabit Ethernet PHY, making it ideal for communication applications.

An FTDI USB 2.0 controller is fitted on the module to easily implement a communication link to a host PC.

A real-time clock is available on the module and is connected to the global I2C bus. A power and current monitor may be optionally equipped on the module and connected to the global I2C bus.

On-board clock generation is based on a 50 MHz crystal oscillator.

The module's internal supply voltages are generated from a single input supply of 5 - 15 V DC. Some of these voltages are available on the Mercury module connectors to supply circuits on the base board.

Up to four LEDs are connected to the FPGA pins for status signaling. Another LED is connected to the FTDI USB 2.0 controller user pin for the same purpose.

2.2 Module Configuration and Product Codes

Table 1 describes the available standard module configurations. Custom configurations are available; please contact Enclustra for further information.

Product Code	FPGA	DDR2 SDRAM	FTDI USB 2.0	Temperature Range
ME-CA1-30-8C-D7	EP4CE30F23C8N	128 MB	✓	0 to +70° C
ME-CA1-75-8C-D7	EP4CE75F23C8N	128 MB	✓	0 to +70° C
ME-CA1-115-7I-D8	EP4CE115F23I7N	256 MB	✓	-40 to +85° C

Table 1: Standard Module Configurations

The product code indicates the module type and main features. Figure 2 describes the fields within the product code.

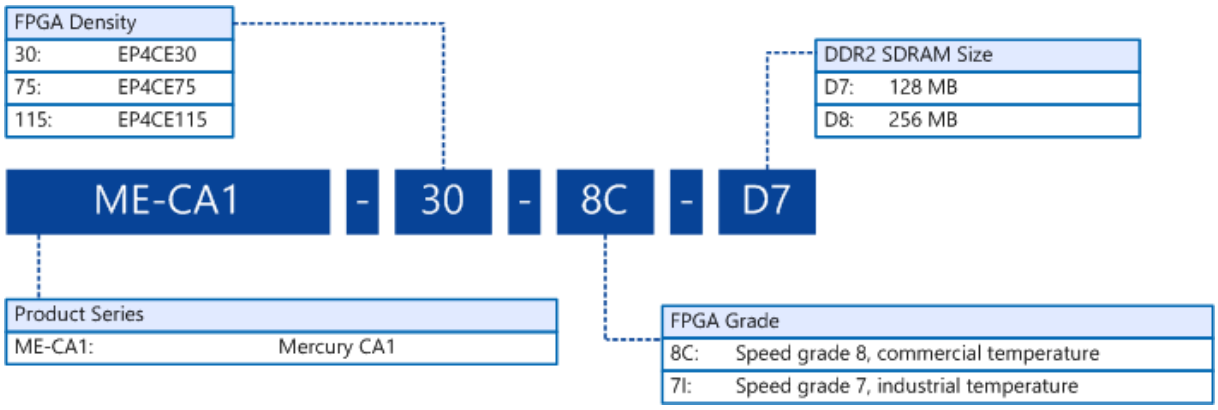

Figure 2: Product Code Fields

Please note that for the first revision modules or early access modules, the product code may not respect entirely this naming convention. Please contact Enclustra for details on this aspect.

2.3 Article Numbers and Article Codes

Every module is uniquely labeled, showing the article number and serial number. An example is presented in Figure 3.

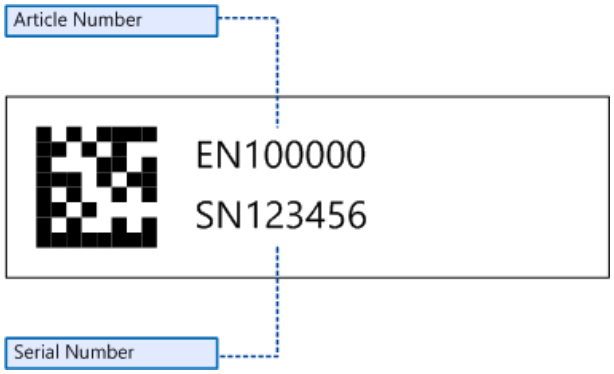

Figure 3: Module Label

The correspondence between article number and article code is shown in Table 2. The article code represents the product code, followed by the revision; the R suffix and number represent the revision number.

The revision changes and product known issues are described in the Mercury CA1 FPGA Module Known Issues and Changes document [6].

Article Number	Article Code
EN100009	ME-CA1-30-8C-D7-R5
EN100010	ME-CA1-75-8C-D7-R5
EN100046	ME-CA1-115-8C-D8-R5
EN100929	ME-CA1-75-8C-D7-R4
EN100930	ME-CA1-30-8C-D7-R4
EN101222	ME-CA1-30-8C-D7-R6
EN101224	ME-CA1-30-8C-D7-X2-R6
EN101225	ME-CA1-75-8C-D7-R6
EN101227	ME-CA1-115-8C-D8-R6
EN101228	ME-CA1-115-7I-D8-R6
EN101229	ME-CA1-115-8C-D8-NEF-X1-R6
EN102569	ME-CA1-30-8C-D7-R6.1
EN102570	ME-CA1-30-8C-D7-X2-R6.1
EN102571	ME-CA1-75-8C-D7-R6.1
EN102572	ME-CA1-115-8C-D8-R6.1
EN102573	ME-CA1-115-7I-D8-R6.1
EN102574	ME-CA1-115-8C-D8-NEF-X1-R6.1

Table 2: Article Numbers and Article Codes

2.4 Top and Bottom Views

2.4.1 Top View

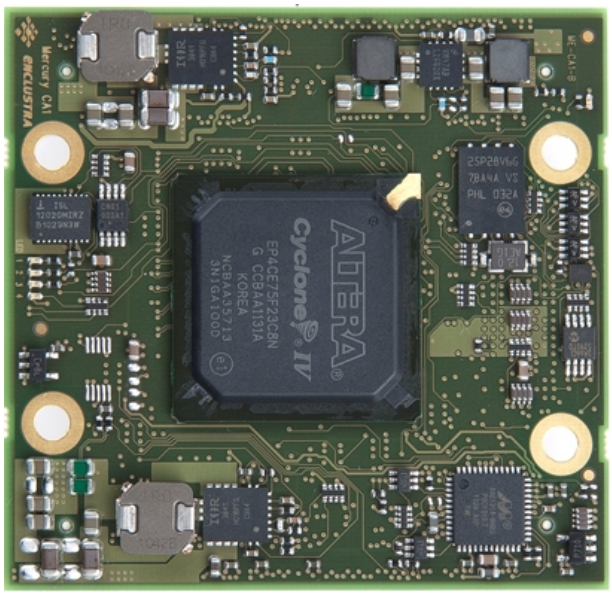

Figure 4: Module Top View

2.4.2 Bottom View

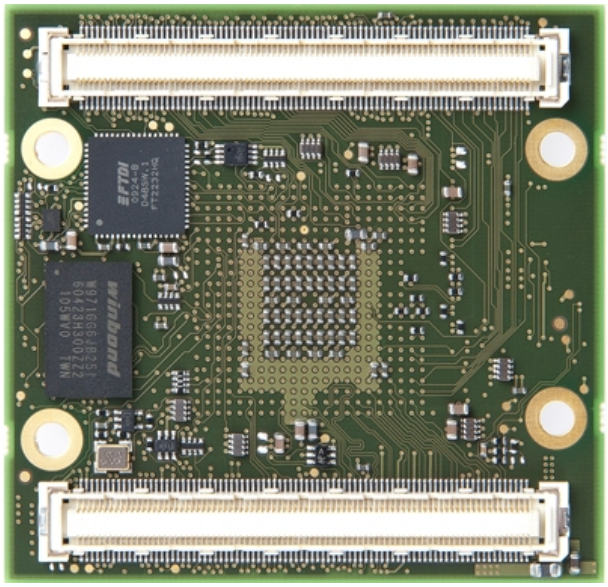

Figure 5: Module Bottom View

Please note that depending on the hardware revision and configuration, the module may look slightly different than shown in this document.

2.5 Top and Bottom Assembly Drawings

2.5.1 Top Assembly Drawing

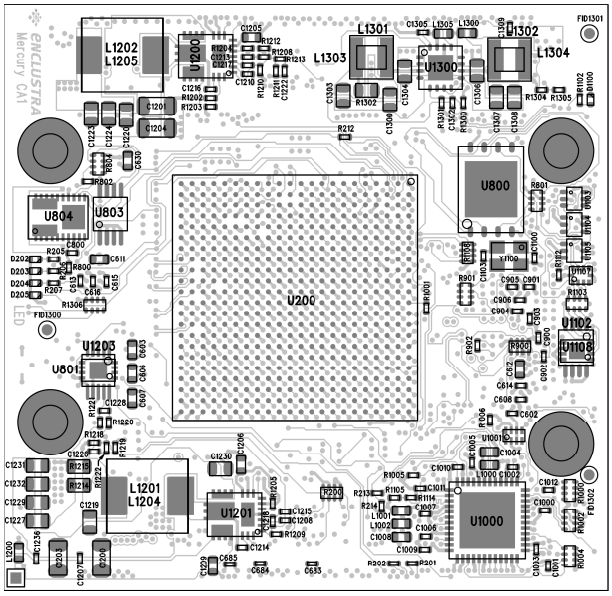

Figure 6: Module Top Assembly Drawing

2.5.2 Bottom Assembly Drawing

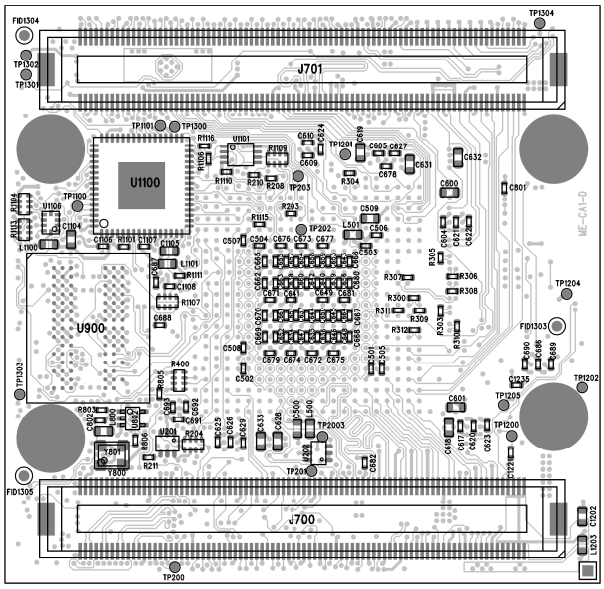

Figure 7: Module Bottom Assembly Drawing

Please note that depending on the hardware revision and configuration, the module may look slightly different than shown in this document.

2.6 Module Footprint

Figure 8 shows the dimensions of the module footprint on the base board.

Enclustra offers Mercury and Mercury+ modules of various geometries having widths of 56, 64, 65, 72 or 74 mm and having different topologies for the mounting holes. If different module types shall be fixed on the base board by screws, additional mounting holes may be required to accommodate different modules. The footprints of the module connectors for the base board design are available for different PCB design tools (Altium, PADS, Eagle, Orcad) [7] and include the required information on the module sizes and holes.

The maximum component height on the base board under the module is dependent on the connector type. Please refer to the Hirose FX10 series product website for detailed connector information [12]. The two connectors are called A (J700) and B (7801).

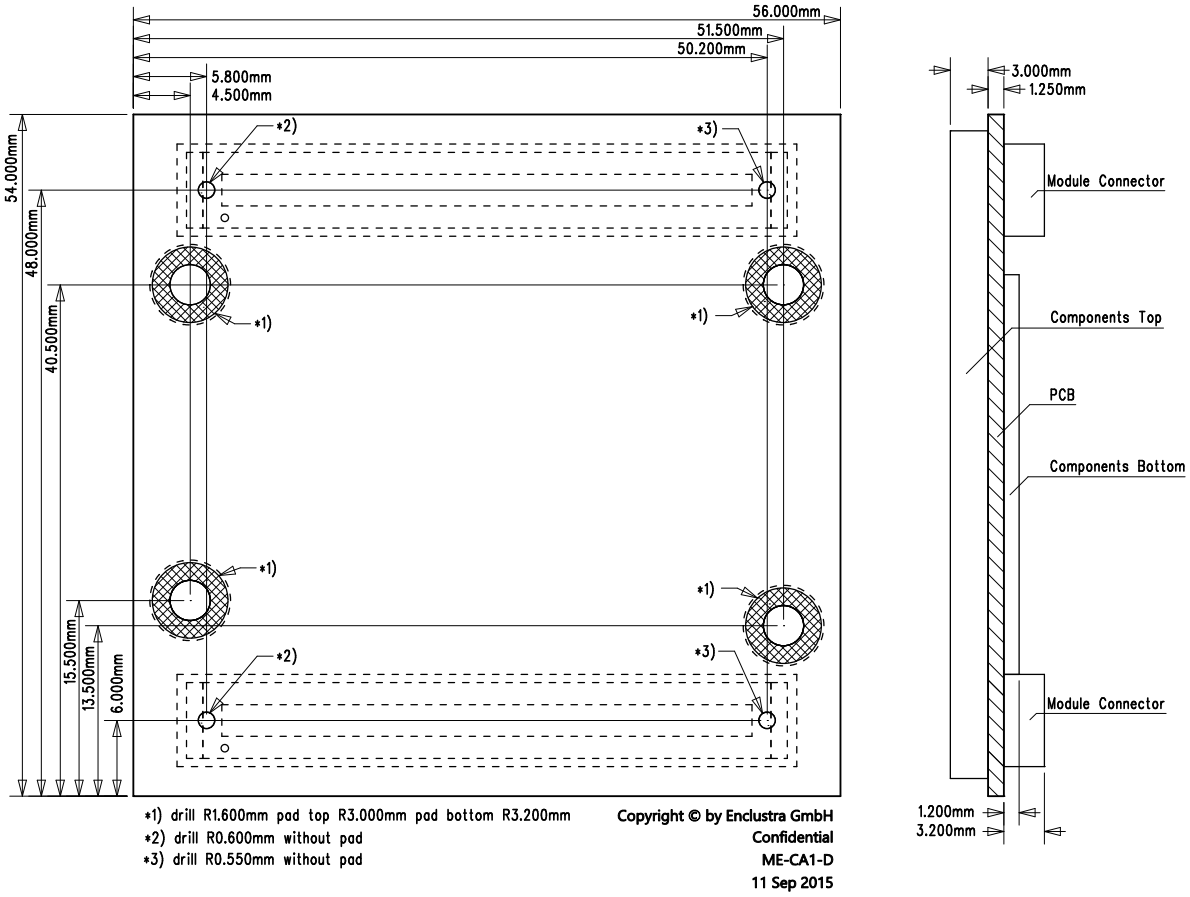

Figure 8: Module Footprint - Top View

Warning!

It is possible to mount the Mercury CA1 FPGA module the wrong way round on the base board - always check that the mounting holes on the base board are aligned with the mounting holes of the Mercury CA1 FPGA module.

2.7 Mechanical Data

Table 3 describes the mechanical characteristics of the Mercury CA1 FPGA module. A 3D model (PDF) and a STEP 3D model are available [8], [9].

Symbol	Value
Size	56 × 54 mm
Component height top	3.0 mm
Component height bottom	1.2 mm
Weight	18 g

Table 3: Mechanical Data

2.8 Module Connector

Two Hirose FX10 168-pin 0.5 mm pitch headers with a total of 336 pins have to be integrated on the base board. Up to four M3 screws may be used to mechanically fasten the module to the base board. Do not use excessive force to tighten the screws, as this could damage the module.

The pinout of the module connector is found in the Mercury Master Pinout Excel Sheet [11]. The connector is available in different packaging options and different stacking heights. Some examples are presented in Table 4. Please refer to the connector datasheet for more information.

Reference	Type	Description
Mercury module connector	FX10A-168S-SV	Hirose FX10, 168-pin, 0.5 mm pitch
Base board connector	FX10A-168P-SV(71)	Hirose FX10, 168-pin, 0.5 mm pitch, 4 mm stacking height
Base board connector	FX10A-168P-SV1(71)	Hirose FX10, 168-pin, 0.5 mm pitch, 5 mm stacking height

Table 4: Module Connector Types

Figure 9 indicates the pin numbering for the Mercury module connectors from the top view of the base board. The connector pins are numbered as follows:

- Connector A: from J700-1 to J700-168
- Connector B: from J701-1 to J701-168

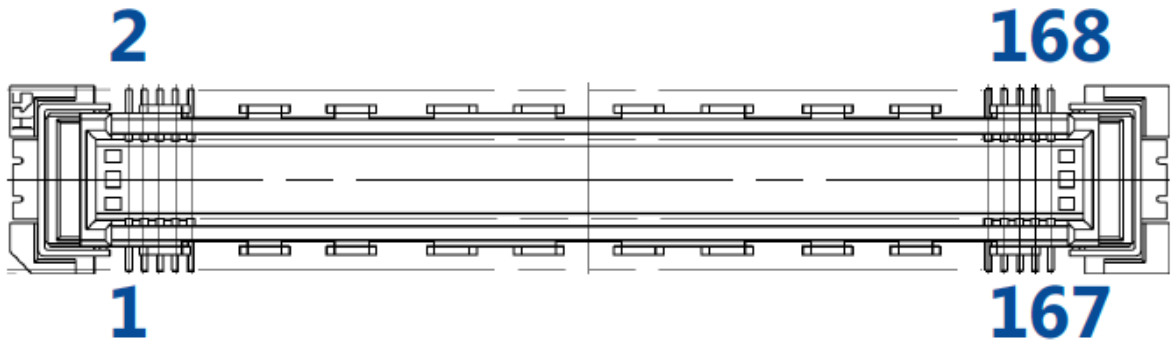

Figure 9: Pin Numbering for the Module Connector

Warning!

Do not use excessive force to latch a Mercury module into the Mercury connectors on the base board, as this could damage the module and the base board; always make sure that the module is correctly oriented before mounting it into the base board.

2.9 User I/O

2.9.1 Pinout

Information on the Mercury CA1 FPGA module pinout can be found in the Enclustra Mercury Master Pinout [11], and in the additional document Enclustra Module Pin Connection Guidelines [10].

Warning!

Please note that the pin types on the schematics symbol of the module connector and in the Master Pinout document are for reference only. On the Mercury CA1 FPGA module it may be possible that the connected pins do not have the targeted functions (such as primary clocks, differential pins, MGT signals, etc).

The available I/O types on the Mercury CA1 FPGA module, possible limitations, and the naming convention for the user I/Os are presented in Table 5.

The clock capable pins are marked with "CLK" in the signal name. For details on their function and usage, please refer to the Intel documentation.

Signal Name	Description	Dir.	Term.	Comment
IN_B<n>_CLK<x>_<PP>_<p>	Differential input clock pair	In	100 Ω	Each differential input clock pair can optionally be used as two single-ended input clocks. For that purpose the 100 Ω termination resistor must be removed.
IN_B<n>_CLK<y>_<PP>	Single-ended input clock	In	-	
IO_B<n>_L<z>_<PP>_<p>	Differential I/O pair	In/Out	-	Each differential I/O pair can optionally be used as two single-ended I/Os.
IO_B<n>_RX_L<z>_<PP>_<p>	Differential input pair	In	100 Ω	Each differential input pair can optionally be used as two single-ended inputs. For that purpose the 100 Ω termination resistor must be removed.
IO_B<n>_<PP>	Single-ended I/O pin	In/Out	-	-
IO_B<n>_S_<PP>	Restricted single-ended I/O pin	In/Out	-	These I/Os can only be used if no differential modes of any FPGA banks are used.
IO_B<n>_<f>_<PP>	Single-ended I/O pin, optional function	In/Out	-	
IO_B<n>_S_VREF_<PP>	Restricted single-ended I/O pin, optional VREF pin	In/Out	-	These I/Os can only be used if no differential modes of any FPGA banks are used.

Table 5: I/O Types Description and Naming Convention

Where:

- <n> represents the FPGA bank number
- <x> represents the differential clock pin number
- <z> represents the differential pin number
- <PP> represents the package pin
- <p> represents the polarity (P = positive, N = negative)
- <f> represents the optional function (e.g. VREF, RUP, RDN)

For example, IO_B4_VREF_AA18 is located on pin AA18 of I/O bank 4 and it can be used as a VREF pin for that specific bank.

Warning!

Using differential signals in single-ended mode may have an effect on other differential signals located in the same FPGA bank. Always check your pinout with Intel Quartus software.

Table 6 includes information related to the available I/O types in each I/O bank and to the number of I/Os.

	Bank 2		Bank 3		Bank 4		Bank 5		Bank 6		
Signal Name	**D**[1]	**SE**[1]	**D**	**SE**	**D**	**SE**	**D**	**SE**	**D**	**SE**	**Total**
IN_B<n>_CLK<x>_<PP>_<p>	1	-	1	-	1	-	-	-	-	-	**3 pairs**
IN_B<n>_CLK<y>_<PP>	-	-	-	-	-	-	-	2	-	2	**4 pins**
IO_B<n>_L<z>_<PP>_<p>	9	-	-	-	-	-	5	-	-	-	**14 pairs**
IO_B<n>_<PP>	-	7	-	18	-	16	-	7	-	26	**74 pins**
IO_B<n>_S_<PP>	-	3	-	2	-	2	-	8	-	-	**15 pins**
IO_B<n>_S_VREF_<PP>	-	1	-	1	-	1	-	2	-	-	**5 pins**
IO_B<n>_<f>_<PP>	-	4	-	3	-	5	-	4	-	4	**20 pins**
IO_B<n>_RX_L<z>_<PP>_<p>	-	-	4	-	4	-	-	-	-	-	**8 pairs**
Total	**10**	**15**	**5**	**24**	**5**	**24**	**5**	**23**	**0**	**32**	

Table 6: I/O Types Availability per I/O Banks

2.9.2 Dual-Purpose Pins

Table 7 lists pins that have special functions during the FPGA configuration or when they are activated in the bitstream. These pins can be configured in Quartus software. Please refer to Intel Cyclone IV Device Handbook [17] and to the Cyclone IV Device Family Pin Connection Guidelines [20] for details on these pins.

Dedicated Function	Signal Name	Description
CRC_ERROR	IO_B6_L21	Active-high signal that indicates that the error-detection circuit has detected errors in the configuration SRAM bits. This pin is optional and is used when the CRC error-detection circuit is enabled. This pin can be configured to support open-drain output.
DEV_CLR#	IO_B5_L3_N21_P	Optional pin that allows you to override all clears on all device registers (device-wide reset). When this pin is driven low, all registers are cleared; when this pin is driven high, all registers behave as programmed.

Continued on next page...

[1] D = differential, SE = single-ended

Dedicated Function	Signal Name	Description
DEV_OE	IO_B5_L3_N22_N	Optional pin that allows you to override all tri-states on the device (device-wide output enable). When this pin is driven low, all I/O pins are tri-stated; when this pin is driven high, all I/O pins behave as defined in the design.
INIT_DONE	IO_B6_L22	This is a dual-purpose pin and can be used as an I/O pin when not enabled as INIT_DONE. When enabled, a transition from low to high at the pin indicates when the device has entered user mode. If the INIT_DONE output is enabled, the INIT_DONE pin cannot be used as a user I/O pin after configuration.

Table 7: Dual-Purpose Pins

2.9.3 Differential I/Os

When using differential pairs, a differential impedance of 100 Ω must be matched on the base board, and the two nets of a differential pair must have the same length.

The information regarding the length of the signal lines from the FPGA device to the module connector is available in Mercury CA1 FPGA Module IO Net Length Excel Sheet [3]. This enables the user to match the total length of the differential pairs on the base board if required by the application.

Warning!

Please note that the trace length of various signals may change between revisions of the Mercury CA1 FPGA module. Please use the information provided in the Mercury CA1 FPGA Module IO Net Length Excel Sheet [3] to check which signals are affected. The differential signals will still be routed differentially in subsequent product revisions.

2.9.4 I/O Banks

Table 8 describes the main attributes of the FPGA I/O banks, and indicates which peripherals are connected to each I/O bank. All I/O pins within a particular I/O bank must use the same I/O (VCC_IO) and reference (VREF) voltages.

Bank	Connectivity	VCC_IO	VREF
Bank 1	Gigabit Ethernet PHY, FTDI USB 2.0 controller, SPI flash, on-board I2C bus, FPGA configuration	3.3 V	Not supported
Bank 2	Module connector	User selectable VCC_IO_B2	IO_B2_S_VREF_M5 IO_B2_VREF_T3 IO_B2_VREF_R5

Continued on next page...

Bank	Connectivity	VCC_IO	VREF
Bank 3	Module connector	User selectable VCC_IO_B3	IO_B3_VREF_Y4 IO_B3_VREF_AB4 IO_B3_VREF_V9 IO_B3_S_VREF_U11
Bank 4	Module connector	User selectable VCC_IO_B4	IO_B4_S_VREF_V12 IO_B4_VREF_W14 IO_B4_VREF_V16
Bank 5	Module connector	User selectable VCC_IO_B5	IO_B5_VREF_W19 IO_B5_VREF_R17 IO_B5_S_VREF_P20 IO_B5_S_VREF_N19
Bank 6	Module connector, LEDs	User selectable VCC_IO_B6	IO_B6_VREF_K19 IO_B6_VREF_J18 IO_B6_VREF_H18 IO_B6_VREF_D20
Bank 7	DDR2 SDRAM	1.8 V	0.9 V
Bank 8	DDR2 SDRAM, Gigabit Ethernet PHY	1.8 V	0.9 V

Table 8: I/O Banks

2.9.5 VREF Usage

I/O standards referenced using VREF can be used on the Mercury module connector. The reference voltage has to be applied to all VREF pins of the respective I/O banks. If a bank is configured to use an I/O standard that does not need a reference voltage, the VREF pins of this bank on the Mercury module connector are available as user I/O pins.

The VREF pins are listed in the Mercury Master Pinout Excel Sheet [11].

Warning!

Use only VREF voltages compliant with the equipped FPGA device; any other voltages may damage the equipped FPGA device, as well as other devices on the Mercury CA1 FPGA module.

Do not leave a VREF pin floating when the used I/O standard requires a reference voltage, as this may damage the equipped FPGA device, as well as other devices on the Mercury CA1 FPGA module.

2.9.6 VCC_IO Usage

The VCC_IO voltages for the I/O banks located on the module connector are configurable by applying the required voltage to the VCC_IO_B[x] pins. All VCC_IO_B[x] pins of the same bank must be connected to the same voltage.

For compatibility with other Enclustra Mercury modules, it is recommended to use a single I/O voltage per module connector.

Signal Name	FPGA Pins	Supported Voltages	Connector A Pins	Connector B Pins
VCC_IO_B2	VCCIO2	1.2 V - 3.3 V ±5%	-	140, 143
VCC_IO_B3	VCCIO3	1.2 V - 3.3 V ±5%	-	88, 95
VCC_IO_B4	VCCIO4	1.2 V - 3.3 V ±5%	-	64, 67
VCC_IO_B5	VCCIO5	1.2 V - 3.3 V ±5%	38, 41	-
VCC_IO_B6[2]	VCCIO6	1.2 V - 3.3 V ±5%	74, 77	-

Table 9: VCC_IO Pins

Warning!

Use only VCC_IO voltages compliant with the equipped FPGA device; any other voltages may damage the equipped FPGA device, as well as other devices on the Mercury CA1 FPGA module.

Do not leave a VCC_IO pin floating, as this may damage the equipped FPGA device, as well as other devices on the Mercury CA1 FPGA module.

Warning!

Do not power the VCC_IO pins when PWR_GOOD and PWR_EN signals are not active. If the module is not powered, you need to make sure that the VCC_IO voltages are disabled (for example, by using a switch on the base board, which uses PWR_GOOD as enable signal). Figure 10 illustrates the VCC_IO power requirements.

[2] VCC_IO_B6 is connected to configuration voltage pins (VIN_CFG) for compatibility with other Enclustra modules. The FPGA configuration signals are at 3.3 V level on the module connector.

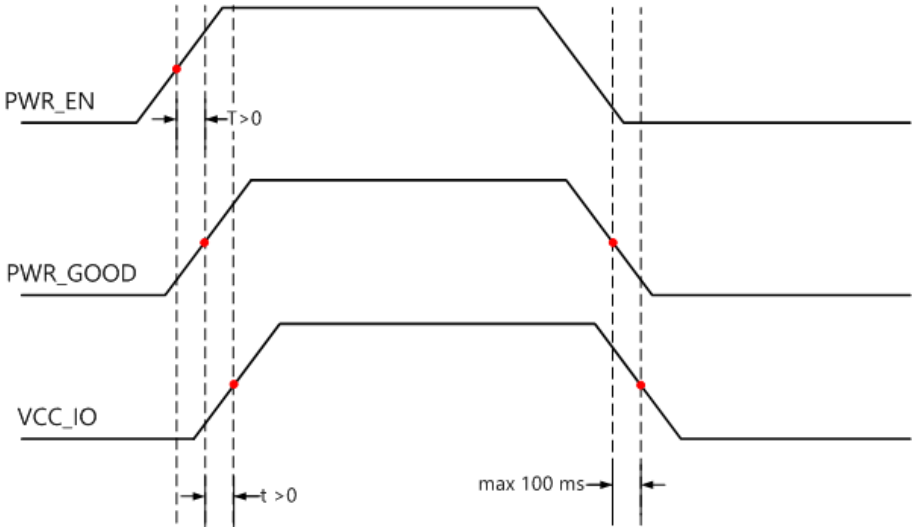

Figure 10: Power-Up Sequence - VCC_IO in Relation with PWR_GOOD and PWR_EN Signals

2.9.7 Signal Terminations

Differential Inputs

All differential inputs (IO_B<n>_RX_L<z>_<PP>_<p>) and differential clock inputs (IO_B<n>_CLK<x>_<PP>_<p>) are equipped with 100 Ω differential termination resistors. These differential inputs may be used as single-ended inputs, if the corresponding 100 Ω parallel resistors are removed from the Mercury CA1 FPGA module.

The resistor identifiers for each differential input pair can be retrieved from the Mercury CA1 FPGA Module User Schematics [5].

Differential I/Os

There are no external differential termination resistors on the Mercury CA1 FPGA module for differential I/Os (IO_B<n>_L<z>_<PP>_<p>). These pairs may be terminated by external termination resistors on the base board (close to the module pins).

Single-Ended Outputs

There are no series termination resistors on the Mercury CA1 FPGA module for single-ended outputs. If required, series termination resistors may be equipped on the base board (close to the module pins).

2.10 Power

2.10.1 Power Generation Overview

The Mercury CA1 FPGA module uses a 5 - 15 V DC power input for generating the on-board supply voltages (1.2 V, 1.8 V, 2.5 V and 3.3 V). Some of these voltages (2.5 V, 3.3 V) are accessible on the module connector.

Table 10 describes the power supplies generated on the module.

Voltage Supply Name	Voltage Value	Rated Current	Voltage Source	Shut down via PWR_EN	Influences PWR_GOOD
VCC_1V2	1.2 V	9 A	VCC_IN	Yes	Yes
VCC_1V8	1.8 V	2 A	VCC_3V3	Yes	Yes
VCC_2V5	2.5 V	2 A	VCC_3V3	Yes	Yes
VCC_3V3	3.3 V	9 A	VCC_IN	No	Yes

Table 10: Generated Power Supplies

Please refer to the Enclustra Module Pin Connection Guidelines for general rules on the power pins [10].

2.10.2 Power Enable/Power Good

The Mercury CA1 FPGA module provides a power enable input on the module connector. This input may be used to shut down the DC/DC converters for 1.2 V, 1.8 V, and 2.5 V, leaving the FPGA, DRR2 SDRAM, Gigabit Ethernet PHY and FTDI device unpowered. The 3.3 V supply is always active.

The PWR_EN input is pulled to VCC_3V3 on the Mercury CA1 FPGA module with a 2.2 kΩ resistor. The PWR_GOOD signal is pulled to VCC_3V3 on the Mercury CA1 FPGA module with a 2.2 kΩ resistor.

PWR_GOOD is an open collector signal and must not be used to drive a load directly. This signal is pulled to GND if the on-board regulators fail or if the module is disabled via PWR_EN. The list of regulators that influence the state of PWR_GOOD signal is provided in Section 2.10.1.

Pin Name	Module Connector Pin	Remarks
PWR_EN	A-10	Floating/3.3 V: Module power enabled Driven low: Module power disabled
PWR_GOOD	A-12	0 V: Module supply not ok 3.3 V: Module supply ok

Table 11: Module Power Status and Control Pins

Warning!

Do not apply any other voltages to the PWR_EN pin than 3.3 V or GND, as this may damage the Mercury CA1 FPGA module. PWR_EN pin can be left unconnected.

Do not power the VCC_IO pins (for example by connecting VCC_3V3 to VCC_IO directly) when PWR_EN is driven low to disable the module. In this case, VCC_IO needs to be switched off in the manner indicated in Figure 10.

2.10.3 Voltage Supply Inputs

Table 12 describes the power supply inputs on the Mercury CA1 FPGA module. The VCC voltages used as supplies for the I/O banks are described in Section 2.9.6.

Pin Name	Module Connector Pins	Voltage	Description
VCC_IN	A-1, 2, 3, 4, 5, 6, 7, 8, 9, 11	5 - 15 V ±5%	Supply for the 1.2 V and 3.3 V voltage regulators. All other supplies are generated from the 3.3 V supply. The input current is rated at 3 A (0.3 A per connector pin).
VCC_BAT	A-168	2.0 - 3.6 V	Battery for the RTC

Table 12: Voltage Supply Inputs

2.10.4 Voltage Supply Outputs

Table 13 presents the supply voltages generated on the Mercury CA1 FPGA module, that are available on the module connector.

Pin Name	Module Connector Pins	Voltage	Maximum Current[3]	Comment
VCC_3V3	A-26, 29, 50, 86 B-55, 79, 115, 127, 152, 155	3.3 V ±5%	3 A (and max 0.3 A per pin)	Always active
VCC_2V5	A-53, 62, 65, 89 B-52, 76, 108, 128	2.5 V ±5%	1.5 A (and max 0.3 A per pin)	Controlled by PWR_EN

Table 13: Voltage Supply Outputs

Warning!

Do not connect any power supply to the voltage supply outputs nor short circuit them to GND, as this may damage the Mercury CA1 FPGA module.

2.10.5 Power Consumption

Please note that the power consumption of any FPGA device strongly depends on the application (on the configured bitstream and I/O activity).

To estimate the power consumption of your design, please use the Intel PowerPlay Early Power Estimators (EPE) and Power Analyzer available on the Intel website.

[3] The maximum available output current depends on your design. See sections 2.10.1 and 2.10.5 for details.

2.10.6 Heat Dissipation

Logic devices like the Intel Cyclone IV FPGA need cooling in most applications; always make sure the FPGA is adequately cooled.

For Mercury modules an Enclustra heat sink kit is available for purchase along with the product. It represents an optimal solution to cool the Mercury CA1 FPGA module - the heat sink body is low profile and usually covers the whole module surface. The kit comes with a gap pad for the FPGA device, a fan and required mounting material to attach the heat sink to the module PCB and baseboard PCB. With additional user configured gap pads, it is possible to cool other components on board as well.

Alternatively, if the Enclustra heat sink does not match the application requirements, a third-party heat sink body (ATS) and an additional gap pad (t-Global) may be used. Please note that the Enclustra heat sink kit already contains all necessary items for cooling the module (heat sink body, gap pad, fan, mounting material).

Table 14 lists the heat sink and thermal pad part numbers that are compatible with the Mercury CA1 FPGA module. Details on the Mercury heatsink kit can be found in the Mercury Heatsink Application Note [15].

Product Name	Package Name	Enclustra Heat Sink	ATS Heat Sink	t-Global Thermal Pad
Mercury CA1	484-pin FBGA [21]	ACC-HS3-Set	ATS-52230G-C1-R0	TG-A6200-25-25-1

Table 14: Heat Sink Type

Please note that the adhesive heat sink part is recommended only for prototyping purposes. In cases where the module is used in environments subject to vibrations, additional mechanical fixation is recommended.

Warning!

Depending on the user application, the Mercury CA1 FPGA module may consume more power than can be dissipated without additional cooling measures; always make sure the FPGA is adequately cooled by installing a heat sink and/or providing air flow.

2.11 Clock Generation

A 50 MHz oscillator is used for the Mercury CA1 FPGA module clock generation. The 50 MHz clock is divided by two and then fed to the FPGA logic and to the Ethernet PHY.

The Ethernet PHY generates a 125 MHz reference clock based on the 25 MHz clock, which is further routed to the FPGA. The 125 MHz is not always available (for example, when the Ethernet PHY is in reset, only a 25 MHz clock is available on the FPGA pins).

Signal Name	Frequency	FPGA Pin	FPGA Pin Type
CLK25	25 MHz	B12	CLK9/DIFFCLK_5P
CLK125	125 MHz	A12	CLK8/DIFFCLK_5N

Table 15: Module Clock Resources

2.12 Reset

The configuration clear signal (CONFIG#) and the FPGA status signal (STATUS#) of the FPGA device are available on the module connector.

Pulling FPGA_CONFIG# low clears the FPGA configuration. Please refer to the Enclustra Module Pin Connection Guidelines [10] for general rules regarding the connection of reset pins.

FPGA_STATUS# can be pulled low to prevent the FPGA configuration. For details on the functions of the CONFIG# and STATUS# signals refer to the Intel documentation.

Table 16 presents the available reset signals. Both signals, FPGA_CONFIG# and FPGA_STATUS#, have on-board 2.2 kΩ pull-up resistors to VCC_3V3.

Signal Name	Connector Pin	FPGA Pin Type	Description
FPGA_CONFIG#	A-132	CONFIG#	Configuration clear signal
FPGA_STATUS#	A-124	STATUS#	FPGA status signal

Table 16: Reset Resources

2.13 LEDs

Three LEDs on the Mercury CA1 FPGA module are connected to the FPGA. Optionally, a fourth LED may be connected to the FPGA; by default, the corresponding signal is connected to a control signal of the FTDI USB 2.0 controller. In order to use the fourth LED, resistor R208 must be assembled while R210 has to be removed.

Signal Name	FPGA Pin	Module Conn. Pin	Remarks
LED0#	B1	B-29	User function/active-low
LED1#	B2	B-33	User function/active-low
LED2#	J2	B-37	User function/active-low
LED3#/FTDI_OE#	J1	B-41	User function/active-low This signal is connected by default to the FTDI device. Hardware changes are required in order to use this pin as a LED signal.

Table 17: LEDs

2.14 DDR2 SDRAM

The DDR2 SDRAM on the Mercury CA1 FPGA module is connected to FPGA I/O banks 7 and 8. In the standard configuration the DDR bus width is 16-bit.

The maximum memory bandwidth on the Mercury CA1 FPGA module is:
333 Mbit/sec × 16 bit = 666 MB/sec

2.14.1 DDR2 SDRAM Type

Table 18 describes the memory availability and configuration on the Mercury CA1 FPGA module.

Module	SDRAM Type	Density	Configuration	Manufacturer
ME-CA1-D7 (commercial)	NT5TU64M16HG-AC	1 Gbit	64 M × 16 bit	Nanya
ME-CA1-D7 (industrial)	NT5TU64M16HG-ACI	1 Gbit	64 M × 16 bit	Nanya
ME-CA1-D8 (commercial)	IM2G16D2DBBG-25	2 Gbit	128 M × 16 bit	I'M Intelligent Memory
ME-CA1-D8 (industrial)	IM2G16D2DBBG-25I	2 Gbit	128 M × 16 bit	I'M Intelligent Memory

Table 18: DDR2 SDRAM Types

Warning!

Other DDR2 memory devices may be equipped in future revisions of the Mercury CA1 FPGA module. Please check the user manual regularly for updates. Any parts with different speed bins or temperature ranges that fulfill the requirements for the module variant may be used.

2.14.2 Signal Description

Please refer to the Mercury CA1 FPGA Module FPGA Pinout Excel Sheet [4] for detailed information on the DDR2 SDRAM connections.

2.14.3 Termination

Warning!

No external termination is implemented for the data signals on the Mercury CA1 FPGA module. Therefore, it is strongly recommended to enable the on-die termination (ODT) feature of the DDR2 SDRAM device.

2.14.4 Parameters

Please refer to the Mercury CA1 FPGA module reference design [2] for DDR2 settings guidelines. The DDR2 SDRAM parameters to be set in Quartus project are presented in Table 19.

The values given in Table 19 are for reference only. Depending on the equipped memory device on the Mercury CA1 FPGA module and on the DDR2 SDRAM frequency, the configuration may be different to the one in the reference design. Please refer to the memory device datasheet for details.

Please note that although the memory device can support data rates of up to 800 Mbit/sec, the DDR2 controller is limited to 166.7 MHz (333 Mbit/sec).

Parameter	Value
SDRAM protocol	DDR2
PHY settings - supply voltage	1.8 V
Memory device speed grade	166.7 MHz
Total Memory interface DQ width	16 bits
Memory CAS latency setting	5 cycles
Column address width	10
Row address width	13-14
Bank address width	3
tRAS	40 ns (1 Gbit devices) / 45 ns (2 Gbit devices)
tRCD	15 ns
tRP	15 ns
tREFI	7.8 us
tRFC	127.5 ns (1 Gbit devices) / 197.5 ns (2 Gbit devices)
tWR	15.0 ns
tWTR	3 cycles
tFAW	50.0 ns
tRRD	10 ns
tRTP	7.5 ns

Table 19: DDR2 SDRAM Parameters

2.15 SPI Flash

The SPI flash can be used to store the FPGA bitstream, Nios II application code and other user data.

2.15.1 SPI Flash Type

Table 20 describes the memory availability and configuration on the Mercury CA1 FPGA module.

Module	Flash Type	Size	Manufacturer
ME-CA1-R1 to R6.0	M25P128-VME6TGB	128 Mbit	Micron
ME-CA1-R6.1	MT25QL128ABA1EW9-0SIT	128 Mbit	Micron

Table 20: SPI Flash Type

The new flash type introduced with revision 6.1 has a smaller sector size (512 Kb) than the older part (2 Mb). This change may require adjustments of the programming algorithm.

Warning!

Other flash memory devices may be equipped in future revisions of the Mercury CA1 FPGA module. Please check the user manual regularly for updates. Any parts with different speeds and temperature ranges that fulfill the requirements for the module variant may be used.

2.15.2 Signal Description

The SPI flash is connected to FPGA bank 1 and to FPGA SPI configuration port. The flash signals are available on the module connector, allowing the user to program the SPI flash from an external master. HOLD#/IO3 and WP#/IO2 flash signals are pulled to VCC_3V3 via 2.2 kΩ resistors.

Please refer to Section 3 for details on programming the flash memory.

Warning!

Special care must be taken when connecting the SPI flash signals on the base board. Long traces or high capacitance may disturb the data communication between the FPGA and the flash device.

2.16 Gigabit Ethernet

A 10/100/1000 Mbit Ethernet PHY is available on the Mercury CA1 FPGA module, connected to the FPGA via RGMII interface. The 25 MHz clock for the PHY is generated on board from the 50 MHz oscillator. A 125 MHz reference clock generated by the PHY is fed back to the FPGA.

2.16.1 Ethernet PHY Type

Table 21 describes the equipped Ethernet PHY device type on the Mercury CA1 FPGA module.

Module	PHY Type	Manufacturer	MDIO Address	Type
ME-CA1 - R1 to R5	88E1318	Marvell	0	10/100/1000 Mbit
ME-CA1 - R6 and newer	KSZ9031RNX	Microchip (Micrel)	3	10/100/1000 Mbit

Table 21: Gigabit Ethernet PHY Type

2.16.2 Signal Description

The RGMII interface is connected to FPGA bank 8 pins. The reset pin for the PHY is connected to FPGA bank 1. It has a pull-down resistor and needs to be driven high to release the PHY from reset.

The MDIO interface is connected to FPGA banks 1 and 8. Table 22 presents the pinout for the Gigabit Ethernet interface.

Signal Name	FPGA Pin	I/O Voltage	Comments
ETH_INT#	A11	1.8 V	
ETH_RST#	G5	3.3 V	Connected via level shifter to the Gigabit Ethernet PHY

Continued on next page...

Signal Name	FPGA Pin	I/O Voltage	Comments
ETH_MDC	H7	3.3 V	Connected via level shifter to the Gigabit Ethernet PHY
ETH_MDIO	D10	1.8 V	
ETH_RX_CLK	B11	1.8 V	
ETH_RX_CTL	B6	1.8 V	
ETH_RX_D0	C3	1.8 V	
ETH_RX_D1	C7	1.8 V	
ETH_RX_D2	E7	1.8 V	
ETH_RX_D3	F9	1.8 V	
ETH_TX_CLK	E5	1.8 V	
ETH_TX_CTL	E6	1.8 V	
ETH_TX_D0	A6	1.8 V	
ETH_TX_D1	D7	1.8 V	
ETH_TX_D2	A10	1.8 V	
ETH_TX_D3	C4	1.8 V	

Table 22: Gigabit Ethernet Signals Description

2.16.3 External Connectivity

The Ethernet signal lines can be connected directly to the magnetics. Please refer to the Enclustra Module Pin Connection Guidelines [10] for details regarding the connection of Ethernet signals.

2.16.4 MDIO Address

For modules from revision 1 to revision 5 equipped with the Marvell Ethernet PHY, the MDIO address assigned to the Gigabit Ethernet PHY is 0.

For modules from revision 6 and newer, the MDIO address is 3.

2.16.5 PHY Configuration

Bootstrap Configuration

For modules revision 6 and newer, the configuration of the Ethernet PHY is bootstrapped when the PHY is released from reset. Make sure all I/Os on the RGMII interface are initialized and all pull-up or pull-down resistors are disabled at that moment.

The bootstrap options of the Ethernet PHY are set as indicated in Table 23.

Pin	Signal Value	Description
MODE[3-0]	1110	RGMII mode: advertise all capabilities (10/100/1000, half/full duplex) except 1000Base-T half duplex.
PHYAD[2-0]	011	MDIO address 3
Clk125_EN	1	125 MHz clock output enabled
LED_MODE	1	Single LED mode
LED1/LED2	1	Active-low LEDs

Table 23: Gigabit Ethernet PHY Configuration

For the Ethernet PHY configuration via the MDIO interface, the MDC clock frequency must not exceed 1 MHz.

RGMII Delays Configuration

The new Ethernet PHY equipped on the Mercury CA1 FPGA module starting with revision 6 requires configuration of the RGMII delays in order to achieve the same timing as the Marvell PHY used in the previous revisions.

The steps required for the PHY configuration are presented in Table 24. Some registers have by default the values listed in the table.

Step	Register	Write Value	Description
1	0xD	0x0002	Select MMD Device Address 2h
2	0xE	0x0004	Select RGMII Control Signal Pad Skew Register
3	0xD	0x4002	Select register data for the selected register
4	0xE	0x0070	Write the value for Control Delay (RX delay = 7, TX delay = 0)
5	0xD	0x0002	
6	0xE	0x0005	Select RGMII RX Data Pad Skew Register
7	0xD	0x4002	
8	0xE	0x7777	Write the value for RX Delay (RX delay = 7 for all lanes)
9	0xD	0x0002	
10	0xE	0x0006	Select RGMII TX Data Pad Skew Register
11	0xD	0x4002	
12	0xE	0x0000	Write the value for TX Delay (TX delay = 0 for all lanes)
13	0xD	0x0002	
14	0xE	0x0008	Select RGMII Clock Pad Skew Register
15	0xD	0x4002	

Continued on next page...

Step	Register	Write Value	Description
16	0xE	0x03FF	Write the value for Clock Delay (RX delay = 31, TX delay = 31)

Table 24: Gigabit Ethernet PHY Configuration - RGMII Delays

Because the new PHY uses MDIO address 3 and the previous version uses MDIO address 0, there are no compatibility issues when using a logic block or a firmware code that configures the new Micrel Ethernet PHY. The configuration procedure can be used with any module revision.

2.17 FTDI USB 2.0 Controller

The Mercury CA1 FPGA module features an FTDI USB 2.0 controller, which allows data transfers to a host computer using speeds of up to 40 MB/s.

The USB controller is connected to the FPGA module using a synchronous FIFO interface configured for 8-bit mode using an interface clock of 60 MHz.

Port A of the FTDI device can be used in synchronous FIFO interface mode or for UART, SPI or I2C transfers between the FPGA and the USB master. Port B of the FTDI is used to access the module I2C bus, to program the SPI Flash or to configure the FPGA in passive serial mode. Please refer to Section 3.9 for details on the module configuration via FTDI.

2.17.1 FTDI Type

Table 25 describes the equipped FTDI controller type on the Mercury CA1 FPGA module.

Type	Manufacturer	Description
FT2232HQ	FTDI	USB 2.0 controller including USB 2.0 PHY

Table 25: USB 2.0 Controller Type

2.17.2 FTDI Synchronous FIFO Interface

Port A of the FTDI device is used for data transfers between the FPGA and the USB master. The interface can be configured in synchronous FIFO interface mode or for UART, SPI or I2C transfers. Please refer to the FTDI device datasheet for details.

Note that for the synchronous FIFO mode an additional D flip-flop is inserted for each of the read and write control signals (FTDI_RD#, FTDI_WR#) in order to meet the setup time of the FTDI device. Please refer to Figure 11 and to the Mercury CA1 FPGA Module User Schematics [5] for details on the FTDI connectivity.

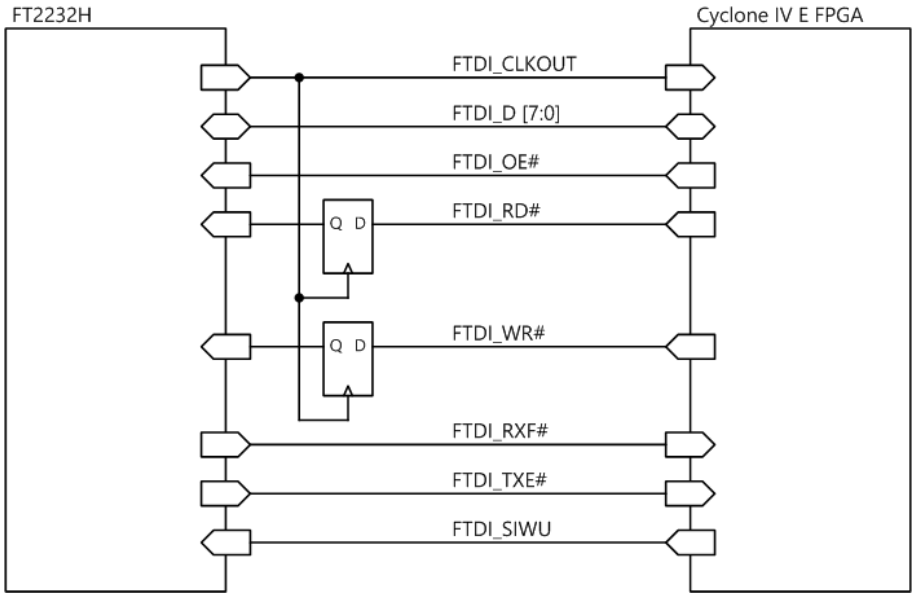

Figure 11: FTDI Device Synchronous FIFO Mode Connectivity

2.18 Real-Time Clock (RTC)

A real-time clock is connected to the I2C bus. The RTC features a battery-buffered 128 bytes user SRAM and a temperature sensor. See Section 4 for details on the I2C bus on the Mercury CA1 FPGA module.

VBAT pin of the RTC is connected to VCC_BAT on the module connector, and can be connected directly to a 3 V battery. Please refer to the Enclustra Module Pin Connection Guidelines [10] for details.

Note that the frequency output mode of the RTC must be disabled when using I2C interrupt system. Otherwise, I2C_INT# is periodically pulled down by the RTC. The disabling of this function can be done by setting bits [3:0] of the RTC register 8 to logic low.

2.18.1 RTC Type

Table 26 describes the equipped RTC device type on the Mercury CA1 FPGA module.

Type	Manufacturer
ISL12020MIRZ	Intersil

Table 26: RTC Type

2.19 Secure EEPROM

The secure EEPROM is used to store the module type and serial number, as well as the Ethernet MAC address and other information. It is connected to the I2C bus.

The secure EEPROM must not be used to store user data.

Please refer to Section 4.4 for details on the content of the EEPROM.

2.19.1 EEPROM Type

Table 27 describes the equipped EEPROM device type on the Mercury CA1 FPGA module.

Module	Type	Manufacturer
ME-CA1 - R1 to R5	DS28CN01	Maxim
ME-CA1 - R6 and newer	ATSHA204A (default)	Atmel
ME-CA1 - R6 and newer	DS28CN01 (assembly option)	Maxim

Table 27: EEPROM Type

2.20 Current and Power Monitor

A current and power monitor may optionally be equipped on the Mercury CA1 FPGA module to monitor the 1.2 V supply. This circuit is connected to the on-board I2C bus. See Section 4 for details on the I2C bus on the Mercury CA1 FPGA module.

The shunt for the current and power monitor is 5 mΩ.

2.20.1 Monitor Type

Table 28 describes the equipped current and power monitor device type on the Mercury CA1 FPGA module.

Type	Manufacturer
INA220	Texas Instruments

Table 28: Current and Power Monitor Type

3 Device Configuration

3.1 Configuration Signals

Table 29 describes the most important configuration pins.

Signal Name	FPGA Pin	FPGA Pin Type	SPI Flash Pin	Mod. Conn. Pin	Comments
FLASH_DCLK	K2	DCLK	C	A-118	2.2 kΩ pull-up to VCC_3V3
FLASH_CS#	E2	DIFFIO_L8P/FLASH_CE#/CSO#	S#	A-116	Depending on the FPGA_MODE
FLASH_DI	D1	DIFFIO_L5N/DATA1/ASDO	D	A-114	2.2 kΩ pull-up to VCC_3V3
FLASH_DO_FPGA_DI	K1	IO/DATA0	Q	A-122	2.2 kΩ pull-up to VCC_3V3
FPGA_STATUS#	K6	STATUS#	-	A-124	2.2 kΩ pull-up to VCC_3V3
FPGA_CONFIG#	K5	CONFIG#	-	A-132	2.2 kΩ pull-up to VCC_3V3 on the FPGA side
FPGA_CONFDONE	M18	CONF_DONE	-	A-130	2.2 kΩ pull-up to VCC_3V3
FPGA_MODE	-	-	-	A-126	10 kΩ pull-up to VCC_3V3

Table 29: FPGA Configuration Pins

Warning!

All configuration signals except for FPGA_MODE must be high impedance as soon as the device is released from reset. Violating this rule may damage the equipped FPGA device, as well as other devices on the Mercury CA1 FPGA module.

FPGA Configuration Pins

The MSEL pins are used to select an FPGA configuration scheme; the pins are described in the Cyclone IV Device Handbook [17].

3.2 Configuration Mode

The FPGA_MODE signal determines whether the FPGA device is configured from the SPI flash or serially via SPI from an external device.

Table 30 describes the available configuration modes and the corresponding configuration mode signals.

FPGA_MODE	FPGA configuration	MSEL[3:0]
0	Active serial configuration	0010
1	Passive serial configuration	0000

Table 30: Configuration Modes

3.3 JTAG

The JTAG interface can be used for configuring and debugging the FPGA logic. The JTAG signals on the FPGA are directly connected to the module connector.

The FPGA device and the SPI flash can be configured via JTAG using Intel tools.

3.3.1 JTAG on Module Connector

Signal Name	Module Connector Pin	Resistor
JTAG_TCK	A-123	1.1 kΩ pull-down
JTAG_TMS	A-119	2.2 kΩ pull-up to VCC_2V5
JTAG_TDI	A-117	2.2 kΩ pull-up to VCC_2V5
JTAG_TDO	A-121	-

Table 31: JTAG Interface

3.3.2 External Connectivity

JTAG signals can be connected directly on the base board to a JTAG connector. No pull-up/pull-down resistors are necessary. The VCC pin of the programmer must be connected to VCC_2V5.

It is recommended to add 22 Ω series termination resistors between the module and the JTAG header, close to the source. Please refer to the Enclustra Module Pin Connection Guidelines for details on JTAG interface.

3.4 Passive Serial Configuration

In the passive serial configuration mode, the bitstream must be transmitted from an external device to the FPGA. The configuration pins of the FPGA are connected directly to the module connector, allowing the configuration of the FPGA from a microcontroller or another SPI capable device. For more information on the configuration modes, please refer to the Cyclone IV datasheet [16].

3.4.1 Signal Description

Signal Name	Description
FLASH_DCLK	Configuration clock
FLASH_DO_FPGA_DI	Configuration data
FPGA_STATUS#	Is pulled low by the FPGA if any CRC error occurs during the configuration; it may be used as an input to delay the start of the FPGA configuration.
FPGA_CONFDONE	Goes high after a successful FPGA configuration
FPGA_CONFIG#	When pulled low, the FPGA configuration sequence is cleared and all pins are tri-stated. The rising edge of FPGA_CONFIG# initializes the configuration.
FPGA_MODE	Must be pulled high or left open during configuration

Table 32: Passive Serial Configuration - Signals Description

Warning!

Note that after the rising edge of FPGA_CONFDONE, the FPGA still requires two falling edges of FPGA_DCLK clock to finish the configuration. Therefore, if the FPGA_DCLK and FLASH_DO_FPGA_DI pins are used in the FPGA design, the user must ensure that these are tri-stated by the FPGA logic for the appropriate amount of time. Details on the configuration time are available in the Altera Configuration and Remote System Upgrades in Cyclone IV Devices document [18].

FPGA_DCLK signal remains in input mode after the configuration has finished. If the SPI Flash shall be accessed after passive serial configuration, another I/O pin must be connected to the FPGA_DCLK signal on the base board.

3.5 Active Serial Configuration

In the active serial configuration mode, the FPGA reads the bitstream from the SPI flash. The bitstream must be located at address 0x0. For more information, please refer to the Cyclone IV datasheet [16].

3.5.1 Signal Description

Signal Name	Description
FPGA_DCLK	Must be high impedance during configuration and operation
FLASH_DO_FPGA_DI	Must be high impedance during configuration and operation
FPGA_STATUS#	Is pulled low by the FPGA if any CRC error occurs during the configuration; it may be used as an input to delay the start of the FPGA configuration.
FPGA_CONFDONE	Goes high after a successful FPGA configuration
FPGA_CONFIG#	When pulled low, the FPGA configuration sequence is cleared and all pins are tri-stated. The rising edge of FPGA_CONFIG# initializes the configuration.
FPGA_MODE	Must be pulled low during and after configuration via a 470 Ω - 680 Ω resistor.
FLASH_DI	Must be high impedance during configuration and operation
FLASH_CS#	Must be high impedance during configuration and operation

Table 33: Active Serial Configuration - Signals Description

3.6 SPI Flash Programming via JTAG

The SPI flash device on the Mercury CA1 FPGA module can be programmed via JTAG using different methods:

- By using Nios II Flash Programmer
  - This option can be used when a Nios II processor is instantiated in the FPGA design
  - It requires the FPGA to be already programmed with an .sof file corresponding to an FPGA design that includes a Nios II processor
- By using Quartus II Programmer
  - This option can be used when a Serial Flash Loader IP core is instantiated in the FPGA design
  - The .sof file must be converted to a JTAG Indirect Configuration File (.jic)
  - The FPGA bitstream .sof file and the configuration data for the SPI flash are programmed using Quartus II Programmer

3.7 SPI Flash In-System-Programming using Quartus-II Programmer

In-System Programming feature is used for programming the flash-memory-based devices through the active serial programming interface using the USB-Blaster or ByteBlaster II download cables.

In order to perform in-system programming with the Quartus-II Programmer the configuration signals have to be connected as shown in Table 34. Further, a jumper or DIP switch must be equipped on FPGA_MODE signal. FPGA_MODE must be pulled to GND to allow the FPGA to load the bitstream from the SPI flash, but for the flash programming FPGA_MODE must be high.

Details on in-system programming are presented in the Cyclone IV Device Handbook, Chapter 8 [17].

Pin Number	Pin Name	Connection
1	DCLK	FPGA_DCLK
2	GND	GND
3	CONF_DONE	FPGA_CONFDONE
4	VCC	VCC_3V3
5	CONFIG#	FPGA_CONFIG#
6	CE#	-
7	DATAOUT	FLASH_DO_FPGA_DI
8	CS#	FLASH_CS#
9	ASDI	FLASH_DI
10	GND	GND

Table 34: Altera ByteBlaster II or USB Blaster Connector Pinout for In-System Flash Programming

3.8 SPI Flash Programming from an External SPI Master

The signals of the SPI flash are directly connected to the module connector for flash access. As the flash signals are connected to the FPGA device as well, the FPGA device pins must be tri-stated while accessing the SPI flash directly from an external device.

This is ensured by pulling the FPGA_CONFIG# to GND, which puts the FPGA device into reset state and tri-states all I/O pins during flash programming.

Figure 12 shows the signal diagrams corresponding to flash programming from an external master.

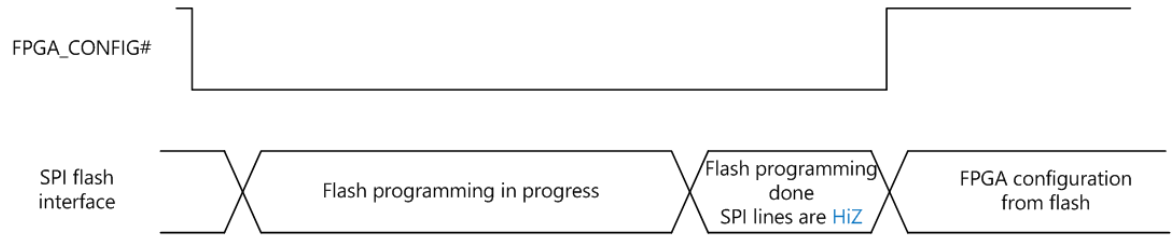

Figure 12: SPI Flash Programming from an External SPI Master - Signal Diagrams

Warning!

Accessing the SPI flash directly without putting the FPGA device into reset may damage the equipped FPGA device, as well as other devices on the Mercury CA1 FPGA module.

3.8.1 Signal Description

Signal Name	SPI Flash Pin	Description
FLASH_DCLK	SCK	SPI CLK
FLASH_DO_FPGA_DI	SO/IO1	SPI MISO
FPGA_CONFIG#	-	Must be pulled low during SPI flash programming. When released, all other pins of the SPI interface must be high impedance.
FLASH_DI	SI/IO0	SPI MOSI
FLASH_CS#	CS#	SPI CS#

Table 35: Flash Programming from an External Master - Signals Description

3.9 Module Configuration via FTDI USB 2.0 Controller

The FPGA configuration interface and SPI flash signals are connected to the FTDI USB 2.0 device controller. This allows FPGA serial configuration and SPI flash programming over USB from a host computer without additional hardware.

Port A of the FTDI device can be used in synchronous FIFO interface mode or for UART, SPI or I2C transfers between the FPGA and the USB master.

Port B of the FTDI is used to access the module I2C bus, to program the SPI Flash or to configure the FPGA in passive serial mode. General purpose I/O pins of port B are used to control the configuration multiplexers; refer to Table 36 for details.

3.9.1 FTDI Port B Configuration

CONFIG_I2C_EN# (BCBUS6)	CONFIG_EN# (BCBUS5)	FPGA_MODE (BCBUS4)	FPGA_CONFIG# (BCBUS3)	Configuration
1	0	0	0	SPI flash programming via FTDI
0	X	X	X	FTDI device pins connected to module I2C bus
1	0	1	HiZ (1)	Passive serial configuration via FTDI
X	1	0	HiZ (1)	Active serial configuration (FPGA is configured from SPI flash)

Table 36: FTDI Configuration Settings - Port B

The control signals CONFIG_I2C_EN# and CONFIG_EN# are used to configure the way BDBUS0-3 pins are routed on the module: to I2C, SPI flash or FPGA SPI configuration port.

Please note that for the SPI flash programming, FPGA_CONFIG# must be pulled to ground. For the passive serial configuration FPGA_MODE must be pulled high or left open, while for active serial configuration FPGA_MODE must be pulled low.

Warning!

After FPGA passive serial configuration or SPI flash programming operations, the CONFIG_EN# signal must be pulled high, to avoid damaging the equipped FPGA device.

Warning!

Do not connect FPGA_MODE directly to GND on the base board, as this will not allow FPGA passive serial configuration. Use a 470 Ω - 680 Ω resistor to pull this signal to GND.

3.9.2 FPGA Passive Serial Configuration via FTDI

Table 37 lists the FTDI signals for passive serial configuration.

FTDI Port	Connection	Dir.	Static Value	Description
BDBUS0	CONFIG_CLK	Out	-	FPGA configuration clock
BDBUS1	CONFIG_DO	Out	-	FPGA configuration data
BCBUS1	FPGA_CONFDONE	In	-	FPGA configuration done signal
BCBUS2	FPGA_STATUS#	In	-	FPGA delay configuration signal, pulled low by the FPGA if errors occur during the configuration
BCBUS3	FPGA_CONFIG#	Out	-	FPGA configuration clear signal
BCBUS4	FPGA_MODE	Out	1	FPGA configuration mode select
BCBUS5	CONFIG_EN#	Out	0	Configuration multiplexer control signal
BCBUS6	CONFIG_I2C_EN#	Out	1	Configuration multiplexer control signal

Table 37: FPGA Passive Serial Configuration via FTDI

3.9.3 SPI Flash Programming via FTDI

Table 38 lists the FTDI signals for SPI flash programming.

FTDI Port	Connection	Dir.	Static Value	Description
BDBUS0	CONFIG_CLK	Out	-	SPI flash configuration clock
BDBUS1	CONFIG_DO	Out	-	SPI flash write data
BDBUS2	CONFIG_DI	In	-	SPI flash read data
BDBUS3	CONFIG_CS#	Out	-	SPI flash chip select
BCBUS3	FPGA_CONFIG#	Out	0	FPGA configuration clear signal
BCBUS4	FPGA_MODE	Out	0	FPGA configuration mode select
BCBUS5	CONFIG_EN#	Out	0	Configuration multiplexer control signal
BCBUS6	CONFIG_I2C_EN#	Out	0	Configuration multiplexer control signal

Table 38: SPI Flash Programming via FTDI

Warning!

Accessing the SPI flash directly without putting the FPGA device into reset may damage the equipped FPGA device, as well as other devices on the Mercury CA1 FPGA module.

3.10 Enclustra Module Configuration Tool

The SPI flash on the Mercury CA1 FPGA module can be programmed via FTDI using the Enclustra Module Configuration Tool (MCT) [14]. Passive serial configuration is also supported by the Enclustra MCT software.

4 I2C Communication

4.1 Overview

The I2C bus on the Mercury CA1 FPGA module is connected to the FPGA device, EEPROM, RTC and current and power monitor, and is available on the module connector. This allows external devices to read the module type and to connect more devices to the I2C bus.

Please note that the RTC must be configured correctly to use I2C interrupts - for details, refer to Section 2.18.

The I2C clock frequency should not exceed 400 kHz.

Warning!

Maximum I2C speed may be limited by the routing path and additional loads on the base board.

Warning!

If the I2C traces on the base board are very long, 100 Ω series resistors should be added between module and I2C device on the base board.

4.2 Signal Description

Table 39 describes the signals of the I2C interface. All signals have on-board pull-up resistors to VCC_3V3.

All signals must be connected to open collector outputs and must not be driven high from any source. I2C_INT# is an input to the FPGA and must not be driven from the FPGA device.

Signal Name	FPGA Package Pin	FTDI Pin	Connector Pin	Resistor
I2C_SDA	C2	BDBUS1/BDBUS2	A-113	2.2 kΩ pull-up
I2C_SCL	C1	BDBUS0	A-111	2.2 kΩ pull-up
I2C_INT#	J3	-	A-115	2.2 kΩ pull-up

Table 39: I2C Signal Description

4.3 I2C Address Map

Table 40 describes the addresses for several devices connected on I2C bus.

Address (7-bit)	Description
0x64	Secure EEPROM
0x50	Secure EEPROM (assembly option, refer to Section 2.19)
0x57	RTC user SRAM
0x6F	RTC registers
0x40	Current and power monitor (optional)

Table 40: I2C Addresses

4.4 Secure EEPROM

The secure EEPROM is used to store the module serial number and configuration. In the future, the EEPROM will be used for copy protection and licensing features. Please contact us for further information.

Warning!
The secure EEPROM is for Enclustra use only. Any attempt to write data to the secure EEPROM causes the warranty to be rendered void.

4.4.1 Memory Map

Address	Length (bits)	Description
0x00	32	Module serial number
0x04	32	Module product information
0x08	32	Module configuration
0x0C	32	Reserved
0x10	48	Ethernet MAC address
0x16	48	Reserved
0x1C	32	Checksum (only for DS28CN01 EEPROM type)

Table 41: EEPROM Sector 0 Memory Map

Module Serial Number

The module serial number is a unique 32-bit number that identifies the module. It is stored using big-endian byte order (MSB on the lowest address).

Module Product Information

This field indicates the type of module and hardware revision.

Module	Product Family	Reserved	Revision	Product Information
Mercury CA1 FPGA module	0x0322	0x[XX]	0x[YY]	0x0322 [XX][YY]

Table 42: Product Information

Module Configuration

Addr.	Bits	Comment	Min. Value	Max. Value	Comment
0x08	7-4	FPGA Type	0	4	See FPGA type table (Table 44)
	3-0	FPGA device speed grade	6	8	
0x09	7	Temperature range	0 (Commercial)	1 (Industrial)	
	6	Power grade	0 (Normal)	1 (Low Power)	
	5-4	Ethernet port count	0	1	
	3	Ethernet speed	0 (Fast Ethernet)	1 (Gigabit Ethernet)	
	2	RTC equipped	0	1	
	1-0	Reserved	-	-	
0x0A	7-2	Reserved	-	-	
	1-0	USB 2.0 device port count	0	1	
0x0B	7-4	DDR2 RAM size (MB)	0 (0 MB)	6 (256 MB)	Resolution = 8 MB
	3-0	SPI flash memory size (MB)	0 (0 MB)	5 (16 MB)	Resolution = 1 MB

Table 43: Module Configuration

The memory sizes are defined as Resolution$\times 2^{(Value-1)}$ (e.g. DRAM=0: not equipped, DRAM=1: 8 MB, DRAM=2: 16 MB, DRAM=3: 32 MB, etc).

Table 44 shows the available FPGA types.

Value	FPGA Device Type
0	EP4CE30
1	EP4CE40
2	EP4CE55
3	EP4CE75
4	EP4CE115

Table 44: FPGA Device Types

Ethernet MAC Address

The Ethernet MAC address is stored using big-endian byte order (MSB on the lowest address). Each module is assigned two sequential MAC addresses; only the lower one is stored in the EEPROM.

5 Operating Conditions

5.1 Absolute Maximum Ratings

Table 45 indicates the absolute maximum ratings for Mercury CA1 FPGA module. The values given are for reference only; for details please refer to the Cyclone IV Datasheet [16].

Symbol	Description	Rating	Unit
VCC_IN	Supply voltage relative to GND	-0.5 to 16	V
VCC_BAT	Supply voltage for the RTC	-0.3 to 3.6	V
VCC_IO_[x]	Output drivers supply voltage relative to GND	-0.5 to 3.75	V
V_IO	I/O input voltage relative to GND	-0.5 to 4.2	V
Temperature	Temperature range for commercial modules (C)*	0 to +70	°C
	Temperature range for industrial modules (I)*	-40 to +85	°C

Table 45: Absolute Maximum Ratings

5.2 Recommended Operating Conditions

Table 46 indicates the recommended operating conditions for Mercury CA1 FPGA module. The values given are for reference only; for details please refer to the Cyclone IV Datasheet [16].

Symbol	Description	Rating	Unit
VCC_IN	Supply voltage relative to GND	4.75 to 15.75	V
VCC_BAT	Supply voltage for the RTC	2.0 to 3.45	V
VCC_IO_[x]	Output drivers supply voltage relative to GND	Refer to Section 2.9.6	V
V_IO	I/O input voltage relative to GND	-0.5 to 3.6	V
Temperature	Temperature range for commercial modules (C)*	0 to +70	°C
	Temperature range for industrial modules (I)*	-40 to +85	°C

Table 46: Recommended Operating Conditions

Warning!

** The components used on the hardware are specified for the relevant temperature range. The user must provide adequate cooling in order to keep the temperature of the components within the specified range.*

6 Ordering and Support

6.1 Ordering

Please use the Enclustra online request/order form for ordering or requesting information:
`http://www.enclustra.com/en/order/`

6.2 Support

Please follow the instructions on the Enclustra online support site:
`http://www.enclustra.com/en/support/`

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