

Monolithic High Voltage Isolated Flyback Converter

FEATURES

- 4.5V to 100V Input Voltage Range
- Internal 420mA, 150V Power Switch
- Boundary Mode Operation
- No Transformer Third Winding or Opto-Isolator Required for Regulation
- Improved Primary-Side Winding Feedback Load Regulation
- V_{OUT} Set with Two External Resistors
- BIAS Pin for Internal Bias Supply and Power Switch Driver
- No External Start-Up Resistor
- 16-Lead MSOP Package

APPLICATIONS

- Isolated Telecom Power Supplies
- Isolated Auxiliary/Housekeeping Power Supplies
- Isolated Industrial, Automotive and Medical Power Supplies

DESCRIPTION

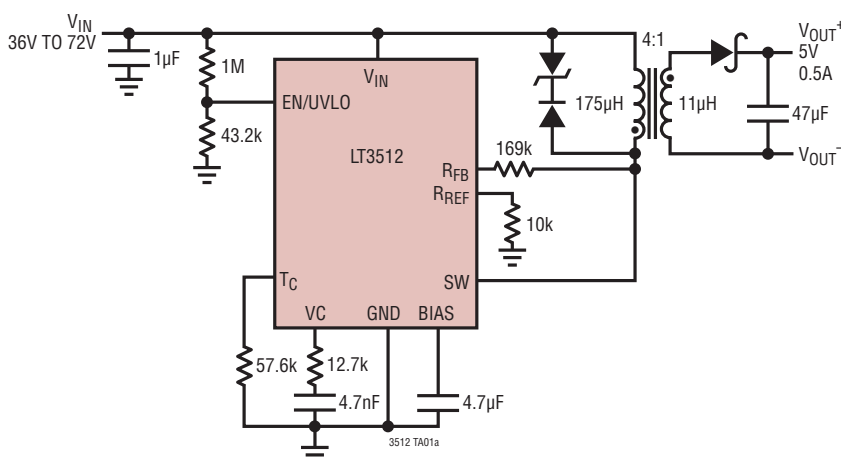
The LT3512 is a high voltage monolithic switching regulator specifically designed for the isolated flyback topology. No third winding or opto-isolator is required for regulation as the part senses output voltage directly from the primary-side flyback waveform. The device integrates a 420mA, 150V power switch, high voltage circuitry, and control into a high voltage 16-lead MSOP package with four leads removed.

The LT3512 operates from an input voltage range of 4.5V to 100V and delivers up to 4.5W of isolated output power. Two external resistors and the transformer turns ratio easily set the output voltage. Off-the-shelf transformers are available for several applications. The high level of integration and the use of boundary mode operation results in a simple, clean, tightly regulated application solution to the traditionally tough problem of isolated power delivery.

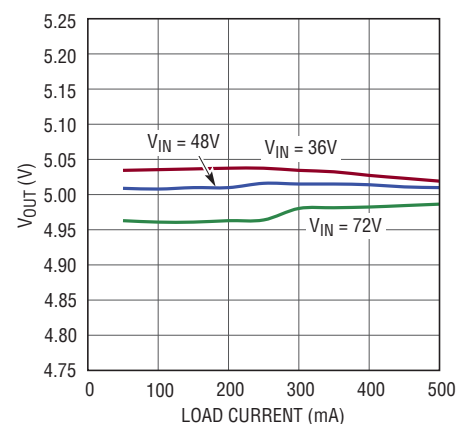
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TYPICAL APPLICATION

48V to 5V Isolated Flyback Converter



Output Load and Line Regulation



3512 TA01b

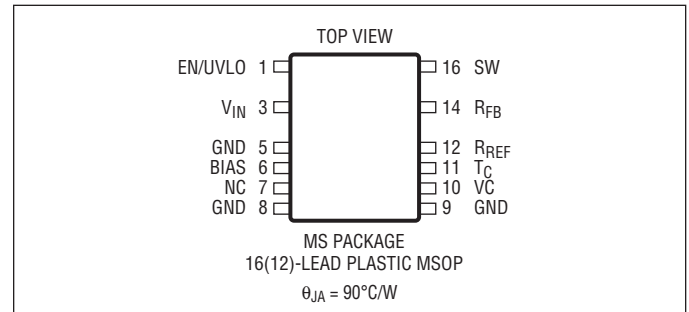
LT3512

ABSOLUTE MAXIMUM RATINGS

(Note 1)

SW (Note 4)	150V
V_{IN} , EN/UVLO, R_{FB}	100V
V_{IN} to R_{FB}	$\pm 6V$
BIAS	Lesser of 20V or V_{IN}
R_{REF} , T_C , VC	6V
Operating Junction Temperature Range (Note 2)	
LT3512E, LT3512I	-40°C to 125°C
LT3512H	-40°C to 150°C
LT3512MP	-55°C to 150°C
Storage Temperature Range	-65°C to 150°C

PIN CONFIGURATION



ORDER INFORMATION

LEAD FREE FINISH	TAPE AND REEL	PART MARKING*	PACKAGE DESCRIPTION	TEMPERATURE RANGE
LT3512EMS#PBF	LT3512EMS#TRPBF	3512	16-Lead Plastic MSOP	-40°C to 125°C
LT3512IMS#PBF	LT3512IMS#TRPBF	3512	16-Lead Plastic MSOP	-40°C to 125°C
LT3512HMS#PBF	LT3512HMS#TRPBF	3512	16-Lead Plastic MSOP	-40°C to 150°C
LT3512MPMS#PBF	LT3512MPMS#TRPBF	3512	16-Lead Plastic MSOP	-55°C to 150°C

Consult LTC Marketing for parts specified with wider operating temperature ranges. *The temperature grade is identified by a label on the shipping container.

For more information on lead free part marking, go to: <http://www.linear.com/leadfree/>

For more information on tape and reel specifications, go to: <http://www.linear.com/tapeandreeel/>

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at $T_A = 25^\circ\text{C}$. $V_{IN} = 24V$ unless otherwise noted.

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Input Voltage Range	$V_{IN} = \text{BIAS}$	● 6		100	V
		4.5		15	V
Quiescent Current	Not Switching $V_{EN/UVLO} = 0.2V$		3.5	4.5	mA
			0		μA
EN/UVLO Pin Threshold	EN/UVLO Pin Voltage Rising	● 1.15	1.21	1.27	V
EN/UVLO Pin Current	$V_{EN/UVLO} = 1.1V$ $V_{EN/UVLO} = 1.4V$		2.0	2.6	μA
				0	3.3
Maximum Switching Frequency			650		kHz
Minimum Switching Frequency			40		kHz
Maximum Current Limit		420	600	800	mA
Minimum Current Limit		80	120	150	mA
Switch V_{CESAT}	$I_{SW} = 200\text{mA}$		0.5		V
R_{REF} Voltage		● 1.18	1.20	1.215	V
		1.17		1.23	V
R_{REF} Voltage Line Regulation	$6V < V_{IN} < 100V$		0.01	0.03	%/V
R_{REF} Pin Bias Current	(Note 3)	●	80	400	nA
Error Amplifier Voltage Gain			150		V/V
Error Amplifier Transconductance	$\Delta I = 2\mu\text{A}$		140		μmhos

3512fb

ELECTRICAL CHARACTERISTICS The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at $T_A = 25^\circ\text{C}$. $V_{IN} = 24\text{V}$ unless otherwise noted.

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
T_C Current into R_{REF}	$R_{TC} = 53.6\text{k}$		9.5		μA
BIAS Pin Voltage	Internally Regulated	3	3.1	3.2	V

Note 1: Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. Exposure to any Absolute Maximum Rating condition for extended periods may affect device reliability and lifetime.

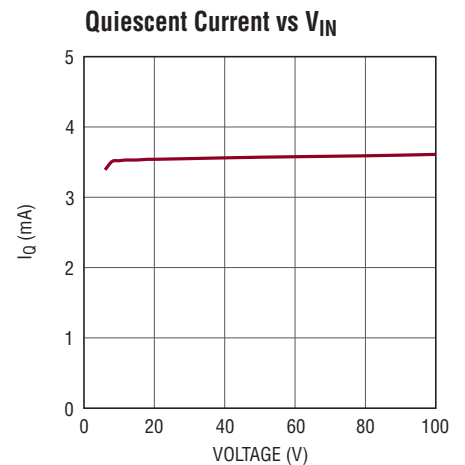
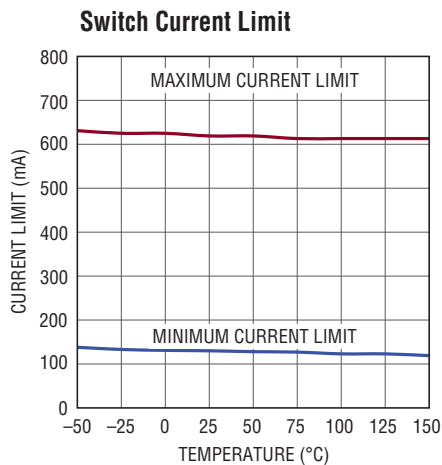
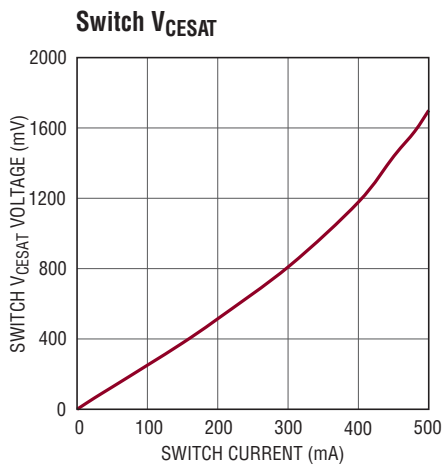
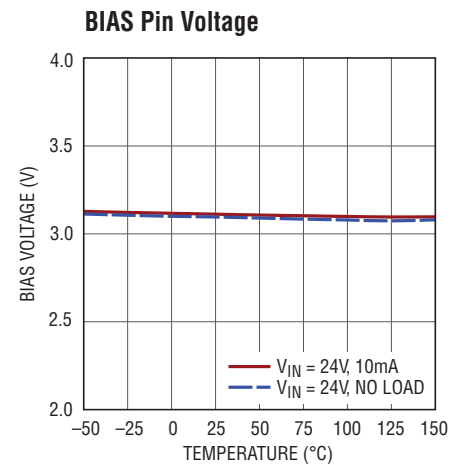
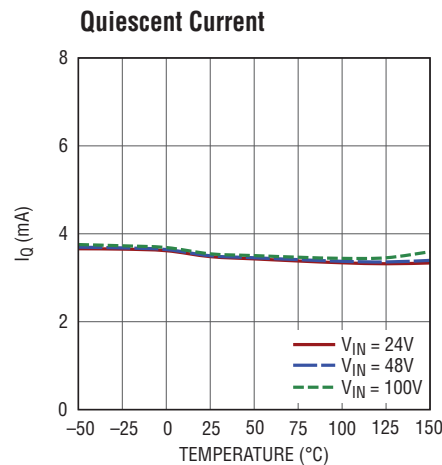
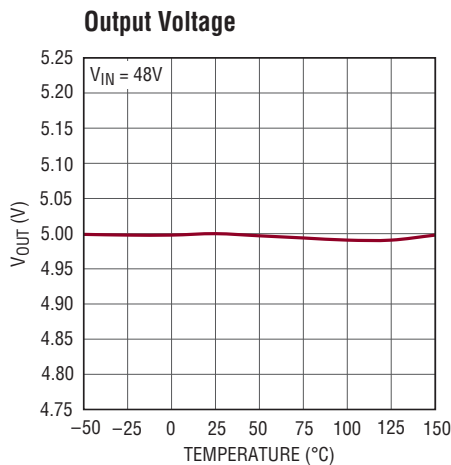
Note 2: The LT3512E is guaranteed to meet performance specifications from 0°C to 125°C junction temperature. Specifications over the -40°C to 125°C operating junction temperature range are assured by design, characterization and correlation with statistical process controls. The LT3512I is guaranteed to meet performance specifications from -40°C to 125°C operating junction temperature range. The LT3512H is guaranteed

to meet performance specifications from -40°C to 150°C operating junction temperature range. The LT3511MP is guaranteed over the full -55°C to 150°C operating junction range. High junction temperatures degrade operating lifetimes. Operating lifetime is derated at junction temperatures greater than 125°C .

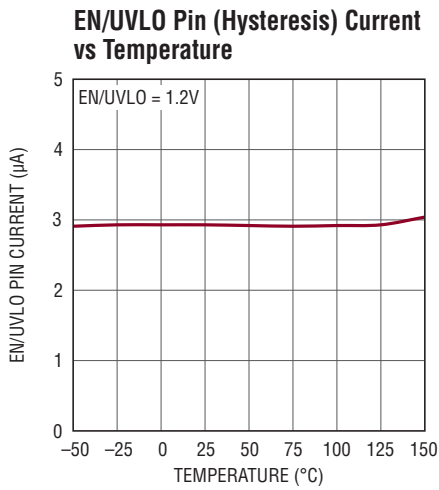
Note 3: Current flows out of the R_{REF} pin.

Note 4: The SW pin is rated to 150V for transients. Operating waveforms of the SW pin should keep the pedestal of the flyback waveform below 100V as shown in Figure 5.

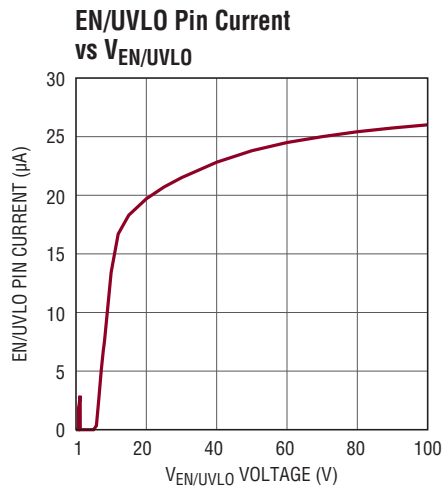
TYPICAL PERFORMANCE CHARACTERISTICS $T_A = 25^\circ\text{C}$, unless otherwise noted.



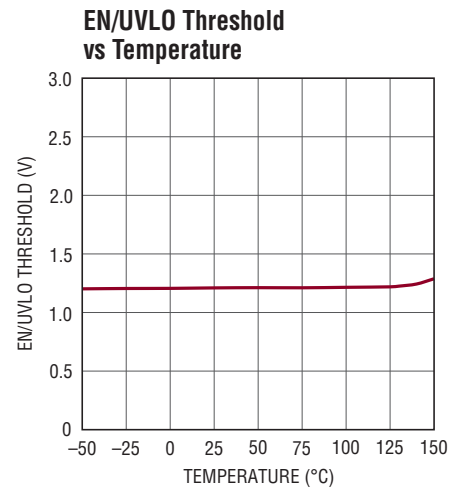
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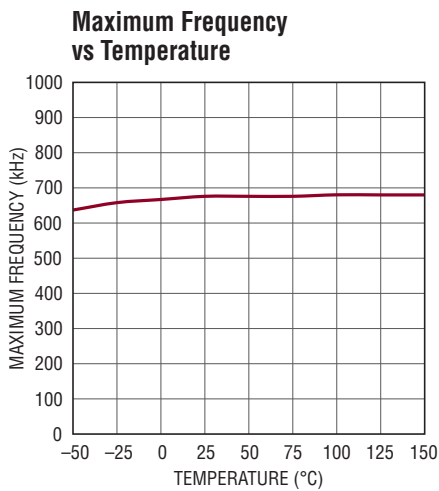
3512 G07



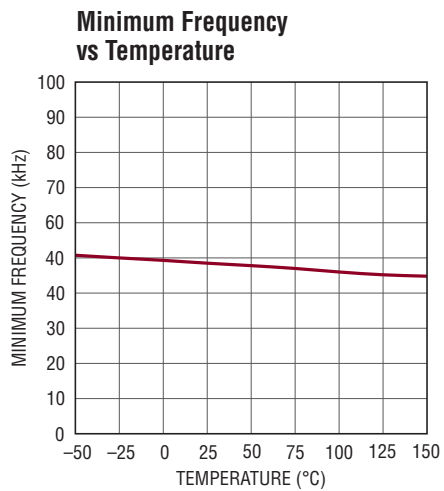
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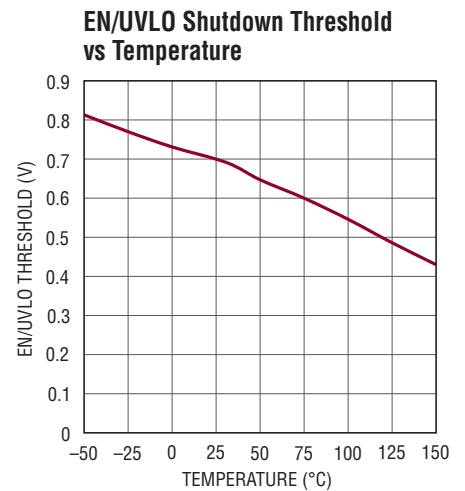
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3512 G10

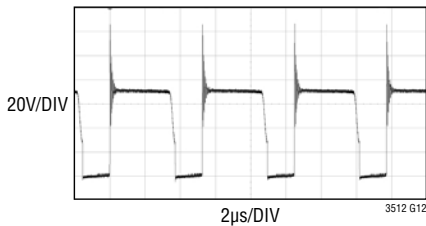


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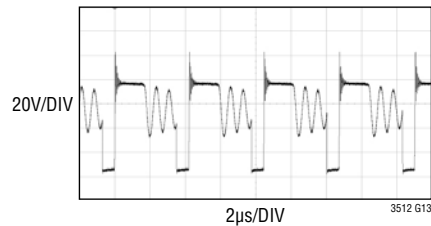


3512 G14

Boundary Mode Waveform



Light Load Discontinuous Mode Waveform



PIN FUNCTIONS

EN/UVLO (Pin 1): Enable/Undervoltage Lockout. The EN/UVLO pin is used to start up the LT3512. Pull the pin to 0V to shut down the LT3512. This pin has an accurate 1.21V threshold and can be used to program an undervoltage lockout (UVLO) threshold using a resistor divider from supply to ground. A 2.6 μ A pin current hysteresis allows the programming of undervoltage lockout (UVLO) hysteresis. EN/UVLO can be directly connected to V_{IN} . If left open circuit the part will not power up.

V_{IN} (Pin 3): Input Supply Pin. This pin supplies current to the internal start-up circuitry, and serves as a reference voltage for the DCM comparator and feedback circuitry. Must be locally bypassed with a capacitor.

GND (Pin 5, 8, 9): Ground Pins. All three pins should be tied directly to the local ground plane.

BIAS (Pin 6): Bias Voltage. This pin supplies current to the switch driver and internal circuitry of the LT3512. This pin may also be connected to V_{IN} if a third winding is not used and if $V_{IN} < 20V$. The part can operate down to 4.5V when BIAS and V_{IN} are connected together. If a third winding is used, the BIAS voltage should be lower than the input voltage and greater than 3.3V for proper operation. BIAS must be bypassed with a 4.7 μ F capacitor placed close to the pin.

VC (Pin 10): Compensation Pin for Internal Error Amplifier. Connect a series RC from this pin to ground to compensate the switching regulator. An additional 100pF capacitor from this pin to ground helps eliminate noise.

T_C (Pin 11): Output Voltage Temperature Compensation. Connect a resistor to ground to produce a current proportional to absolute temperature to be sourced into the R_{REF} node.

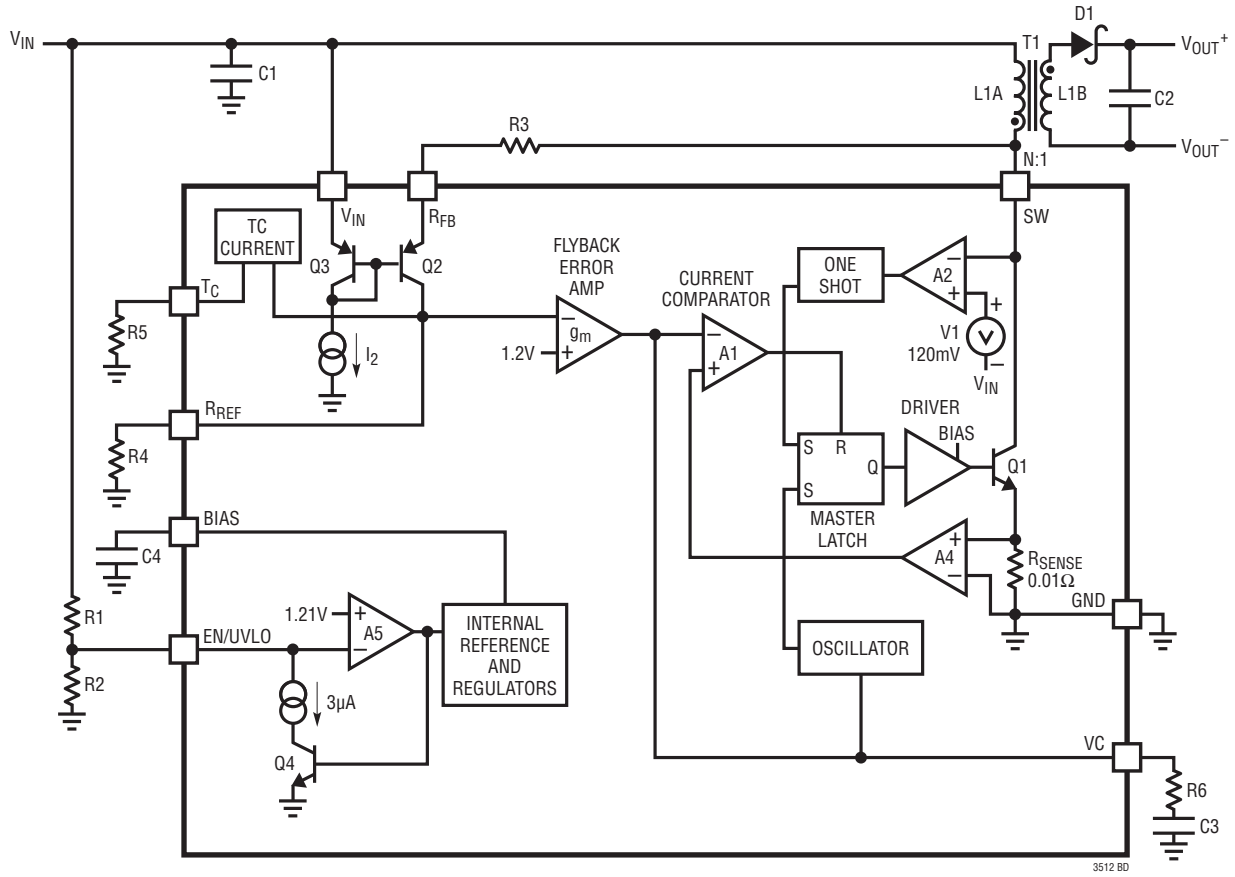
$$I_{TC} = 0.55V/R_{TC}$$

R_{REF} (Pin 12): Input Pin for External Ground-Referenced Reference Resistor. The resistor at this pin should be 10k. For nonisolated applications, a traditional resistor voltage divider from V_{OUT} may be connected to this pin.

R_{FB} (Pin 14): Input Pin for External Feedback Resistor. This pin is connected to the transformer primary (V_{SW}). The ratio of this resistor to the R_{REF} resistor, times the internal bandgap reference, determines the output voltage (plus the effect of any non-unity transformer turns ratio). For nonisolated applications, this pin should be connected to V_{IN} .

SW (Pin 16): Switch Pin. Collector of the internal power switch. Minimize trace area at this pin to minimize EMI and voltage spikes.

BLOCK DIAGRAM



OPERATION

The LT3512 is a current mode switching regulator IC designed specifically for the isolated flyback topology. The key problem in isolated topologies is how to communicate information regarding the output voltage from the isolated secondary side of the transformer to the primary side. Historically, optoisolators or extra transformer windings communicate this information across the transformer. Optoisolator circuits waste output power, and the extra components increase the cost and physical size of the power supply. Optoisolators can also exhibit trouble due to limited dynamic response, nonlinearity, unit-to-unit variation and aging over life. Circuits employing an extra transformer winding also exhibit deficiencies. Using an extra winding adds to the transformer's physical size and cost, and dynamic response is often mediocre.

In the LT3512, the primary-side flyback pulse provides information about the isolated output voltage. In this manner, neither optoisolator nor extra transformer winding is required for regulation. Two resistors program the output voltage. Since this IC operates in boundary mode, the part calculates output voltage from the switch pin when the secondary current is almost zero.

The Block Diagram shows an overall view of the system. Many of the blocks are similar to those found in traditional switching regulators including internal bias regulator, oscillator, logic, current amplifier, current comparator, driver, and output switch. The novel sections include a special flyback error amplifier and a temperature compensation circuit. In addition, the logic system contains additional logic for boundary mode operation.

The LT3512 features boundary mode control, where the part operates at the boundary between continuous conduction mode and discontinuous conduction mode. The VC pin

controls the current level just as it does in normal current mode operation, but instead of turning the switch on at the start of the oscillator period, the part turns on the switch when the secondary-side winding current is zero.

Boundary Mode Operation

Boundary mode is a variable frequency, current mode switching scheme. The switch turns on and the inductor current increases until a VC pin controlled current limit. After the switch turns off, the voltage on the SW pin rises to the output voltage divided by the secondary-to-primary transformer turns ratio plus the input voltage. When the secondary current through the diode falls to zero, the SW pin voltage falls below V_{IN} . A discontinuous conduction mode (DCM) comparator detects this event and turns the switch back on.

Boundary mode returns the secondary current to zero every cycle, so parasitic resistive voltage drops do not cause load regulation errors. Boundary mode also allows the use of a smaller transformer compared to continuous conduction mode and does not exhibit subharmonic oscillation.

At low output currents, the LT3512 delays turning on the switch, and thus operates in discontinuous mode. Unlike traditional flyback converters, the switch has to turn on to update the output voltage information. Below 0.6V on the VC pin, the current comparator level decreases to its minimum value, and the internal oscillator frequency decreases. With the decrease of the internal oscillator, the part starts to operate in DCM. The output current is able to decrease while still allowing a minimum switch off time for the flyback error amplifier. The typical minimum internal oscillator frequency with VC equal to 0V is 40kHz.

APPLICATIONS INFORMATION

PSEUDO DC THEORY

In the Block Diagram, R_{REF} (R4) and R_{FB} (R3) are external resistors used to program the output voltage. The LT3512 operates similar to traditional current mode switchers, except in the use of a unique error amplifier, which derives its feedback information from the flyback pulse.

Operation is as follows: when the output switch, Q1, turns off, its collector voltage rises above the V_{IN} rail. The amplitude of this flyback pulse, i.e., the difference between it and V_{IN} , is given as:

$$V_{FLBK} = (V_{OUT} + V_F + I_{SEC} \cdot ESR) \cdot N_{PS}$$

V_F = D1 forward voltage

I_{SEC} = Transformer secondary current

ESR = Total impedance of secondary circuit

N_{PS} = Transformer effective primary-to-secondary turns ratio

R_{FB} and Q2 convert the flyback voltage into a current. Nearly all of this current flows through R_{REF} to form a ground-referred voltage. The resulting voltage forms the input to the flyback error amplifier. The flyback error amplifier samples the voltage information when the secondary side winding current is zero. The bandgap voltage, 1.20V, acts as the reference for the flyback error amplifier.

The relatively high gain in the overall loop will then cause the voltage at R_{REF} to be nearly equal to the bandgap reference voltage V_{BG} . The resulting relationship between V_{FLBK} and V_{BG} approximately equals:

$$\left(\frac{V_{FLBK}}{R_{FB}} \right) = \frac{V_{BG}}{R_{REF}} \text{ or } V_{FLBK} = V_{BG} \left(\frac{R_{FB}}{R_{REF}} \right)$$

V_{BG} = Internal bandgap reference

Combination of the preceding expression with earlier derivation of V_{FLBK} results in the following equation:

$$V_{OUT} = V_{BG} \left(\frac{R_{FB}}{R_{REF}} \right) \left(\frac{1}{N_{PS}} \right) - V_F - I_{SEC} (ESR)$$

The expression defines V_{OUT} in terms of the internal reference, programming resistors, transformer turns ratio and diode forward voltage drop. Additionally, it includes

the effect of nonzero secondary output impedance (ESR). Boundary control mode minimizes the effect of this impedance term.

Temperature Compensation

The first term in the V_{OUT} equation does not have temperature dependence, but the diode forward drop has a significant negative temperature coefficient. A positive temperature coefficient current source connects to the R_{REF} pin to compensate. A resistor to ground from the T_C pin sets the compensation current.

The following equation explains the cancellation of the temperature coefficient:

$$\frac{\delta V_F}{\delta T} = -\frac{R_{FB}}{R_{TC}} \cdot \frac{1}{N_{PS}} \cdot \frac{\delta V_{TC}}{\delta T} \text{ or,}$$

$$R_{TC} = \frac{-R_{FB}}{N_{PS}} \cdot \frac{1}{\delta V_F / \delta T} \cdot \frac{\delta V_{TC}}{\delta T} \approx \frac{R_{FB}}{N_{PS}}$$

$(\delta V_F / \delta T)$ = Diode's forward voltage temperature coefficient

$(\delta V_{TC} / \delta T)$ = 2mV

V_{TC} = 0.55V

Experimentally verify the resulting value of R_{TC} and adjust as necessary to achieve optimal regulation over temperature.

The addition of a temperature coefficient current modifies the expression of output voltage as follows:

$$V_{OUT} = V_{BG} \left(\frac{R_{FB}}{R_{REF}} \right) \left(\frac{1}{N_{PS}} \right) - V_F - \left(\frac{V_{TC}}{R_{TC}} \right) \cdot \frac{R_{FB}}{N_{PS}} - I_{SEC} (ESR)$$

Output Power

A flyback converter has a complicated relationship between the input and output current compared to a buck or a boost. A boost has a relatively constant maximum input current regardless of input voltage and a buck has a relatively constant maximum output current regardless of input voltage. This is due to the continuous nonswitching behavior of the two currents. A flyback converter has both discontinuous input and output currents which makes it

APPLICATIONS INFORMATION

similar to a nonisolated buck-boost. The duty cycle will affect the input and output currents, making it hard to predict output power. In addition, the winding ratio can be changed to multiply the output current at the expense of a higher switch voltage.

The graphs in Figures 1-4 show the typical maximum output power possible for the output voltages 3.3V, 5V, 12V and 24V. The maximum power output curve is the calculated output power if the switch voltage is 100V during the off-time. 50V of margin is left for leakage voltage spike. To achieve this power level at a given input, a winding ratio value must be calculated to stress the switch to 100V, resulting in some odd ratio values. The following curves are examples of common winding ratio values and the amount of output power at given input voltages.

One design example would be a 5V output converter with a minimum input voltage of 36V and a maximum input voltage of 72V. A four-to-one winding ratio fits this design example perfectly and outputs close to 3.0W at 72V but lowers to 2.5W at 36V.

The equations below calculate output power:

$$\text{Power} = \eta \cdot V_{IN} \cdot D \cdot I_{PEAK} \cdot 0.5$$

$$\text{Efficiency} = \eta = \sim 83\%$$

$$\text{Duty cycle} = D = \frac{(V_{OUT} + V_F) \cdot N_{PS}}{(V_{OUT} + V_F) \cdot N_{PS} + V_{IN}}$$

$$\text{Peak switch current} = I_{PEAK} = 0.44A$$

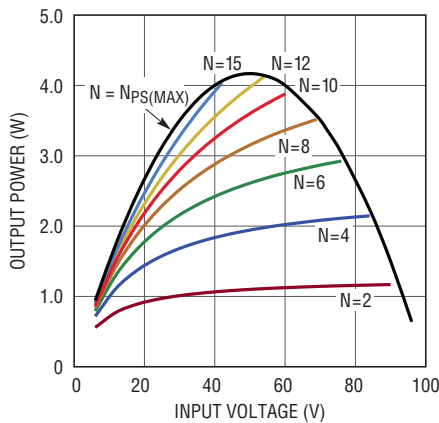


Figure 1. Output Power for 3.3V Output

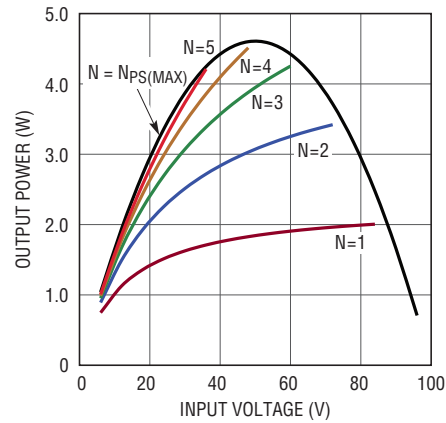


Figure 3. Output Power for 12V Output

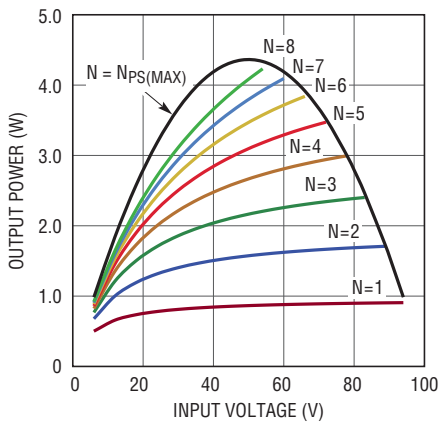


Figure 2. Output Power for 5V Output

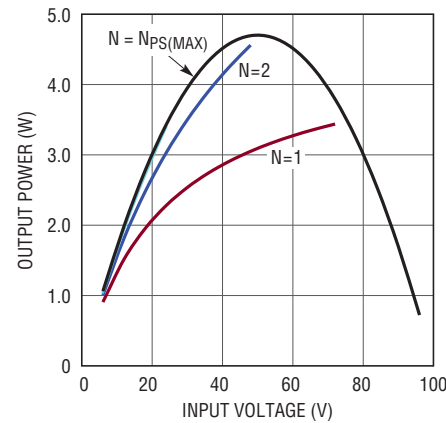


Figure 4. Output Power for 24V Output

APPLICATIONS INFORMATION

Table 1. Predesigned Transformers

TRANSFORMER PART NUMBER	L _{PRI} (μH)	LEAKAGE (μH)	N _P :N _S :N _B	ISOLATION (V)	SATURATION CURRENT (mA)	VENDOR	TARGET APPLICATIONS
750311559	175	1.5	4:1:1	1500	800	Würth Elektronik	48V to 5V, 0.5A 24V to 5V, 0.38A 12V to 5V, 0.2A 48V to 3.3V, 0.59A 24V to 3.3V, 0.48A 12V to 3.3V, 0.29A
750311573	200	2	6:1:2	1500	800	Würth Elektronik	24V to 5V, 0.45A 12V to 5V, 0.23A 48V to 3.3V, 0.7A 24V to 3.3V, 0.59A 12V to 3.3V, 0.33A
750311662	151	2	1:1:0.2	1500	800	Würth Elektronik	48V to 24V, 0.11A
750311661	150	1.85	2:1:0.66	1500	1.1A	Würth Elektronik	48V to 15V, 0.2A 48V to 12V, 0.22A 24V to 15V, 0.15A 12V to 15V, 0.075A
750311839	200	3	2:1:1	1500	800	Würth Elektronik	48V to ±15V, 0.1A 48V to ±12V, 0.11A 24V to ±15V, 0.075A
750311964	100	0.7	1:5:5	1500	900	Würth Elektronik	12V to ± 70V, 0.007A 12V to ± 100V, 0.005A 12V to ± 150V, 0.004A
750311966	120	0.45	1:5:0.5	1500	900	Würth Elektronik	12V to +120V& -12V, 0.005A
750311692	80	2	1:5:5	1500	1.0A	Würth Elektronik	12V ± 70V, 0.007A
10396-T025	200	2.0	4:1:1.2	1500	800	Sumida	48V to 5V, 0.5A 24V to 5V, 0.38A 12V to 5V, 0.2A 48V to 3.3V, 0.59A 24V to 3.3V, 0.48A 12V to 3.3V, 0.29A
10396-T027	200	2.0	6:1:2	1500	800	Sumida	24V to 5V, 0.45A 12V to 5V, 0.23A 48V to 3.3V, 0.7A 24V to 3.3V, 0.59A 12V to 3.3V, 0.33A
01355-T058	125	2.0	1:1:0.2	1500	800	Sumida	48V to 24V, 0.11A
10396-T023	200	2.0	2:1:0.33	1500	800	Sumida	48V to 15V, 0.2A 48V to 12V, 0.22A 24V to 15V, 0.15A 12V to 15V, 0.075A
10396-T029	200	2.5	2:1:1	1500	800	Sumida	48V to ±15V, 0.1A 48V to ±12V, 0.11A 24V to ±15V, 0.075A
01355-T061	100	2	1:5:5	1500	800	Sumida	12V to ± 70V, 0.007A 12V to ± 100V, 0.005A 12V to ± 150V, 0.004A

APPLICATIONS INFORMATION

TRANSFORMER DESIGN CONSIDERATIONS

Successful application of the LT3512 relies on proper transformer specification and design. Carefully consider the following information in addition to the traditional guidelines associated with high frequency isolated power supply transformer design.

Linear Technology has worked with several leading magnetic component manufacturers to produce pre-designed flyback transformers for use with the LT3512. Table 1 shows the details of these transformers.

Turns Ratio

Note that when using an R_{FB}/R_{REF} resistor ratio to set output voltage, the user has relative freedom in selecting a transformer turns ratio to suit a given application. In contrast, the use of simple ratios of small integers, e.g., 1:1, 2:1, 3:2, provides more freedom in setting total turns and mutual inductance.

Typically, choose the transformer turns to maximize available output power. For low output voltages (3.3V or 5V), a N:1 turns ratio can be used with multiple primary windings relative to the secondary to maximize the transformer's current gain (and output power). However, remember that the SW pin sees a voltage that is equal to the maximum input supply voltage plus the output voltage multiplied by the turns ratio. In addition, leakage inductance will cause a voltage spike ($V_{LEAKAGE}$) on top of this reflected voltage. This total quantity needs to remain below the absolute maximum rating of the SW pin to prevent breakdown of the internal power switch. Together these conditions place an upper limit on the turns ratio, N, for a given application. Choose a turns ratio low enough to ensure:

$$N < \frac{150V - V_{IN(MAX)} - V_{LEAKAGE}}{V_{OUT} + V_F}$$

For larger N:1 values, choose a transformer with a larger physical size to deliver additional current. In addition, choose a large enough inductance value to ensure that the off-time is long enough to measure the output voltage.

For lower output power levels, choose a 1:1 or 1:N transformer for the absolute smallest transformer size. A 1:N transformer will minimize the magnetizing inductance (and minimize size), but will also limit the available output power. A higher 1:N turns ratio makes it possible to have very high output voltages without exceeding the breakdown voltage of the internal power switch.

The turns ratio is an important element in the isolated feedback scheme. Make sure the transformer manufacturer guarantees turns ratio accuracy within $\pm 1\%$.

Saturation Current

The current in the transformer windings should not exceed its rated saturation current. Energy injected once the core is saturated will not be transferred to the secondary and will instead be dissipated in the core. Information on saturation current should be provided by the transformer manufacturers. Table 1 lists the saturation current of the transformers designed for use with the LT3512.

Primary Inductance Requirements

The LT3512 obtains output voltage information from the reflected output voltage on the switch pin. The conduction of secondary winding current reflects the output voltage on the primary. The sampling circuitry needs a minimum of 400ns to settle and sample the reflected output voltage. In order to ensure proper sampling, the secondary winding needs to conduct current for a minimum of 400ns. The following equation gives the minimum value for primary-side magnetizing inductance:

$$L_{PRI} \geq \frac{t_{OFF(MIN)} \cdot N_{PS} \cdot (V_{OUT} + V_F)}{I_{PEAK(MIN)}}$$

$$t_{OFF(MIN)} = 400ns$$

$$I_{PEAK(MIN)} = 100mA$$

In addition to the primary inductance requirement for sampling time, the LT3512 has internal circuit constraints that prevent the switch from staying on for less than 100ns. If the inductor current exceeds the desired current limit

APPLICATIONS INFORMATION

during that time, oscillation may occur at the output as the current control loop will lose its ability to regulate. The following equation based on maximum input voltage must also be followed in selecting primary-side magnetizing inductance:

$$L_{PRI} \geq \frac{t_{ON(MIN)} \cdot V_{IN(MAX)}}{I_{PEAK(MIN)}}$$

$$t_{ON(MIN)} = 100\text{ns}$$

$$I_{PEAK(MIN)} = 100\text{mA}$$

Leakage Inductance and Clamp Circuits

Transformer leakage inductance (on either the primary or secondary) causes a voltage spike to appear at the primary after the output switch turns off. This spike is increasingly prominent at higher load currents where more stored energy must be dissipated. When designing an application, adequate margin should be kept for the effect of leakage voltage spikes. In most cases the reflected output voltage on the primary plus V_{IN} should be kept below 100V. This leaves at least 50V of margin for the leakage spike across line and load conditions. A larger voltage margin will be needed for poorly wound transformers or for excessive leakage inductance. Figure 5 illustrates this point. Minimize transformer leakage inductance.

A clamp circuit is recommended for most applications. Two circuits that can protect the internal power switch include the RCD (resistor-capacitor-diode) clamp and the DZ (diode-Zener) clamp. The clamp circuits dissipate the stored energy in the leakage inductance. The DZ clamp is the recommended clamp for the LT3512. Simplicity of design, high clamp voltages, and low power levels make the DZ clamp the preferred solution. Additionally, a DZ clamp ensures well defined and consistent clamping voltages. Figure 5 shows the clamp effect on the switch waveform and Figure 6 shows the connection of the DZ clamp.

Proper care must be taken when choosing both the diode and the Zener diode. Schottky diodes are typically the best choice, but some PN diodes can be used if they turn on fast enough to limit the leakage inductance spike. Choose a diode that has a reverse-voltage rating higher than the maximum switch voltage. The Zener diode breakdown voltage should be chosen to balance power loss and switch

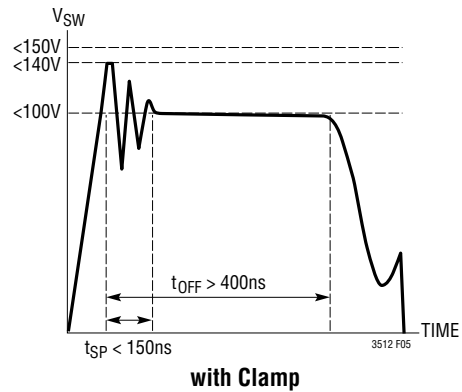
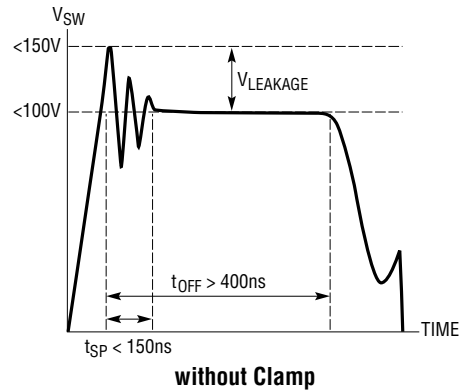


Figure 5. Maximum Voltages for SW Pin Flyback Waveform

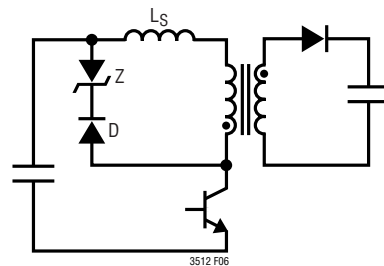


Figure 6. DZ Clamp

voltage protection. The best compromise is to choose the largest voltage breakdown. Use the following equation to make the proper choice:

$$V_{ZENER(MAX)} \leq 150\text{V} - V_{IN(MAX)}$$

For an application with a maximum input voltage of 72V, choose a 68V V_{ZENER} which has $V_{ZENER(MAX)}$ at 72V, which will be below the 78V maximum.

The power loss in the clamp will determine the power rating of the Zener diode. Power loss in the clamp is highest at maximum load and minimum input voltage. The switch

APPLICATIONS INFORMATION

current is highest at this point along with the energy stored in the leakage inductance. A 0.5W Zener will satisfy most applications when the highest V_{ZENER} is chosen. Choosing a low value for V_{ZENER} will cause excessive power loss as shown in the following equations:

$$DZ \text{ Power Loss} = \frac{1}{2} \cdot L_{\ell} \cdot I_{PK(VIN(MIN))}^2 \cdot f_{SW} \cdot \left(1 + \frac{N_{PS} \cdot (V_{OUT} + V_F)}{V_{ZENER} - N_{PS} \cdot (V_{OUT} + V_F)} \right)$$

L_{ℓ} = Leakage Inductance

$$I_{PK(VIN(MIN))} = \frac{V_{OUT} \cdot I_{OUT} \cdot 2}{\eta \cdot V_{IN(MIN)} \cdot D_{VIN(MIN)}}$$

$$f_{SW} = \frac{1}{t_{ON} + t_{OFF}} = \frac{1}{\frac{L_{PRI} \cdot I_{PK(VIN(MIN))}}{V_{IN(MIN)}} + \frac{L_{PRI} \cdot I_{PK(VIN(MIN))}}{N_{PS} \cdot (V_{OUT} + V_F)}}$$

Table 2 and 3 show some recommended diodes and Zener diodes.

Table 2. Recommended Zener Diodes

PART	V_{ZENER} (V)	POWER (W)	CASE	VENDOR
MMSZ5266BT1G	68	0.5	SOD-123	On Semi
MMSZ5270BT1G	91	0.5	SOD-123	
CMHZ5266B	68	0.5	SOD-123	Central Semiconductor
CMHZ5267B	75	0.5	SOD-123	
BZX84J-68	68	0.5	SOD323F	NXP
BZX100A	100	0.5	SOD323F	

Table 3. Recommended Diodes

PART	I (A)	$V_{REVERSE}$ (V)	VENDOR
DFLS1200	1.0	200	Diodes Inc.
DFLS1150	1.0	150	

Leakage Inductance Blanking

When the power switch turns off, the flyback pulse appears. However, a finite time passes before the transformer primary-side voltage waveform approximately represents the output voltage. Rise time on the SW node

and transformer leakage inductance cause the delay. The leakage inductance also causes a very fast voltage spike on the primary side of the transformer. The amplitude of the leakage spike is largest when power switch current is highest. Introduction of an internal fixed delay between switch turn-off and the start of sampling provides immunity to the phenomena discussed above. The LT3512 sets internal blanking to 150ns. In certain cases leakage inductance spikes last longer than the internal blanking, but will not significantly affect output regulation.

Secondary Leakage Inductance

In addition to primary leakage inductance, secondary leakage inductance exhibits an important effect on application design. Secondary leakage inductance forms an inductive divider on the transformer secondary. The inductive divider effectively reduces the size of the primary-referred flyback pulse. The smaller flyback pulse results in a higher regulated output voltage. The inductive divider effect of secondary leakage inductance is load independent. R_{FB}/R_{REF} ratio adjustments can accommodate this effect to the extent secondary leakage inductance is a constant percentage of mutual inductance (over manufacturing variations).

Winding Resistance Effects

Resistance in either the primary or secondary will reduce overall efficiency (P_{OUT}/P_{IN}). Good output voltage regulation will be maintained independent of winding resistance due to the boundary mode operation of the LT3512.

Bifilar Winding

A bifilar, or similar winding technique, is a good way to minimize troublesome leakage inductances. However, remember that this will also increase primary-to-secondary capacitance and limit the primary-to-secondary breakdown voltage, so bifilar winding is not always practical. The Linear Technology applications group is available and extremely qualified to assist in the selection and/or design of the transformer.

APPLICATIONS INFORMATION

APPLICATION DESIGN CONSIDERATIONS

Iterative Design Process

The LT3512 uses a unique sampling scheme to regulate the isolated output voltage. The use of this isolated scheme requires a simple iterative process to choose feedback resistors and temperature compensation. Feedback resistor values and temperature compensation resistance is heavily dependent on the application, transformer and output diode chosen.

Once resistor values are fixed after iteration, the values will produce consistent output voltages with the chosen transformer and output diode. Remember, the turns ratio of the transformer must be guaranteed within $\pm 1\%$. The transformer vendors mentioned in this data sheet can build transformers to this specification.

Selecting R_{FB} and R_{REF} Resistor Values

The following section provides an equation for setting R_{FB} and R_{REF} values. The equation should only serve as a guide. Follow the procedure outlined in the Design Procedure to set accurate values for R_{FB} , R_{REF} and R_{TC} using the iterative design procedure.

Rearrangement of the expression for V_{OUT} in the Temperature Compensation section, developed in the Operations section, yields the following expression for R_{FB} :

$$R_{FB} = \frac{R_{REF} \cdot N_{PS} [(V_{OUT} + V_F) + V_{TC}]}{V_{BG}}$$

where:

V_{OUT} = Output voltage

V_F = Switching diode forward voltage

N_{PS} = Effective primary-to-secondary turns ratio

$V_{TC} = 0.55V$

This equation assumes:

$$R_{TC} = \frac{R_{FB}}{N_{PS}}$$

The equation assumes the temperature coefficients of the diode and V_{TC} are equal, which is a good first order approximation.

Strictly speaking, the above equation defines R_{FB} not as an absolute value, but as a ratio of R_{REF} . So the next question is, what is the proper value for R_{REF} ? The answer is that R_{REF} should be approximately 10k. The LT3512 is trimmed and specified using this value of R_{REF} . If the impedance of R_{REF} varies considerably from 10k, additional errors will result. However, a variation in R_{REF} of several percent is acceptable. This yields a bit of freedom in selecting standard 1% resistor values to yield nominal R_{FB}/R_{REF} ratios.

Undervoltage Lockout (UVLO)

A resistive divider from V_{IN} to the EN/UVLO pin implements undervoltage lockout (UVLO). Figure 7 shows this configuration. The EN/UVLO pin threshold is set at 1.21V.

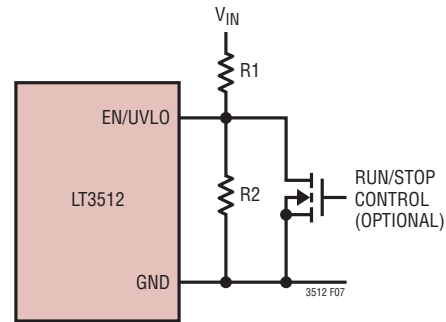


Figure 7. Undervoltage Lockout (UVLO)

In addition, the EN/UVLO pin draws 2.6 μA when the voltage at the pin is below 1.21V. This current provides user programmable hysteresis based on the value of $R1$. The effective UVLO thresholds are:

$$V_{IN(UVLO,RISING)} = \frac{1.2V \cdot (R1 + R2)}{R2} + 2.6\mu A \cdot R1$$

$$V_{IN(UVLO,FALLING)} = \frac{1.2V \cdot (R1 + R2)}{R2}$$

Figure 7 also shows the implementation of external shut-down control while still using the UVLO function. The NMOS grounds the EN/UVLO pin when turned on, and puts the LT3512 in shutdown with quiescent current draw of less than 1 μA .

Minimum Load Requirement

The LT3512 recovers output voltage information using the flyback pulse. The flyback pulse occurs once the switch turns off and the secondary winding conducts current. In

3512fb

APPLICATIONS INFORMATION

order to regulate the output voltage, the LT3512 needs to sample the flyback pulse. The LT3512 delivers a minimum amount of energy even during light load conditions to ensure accurate output voltage information. The minimum delivery of energy creates a minimum load requirement of 20mA to 25mA depending on the specific application. Verify minimum load requirements for each application. A Zener diode with a Zener breakdown of 20% higher than the output voltage can serve as a minimum load if pre-loading is not acceptable. For a 5V output, use a 6V Zener with cathode connected to the output.

BIAS Pin Considerations

The BIAS pin powers the internal circuitry of the LT3512. Three unique configurations exist for regulation of the BIAS pin. In the first configuration, the internal LDO drives the BIAS pin internally from the V_{IN} supply. In the second setup, the V_{IN} supply directly drives the BIAS pin through a direct connection bypassing the internal LDO. This configuration will allow the part to operate down to 4.5V and up to 15V. In the third configuration, an external supply or third winding drives the BIAS pin. Use this option when a voltage supply exists lower than the input supply. Drive the BIAS pin with a voltage supply higher than 3.3V to disable the internal LDO. The lower voltage supply provides a more efficient source of power for internal circuitry.

Overdriving the BIAS Pin with a Third Winding

The LT3512 provides excellent output voltage regulation without the need for an opto-coupler, or third winding, but for some applications with higher input voltages (>20V), an additional winding (often called a third winding) improves overall system efficiency. Design the third winding to output a voltage between 3.3V and 12V. For a typical 48V_{IN} application, overdriving the BIAS pin improves efficiency 4% to 5%.

Loop Compensation

An external resistor-capacitor network compensates the LT3512 on the VC pin. Typical compensation values are in the range of $R_C = 15k$ and $C_C = 4.7nF$ (see the numerous schematics in the Typical Applications section for other possible values). Proper choice of both R_C and C_C is important to achieve stability and acceptable transient response. For

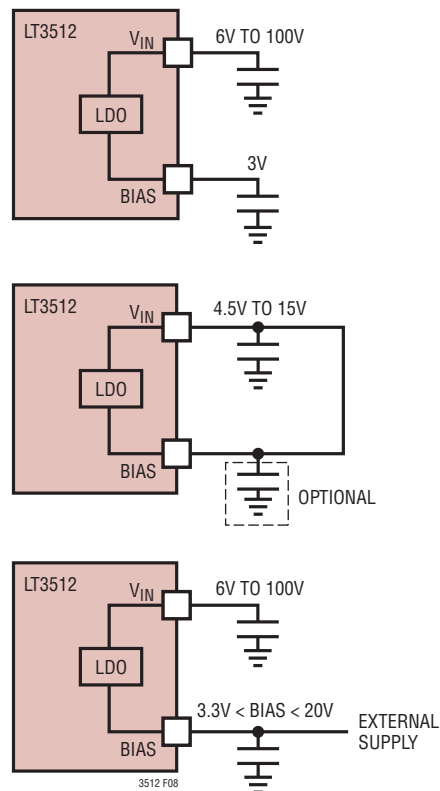


Figure 8. BIAS Pin Configurations

example, vulnerability to high frequency noise and jitter result when R_C is too large. On the other hand, if R_C is too small, transient performance suffers. The inverse is true with respect to the value of C_C . Transient response suffers with too large of a C_C , and instability results from too small a C_C . The specific value for R_C and C_C will vary based on the application and transformer choice. Verify specific choices with board level evaluation and transient response performance.

DESIGN PROCEDURE/DESIGN EXAMPLE

Use the following design procedure as a guide to designing applications for the LT3512. Remember, the unique sampling architecture requires an iterative process for choosing correct resistor values.

The design example involves designing a 15V output with a 200mA load current and an input range from 36V to 72V.

$V_{IN(MIN)} = 36V$, $V_{IN(NOM)} = 48V$, $V_{IN(MAX)} = 72V$, $V_{OUT} = 15V$ and $I_{OUT} = 200mA$

APPLICATIONS INFORMATION

Step 1: Select the transformer turns ratio.

$$N_{PS} < \frac{V_{SW(MAX)} - V_{IN(MAX)} - V_{LEAKAGE}}{V_{OUT} + V_F}$$

$V_{SW(MAX)}$ = Max rating of internal switch = 150V

$V_{LEAKAGE}$ = Margin for transformer leakage spike = 40V

V_F = Forward voltage of output diode = assume approximately ~ 0.5V

Example:

$$N_{PS} < \frac{150V - 72V - 40V}{15V + 0.5V}$$

$$N_{PS} < 2.45$$

$$N_{PS} = 2$$

The choice of turns ratio is critical in determining output power as shown earlier in the Output Power section. At this point, a third winding can be added to the transformer to drive the BIAS pin of the LT3512 for higher efficiencies. Choose a turns ratio that sets the third winding voltage to regulate between 3.3V and 6V for maximum efficiency.

Choose a third winding ratio to drive BIAS winding with 5V. (Optional)

Example:

$$\frac{N_{THIRD}}{N_S} = \frac{V_{THIRD}}{V_{OUT}} = \frac{5V}{15V} = 0.33$$

The turns ratio of the transformer chosen is as follows $N_{PRIMARY} : N_{SECONDARY} : N_{THIRD} = 2:1:0.33$.

Step 2: Calculate maximum power output at minimum V_{IN} .

$$P_{OUT(VIN(MIN))} = \eta \cdot V_{IN(MIN)} \cdot I_{IN} = \eta \cdot V_{IN(MIN)} \cdot D \cdot I_{PEAK} \cdot 0.5$$

$$D = \frac{(V_{OUT} + V_F) \cdot N_{PS}}{(V_{OUT} + V_F) \cdot N_{PS} + V_{IN(MIN)}}$$

η = Efficiency = ~83%

I_{PEAK} = Peak switch current = 0.44A

Example:

$$D = 0.46$$

$$P_{OUT(VIN(MIN))} = 3W$$

$$I_{OUT(VIN(MIN))} = P_{OUT(VIN(MIN))} / V_{OUT} = 0.2A$$

The chosen turns ratio satisfies the output current requirement of 200mA. If the output current was too low, the minimum input voltage could be adjusted higher. The turns ratio in this example is set to its highest ratio given switch voltage requirements and margin for leakage inductance voltage spike.

Step 3: Determine primary inductance, switching frequency and saturation current.

Primary inductance for the transformer must be set above a minimum value to satisfy the minimum off and on time requirements.

$$L_{PRI} \geq \frac{t_{OFF(MIN)} \cdot N_{PS} \cdot (V_{OUT} + V_F)}{I_{PEAK(MIN)}}$$

$$t_{OFF(MIN)} = 400ns$$

$$I_{PEAK(MIN)} = 100mA$$

$$L_{PRI} \geq \frac{t_{ON(MIN)} \cdot V_{IN(MAX)}}{I_{PEAK(MIN)}}$$

$$t_{ON(MIN)} = 100ns$$

$$I_{PEAK(MIN)} = 100mA$$

Example:

$$L_{PRI} \geq \frac{400ns \cdot 2 \cdot (15 + 0.5)}{0.1}$$

$$L_{PRI} \geq 124\mu H$$

$$L_{PRI} \geq \frac{100ns \cdot 72}{0.1}$$

$$L_{PRI} \geq 72\mu H$$

APPLICATIONS INFORMATION

In addition, primary inductance will determine switching frequency.

$$f_{SW} = \frac{1}{t_{ON} + t_{OFF}} = \frac{1}{\frac{L_{PRI} \cdot I_{PEAK}}{V_{IN}} + \frac{L_{PRI} \cdot I_{PEAK}}{N_{PS} \cdot (V_{OUT} + V_F)}}$$

$$I_{PEAK} = \frac{V_{OUT} \cdot I_{OUT} \cdot 2}{\eta \cdot V_{IN} \cdot D}$$

Example:

Let's calculate switching frequency at our nominal V_{IN} of 48V.

$$D = \frac{(15 + 0.5) \cdot 2}{(15 + 0.5) \cdot 2 + 48} = 0.39$$

$$I_{PEAK} = \frac{15V \cdot 0.2A \cdot 2}{0.83 \cdot 48V \cdot 0.39} = 0.39A$$

Let's choose $L_{PRI} = 200\mu H$. Remember, most transformers specify primary inductance with a tolerance of $\pm 20\%$.

$$f_{SW} = 240kHz$$

Finally, the transformer needs to be rated for the correct saturation current level across line and load conditions. In the given example, the worst-case condition for switch current is at minimum V_{IN} and maximum load.

$$I_{PEAK} = \frac{V_{OUT} \cdot I_{OUT} \cdot 2}{\eta \cdot V_{IN} \cdot D}$$

$$I_{PEAK} = \frac{15V \cdot 0.2A \cdot 2}{0.83 \cdot 36V \cdot 0.46} = 0.44A$$

Ensure that the saturation current covers steady-state operation, start-up and transient conditions. To satisfy these conditions, choose a saturation current 50% or more higher than the steady-state calculation. In this example, a saturation current between 700mA and 800mA is chosen.

Table 1 presents a list of pre-designed flyback transformers. For this application, the Sumida 10396-T023 transformer will be used.

Step 4: Choose the correct output diode.

The two main criteria for choosing the output diode include forward current rating and reverse voltage rating. The maximum load requirement is a good first-order guess at the average current requirement for the output diode. A better metric is RMS current.

$$I_{RMS} = I_{PEAK(VIN(MIN))} \cdot N_{PS} \cdot \sqrt{\frac{1 - D_{VIN(MIN)}}{3}}$$

Example:

$$I_{RMS} = 0.44 \cdot 2 \cdot \sqrt{\frac{1 - 0.46}{3}} = 0.37A$$

Next calculate reverse voltage requirement using maximum V_{IN} :

$$V_{REVERSE} = V_{OUT} + \frac{V_{IN(MAX)}}{N_{PS}}$$

Example:

$$V_{REVERSE} = 15V + \frac{72V}{2} = 51V$$

A 1.0A, 60V diode from Diodes Inc. (DFLS160) will be used.

Step 5: Choose an output capacitor.

The output capacitor choice should minimize output voltage ripple and balance the trade-off between size and cost for a larger capacitor. Use the equation below at nominal V_{IN} :

$$C = \frac{I_{OUT} \cdot D}{\Delta V_{OUT} \cdot f_{SW}}$$

Example:

Design for ripple levels below 50mV.

$$C = \frac{0.2A \cdot 0.39}{0.05V \cdot 240kHz} = 6.5\mu F$$

A 22 μF , 25V output capacitor is chosen. Remember ceramic capacitors lose capacitance with applied voltage. The capacitance can drop to 40% of quoted capacitance at the max voltage rating.

APPLICATIONS INFORMATION

Step 6: Design clamp circuit.

The clamp circuit protects the switch from leakage inductance spike. A DZ clamp is the preferred clamp circuit. The Zener and the diode need to be chosen.

The maximum Zener value is set according to the maximum V_{IN} :

$$V_{ZENER(MAX)} \leq 150V - V_{IN(MAX)}$$

Example:

$$V_{ZENER(MAX)} \leq 150V - 72V$$

$$V_{ZENER(MAX)} \leq 78V$$

In addition, power loss in the clamp circuit is inversely related to the clamp voltage as shown previously. Higher clamp voltages lead to lower power loss.

A 68V Zener with a maximum of 72V will provide optimal protection and minimize power loss. Half-watt Zeners will satisfy most clamp applications involving the LT3512. Power loss can be calculated using the equations presented in the Leakage Inductance and Clamp Circuit section.

The Zener chosen is a 68V 0.5W Zener from On Semiconductor (MMSZ5266BT1G).

Choose a diode that is fast and has sufficient reverse voltage breakdown:

$$V_{REVERSE} > V_{SW(MAX)}$$

$$V_{SW(MAX)} = V_{IN(MAX)} + V_{ZENER(MAX)}$$

Example:

$$V_{REVERSE} > 140V$$

The diode needs to handle the peak switch current of the switch which was determined to be 0.45A. A 200V, 1.0A diode from Diodes Inc. (DFLS1200) is chosen.

Step 7: Compensation.

Compensation will be optimized towards the end of the design procedure. Connect a resistor and capacitor from the VC node to ground. Use a 15k resistor and a 4.7nF capacitor.

Step 8: Select R_{FB} and R_{TC} Resistors.

Use the following equations to choose starting values for R_{FB} and R_{TC} . Set R_{REF} to 10k.

$$R_{FB} = \frac{(V_{OUT} + V_F + 0.55V) \cdot N_{PS} \cdot R_{REF}}{1.2V}$$

$$R_{REF} = 10k$$

$$R_{TC} = \frac{R_{FB}}{N_{PS}}$$

Example:

$$R_{FB} = \frac{(15 + 0.5 + 0.55V) \cdot 2 \cdot 10k}{1.2V} = 267k$$

$$R_{TC} = \frac{267k}{2} = 133k$$

Step 9: Adjust R_{FB} based on output voltage.

Power up the application with application components connected and measure the regulated output voltage. Readjust R_{FB} based on the measured output voltage.

$$R_{FB(NEW)} = \frac{V_{OUT}}{V_{OUT(MEAS)}} \cdot R_{FB(OLD)}$$

Example:

$$R_{FB(NEW)} = \frac{15V}{16.7V} \cdot 267k = 237k$$

Step 10: Remove R_{TC} and measure output voltage over temperature.

Measure output voltage in a controlled temperature environment like an oven to determine the output temperature coefficient. Measure output voltage at a consistent load current and input voltage, across the temperature range of operation. This procedure will optimize line and load regulation over temperature.

Calculate the temperature coefficient of V_{OUT} :

$$\frac{\Delta V_{OUT}}{\Delta Temp} = \frac{V_{OUT(HOT)} - V_{OUT(COLD)}}{T_{HOT(°C)} - T_{COLD(°C)}}$$

APPLICATIONS INFORMATION

Example:

V_{OUT} measured at 200mA and 48V_{IN}

$$\frac{\Delta V_{OUT}}{\Delta Temp} = \frac{15.42V - 15.02V}{125^{\circ}C - (-50^{\circ}C)} = 2.26mV/^{\circ}C$$

Step 11: Calculate new value for R_{TC}.

$$R_{TC(NEW)} = \frac{R_{FB}}{N_{PS}} \cdot \frac{1.85mV/^{\circ}C}{\frac{\Delta V_{OUT}}{\Delta Temp}}$$

Example:

$$R_{TC(NEW)} = \frac{237k}{2} \cdot \frac{1.85}{2.26} = 97.6k$$

Step 12: Place new value for R_{TC}, measure V_{OUT}, and readjust R_{FB} due to R_{TC} change.

$$R_{FB(NEW)} = \frac{V_{OUT}}{V_{OUT(MEAS)}} \cdot R_{FB(OLD)}$$

Example:

$$R_{FB(NEW)} = \frac{15V}{14.7V} \cdot 237k = 243k$$

Step 13: Verify new values of R_{FB} and R_{TC} over temperature.

Measure output voltage over temperature with R_{TC} connected.

Step 14: Optimize compensation.

Now that values for R_{FB} and R_{TC} are fixed, optimize the compensation. Compensation should be optimized for transient response to load steps on the output. Check transient response across the load range.

Example:

The optimal compensation for the application is:

$$R_C = 18.7k, C_C = 4.7nF$$

Step 15: Ensure minimum load.

Check minimum load requirement at maximum input voltage. The minimum load occurs at the point where the output voltage begins to climb up as the converter delivers more energy than what is consumed at the output.

Example:

The minimum load at an input voltage of 72V is:

$$11mA$$

Step 16: EN/UVLO resistor values.

Determine amount of hysteresis required.

$$\text{Voltage hysteresis} = 2.6\mu A \cdot R1$$

Example:

Choose 2V of hysteresis.

$$R1 = \frac{2V}{2.6\mu A} = 768k$$

Determine UVLO Threshold.

$$V_{IN(UVLO,FALLING)} = \frac{1.2V \cdot (R1 + R2)}{R2}$$

$$R2 = \frac{1.2V \cdot R1}{V_{IN(UVLO,FALLING)} - 1.2V}$$

Set UVLO falling threshold to 30V.

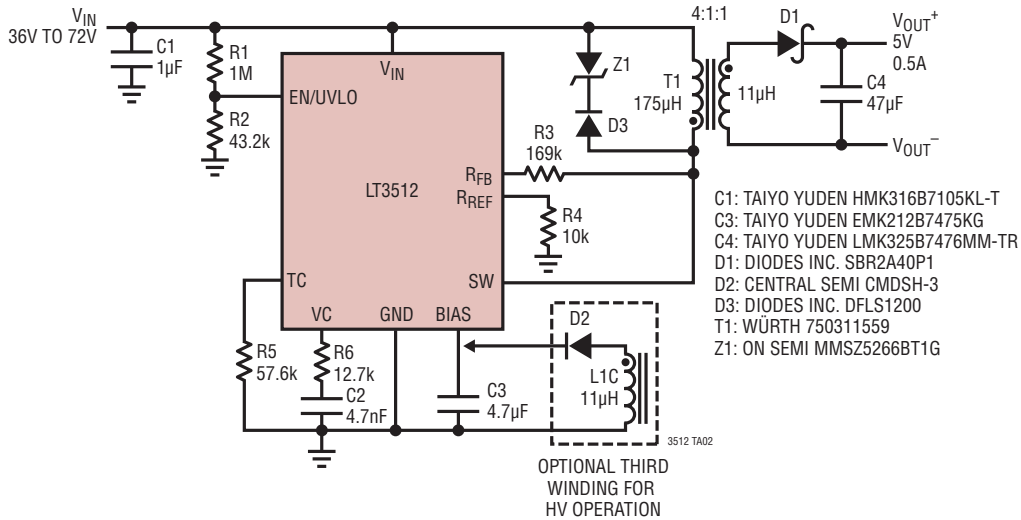
$$R2 = \frac{1.2V \cdot 768k}{30V - 1.2V} = 32.4k$$

$$V_{IN(UVLO,FALLING)} = \frac{1.2V \cdot (R1 + R2)}{R2} = \frac{1.2V \cdot (768k + 32.4k)}{32.4k} = 30V$$

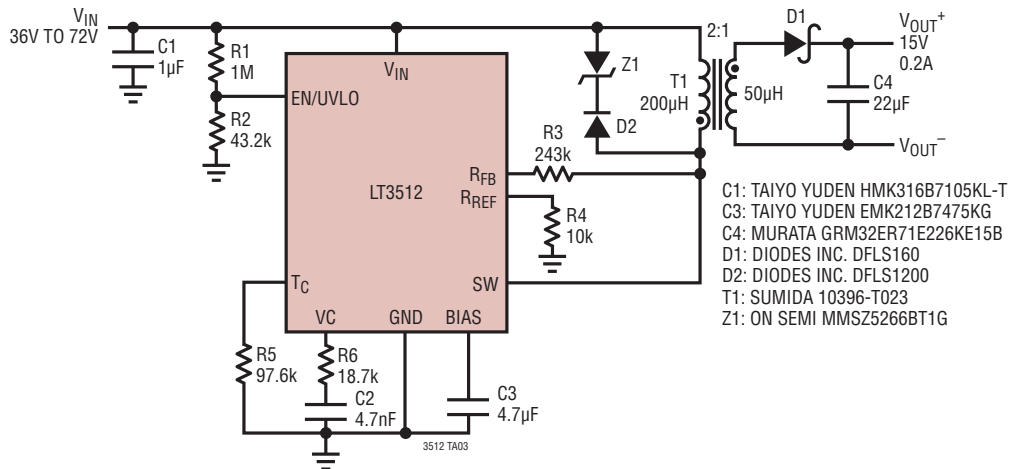
$$V_{IN(UVLO,RISING)} = V_{IN(UVLO,FALLING)} + 2.6\mu A \cdot R1 = 30V + 2.6\mu A \cdot 768k = 32V$$

TYPICAL APPLICATIONS

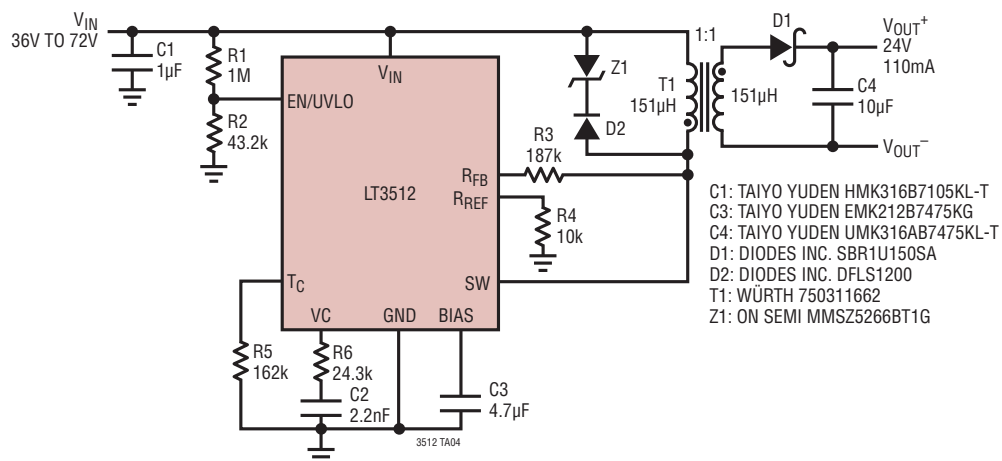
48V to 5V Isolated Flyback Converter



48V to 15V Isolated Flyback Converter

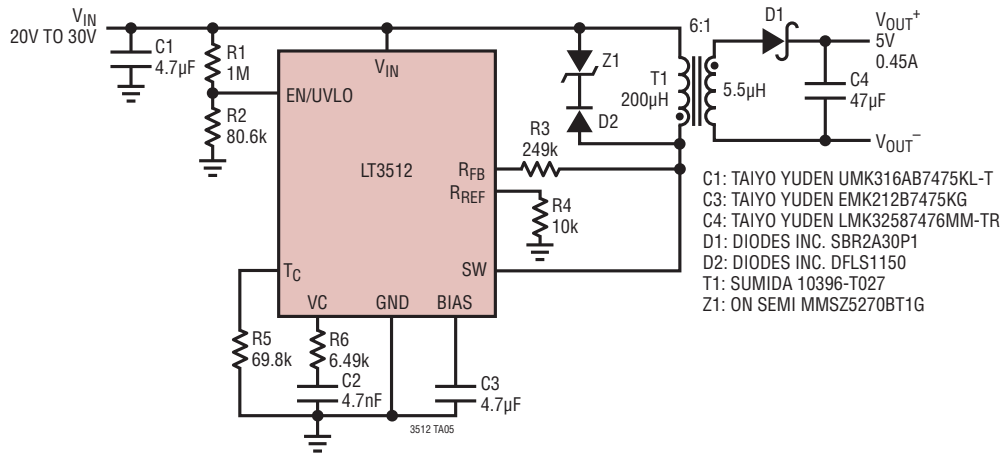


48V to 24V Isolated Flyback Converter

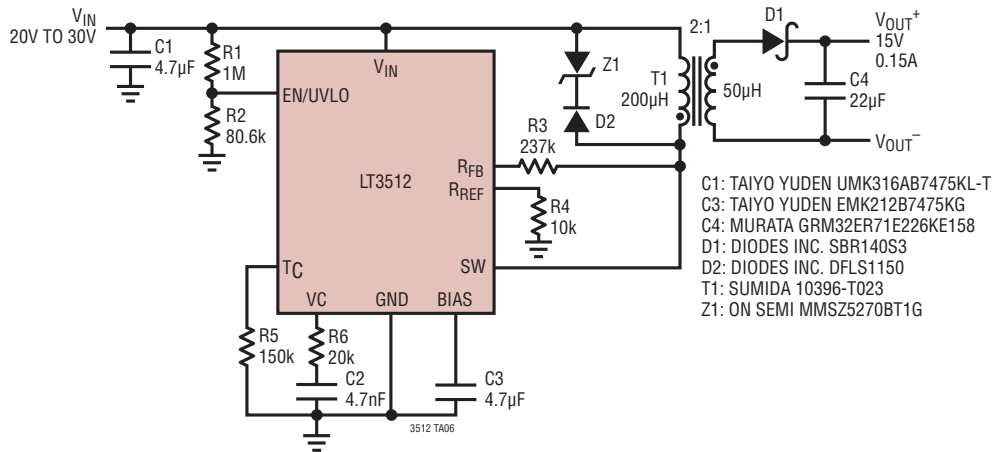


TYPICAL APPLICATIONS

24V to 5V Isolated Flyback Converter

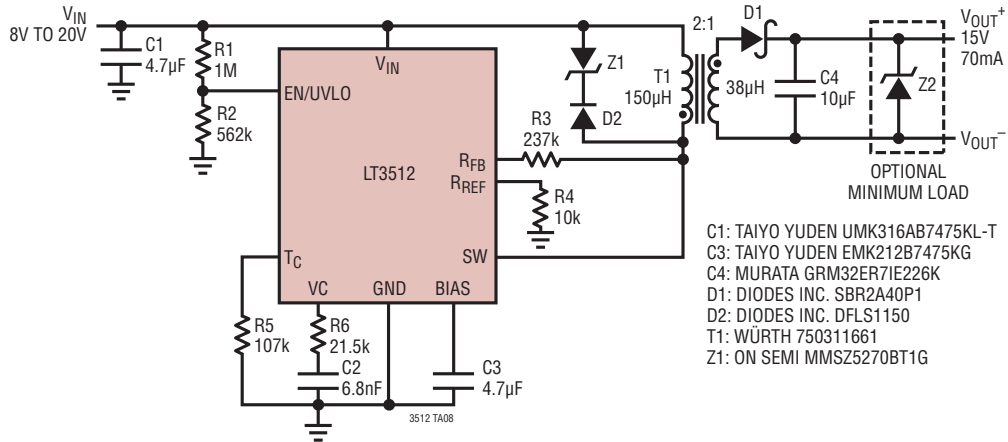


24V to 15V Isolated Flyback Converter

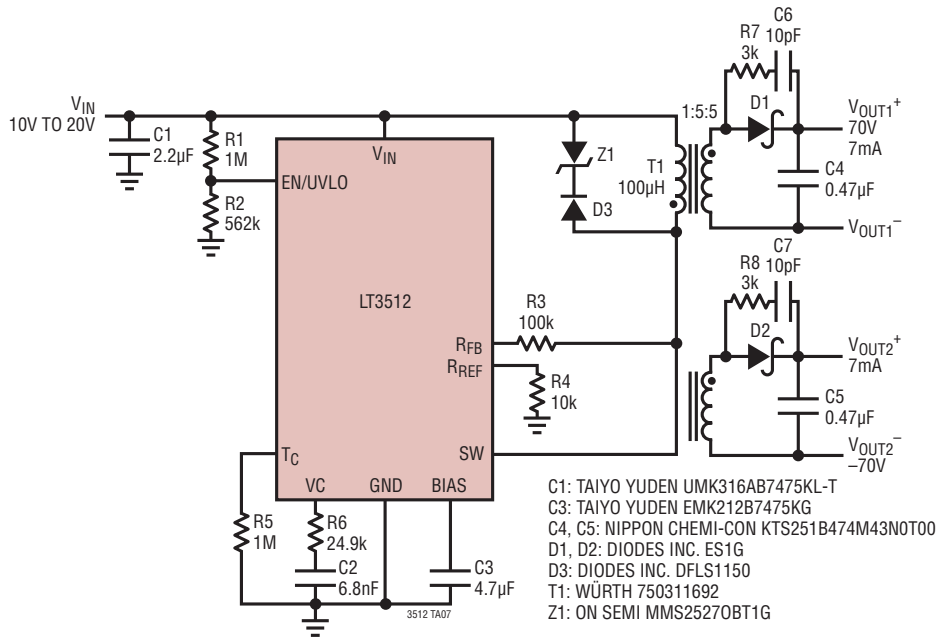


TYPICAL APPLICATIONS

12V to 15V Isolated Flyback Converter

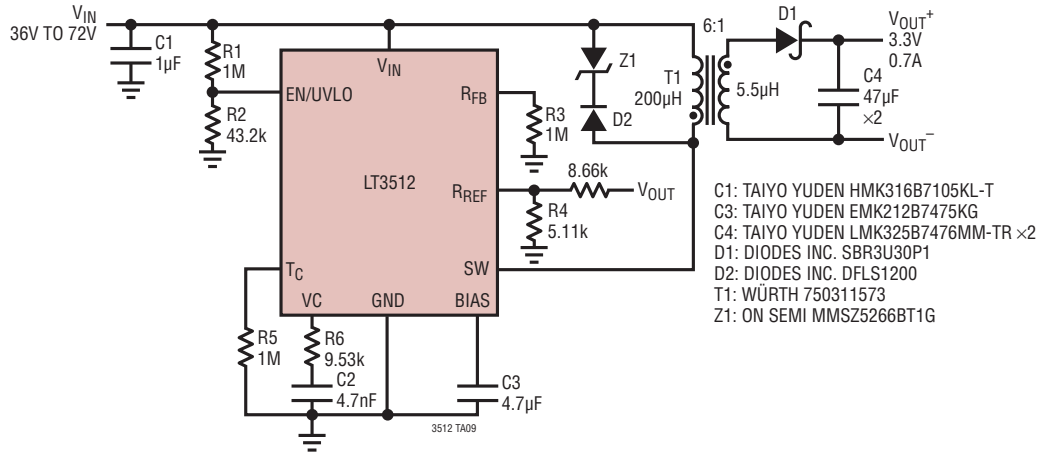


12V to ±70V Isolated Flyback Converter

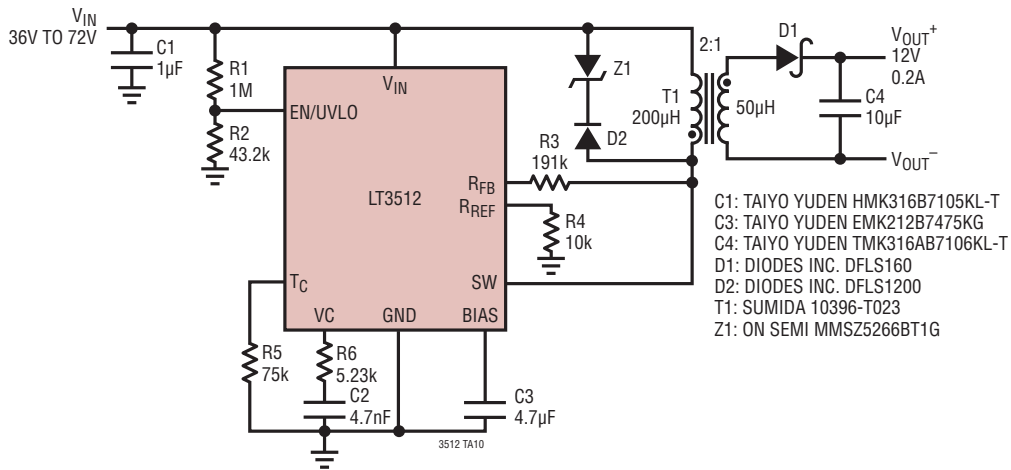


TYPICAL APPLICATIONS

48V to 3.3V Non-Isolated Flyback Converter



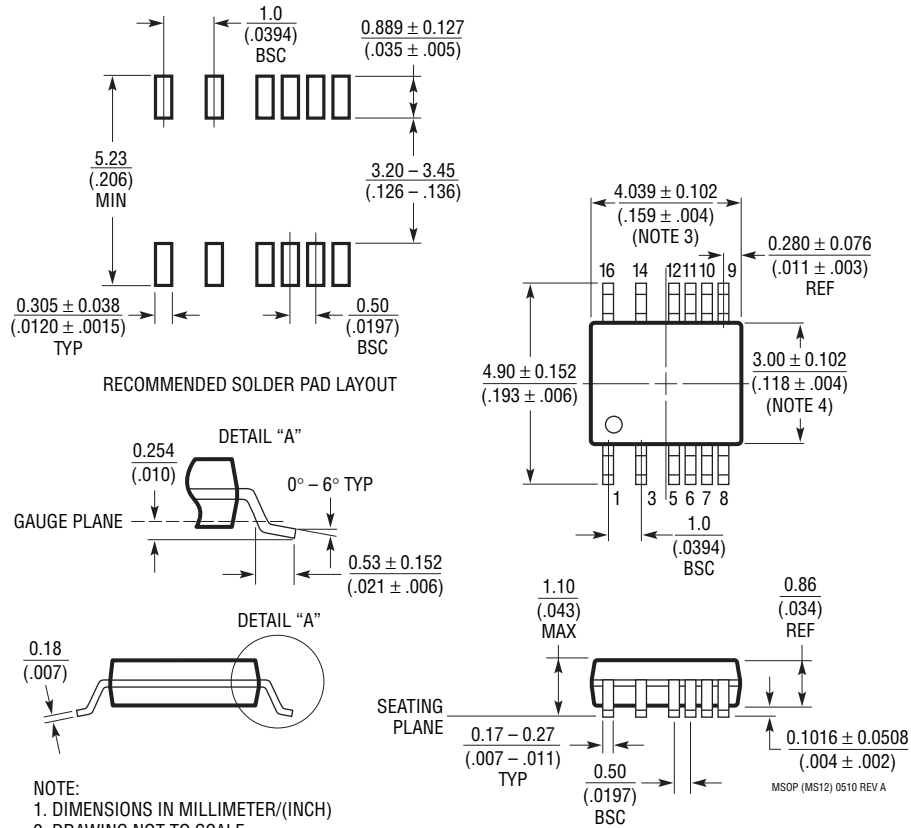
48V to 12V Isolated Flyback Converter



PACKAGE DESCRIPTION

Please refer to <http://www.linear.com/designtools/packaging/> for the most recent package drawings.

MS Package
Variation: MS16 (12)
16-Lead Plastic MSOP with 4 Pins Removed
 (Reference LTC DWG # 05-08-1847 Rev A)



- NOTE:
1. DIMENSIONS IN MILLIMETER/(INCH)
 2. DRAWING NOT TO SCALE
 3. DIMENSION DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS.
MOLD FLASH, PROTRUSIONS OR GATE BURRS SHALL NOT EXCEED 0.152mm (.006") PER SIDE
 4. DIMENSION DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSIONS.
INTERLEAD FLASH OR PROTRUSIONS SHALL NOT EXCEED 0.152mm (.006") PER SIDE
 5. LEAD COPLANARITY (BOTTOM OF LEADS AFTER FORMING) SHALL BE 0.102mm (.004") MAX

REVISION HISTORY

REV	DATE	DESCRIPTION	PAGE NUMBER
A	9/11	Added MP-Grade part. Changes reflected throughout the data sheet.	1 - 26
B	11/11	Revised Absolute Maximum Ratings. Minor corrections to the Typical Applications drawings, TA07 and TA08.	2 22, 23

