LTM8078
40V, 1.4A Dual Step -Down µModule Regulator

DESCRIPTION

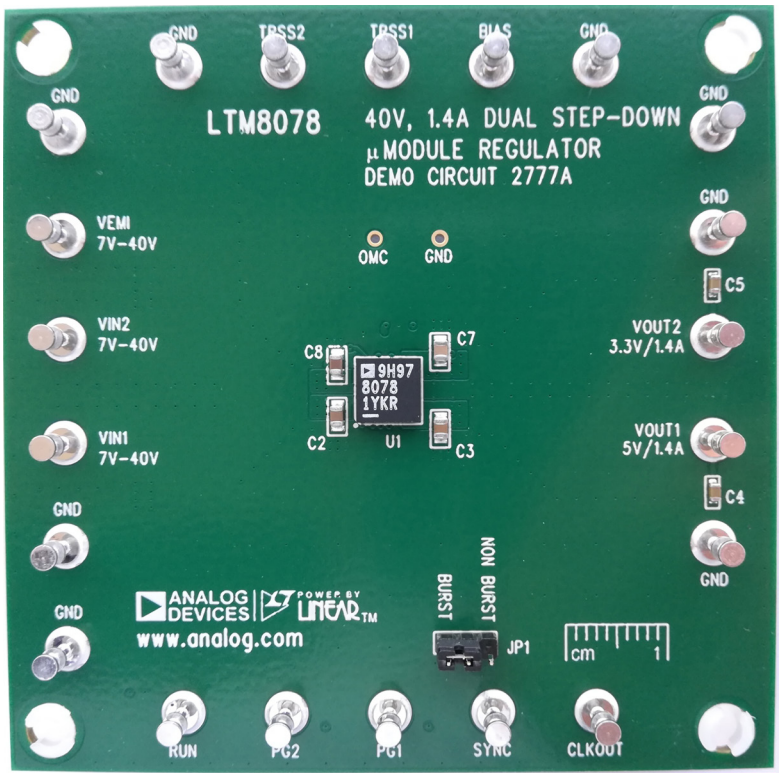
Demonstration circuit 2777A is a dual step-down DC/DC switching converter featuring the LTM®8078 µModule regulator. The demo board is designed to deliver dual 5V/1.4A and 3.3V/1.4A outputs from a 7V to 40V input. The Silent Switcher® architecture minimizes EMI while achieving high efficiency at frequencies up to 3MHz. The modes of operation (Burst Mode® operation or discontinuous mode/SYNC) are jumper selectable. Burst Mode operation improves efficiency at light loads.

The LTM8078 is a fixed frequency PWM regulator with current mode control scheme. The switching frequency is set by an appropriate resistor (R11) from the RT pin to ground. The RUN pin (RUN terminal) can be used to set the LTM8078 in micropower shutdown mode. Output tracking and soft-start pins (TRSS1/TRSS2) allow user control of output voltage ramp rate during start-up. The power good output of each channel (PG1 or PG2 terminal) will be low when that channel's output voltage is outside of the ±7.5% regulation window.

The LTM8078 data sheet gives a complete description of the operation and application information. The data sheet must be read in conjunction with this demo manual

Design files for this circuit board are available.

BOARD PHOTO



PERFORMANCE SUMMARY

Specifications are at T_A = 25°C

PARAMETER	CONDITION	VALUE
Input Voltage Range		7V to 40V
Output Voltage, V_{OUT1}	V_{IN} = 7V to 40V, I_{OUT1} = 0A to 1.4A	5V ±2%
Output Voltage, V_{OUT2}	V_{IN} = 7V to 40V, I_{OUT2} = 0A to 1.4A	3.3V ±2%
Maximum Output Current, I_{OUT1}	V_{IN} = 7V to 40V, V_{OUT1} = 5V	1.4A
Maximum Output Current, I_{OUT2}	V_{IN} = 7V to 40V, V_{OUT2} = 3.3V	1.4A
Typical Switching Frequency		1.6MHz
Typical Efficiency, V_{OUT1} (5V)	V_{IN} = 12V, I_{OUT1} = 1.4A, Burst Mode Operation	91.4%
Typical Efficiency, V_{OUT2} (3.3V)	V_{IN} = 12V, I_{OUT2} = 1.4A, Burst Mode Operation	88.5%

QUICK START PROCEDURE

Demonstration circuit 2777A is easy to set up to evaluate the performance of the LTM8078. Refer to Figure 1 for the proper measurement equipment setup and follow the procedure below:

1. With power off, connect the input power supply to V_{IN1} (7V to 40V) and GND (input return).
2. Connect the 5V output load between V_{OUT1} and GND (Initial load: no load); and connect the 3.3V output load between V_{OUT2} and GND (Initial load: no load).
3. Connect the DVMs to the input and outputs.
4. Turn on the input power supply and check for the proper output voltages. V_{OUT1} should be 5V ±2%; V_{OUT2} should be 3.3V ±2%.
5. Once the proper output voltages are established, adjust the loads within the operating range and observe the output voltage regulation, efficiency and other parameters.

   Note: When measuring the output or input voltage ripple, do not use the long ground lead on the oscilloscope probe. SeeFigure 2 for the proper scope probe technique. Short, stiff leads need to be soldered to the (+) and (–) terminals of an output capacitor. The probe's ground ring needs to touch the (–) lead and the probe tip needs to touch the (+) lead.

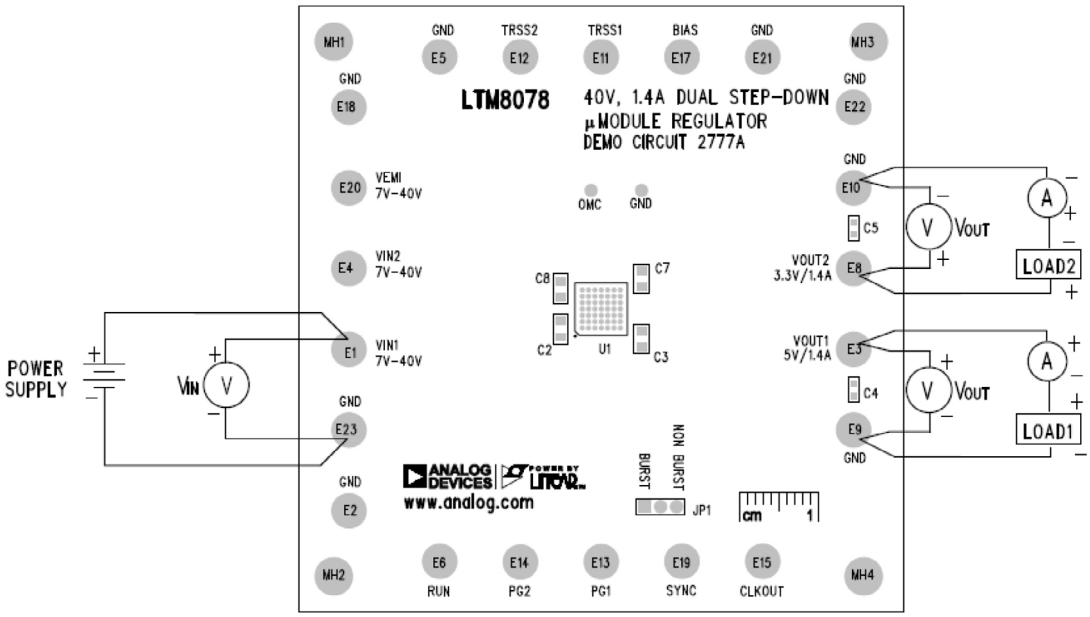


Figure 1. Proper Measurement Equipment Setup

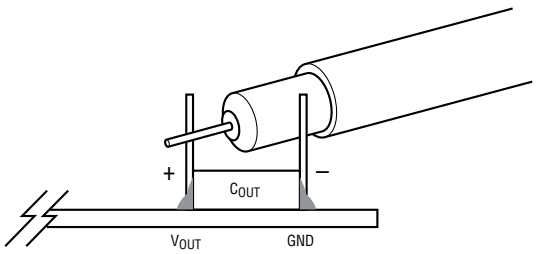


Figure 2. Measuring Output Voltage Ripple

QUICK START PROCEDURE

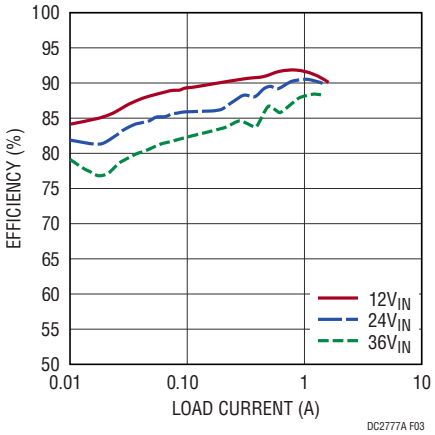


Figure 3. 5V Efficiency vs Load Current (Burst Mode Operation, 1.6MHz, Channel 2 No Load)

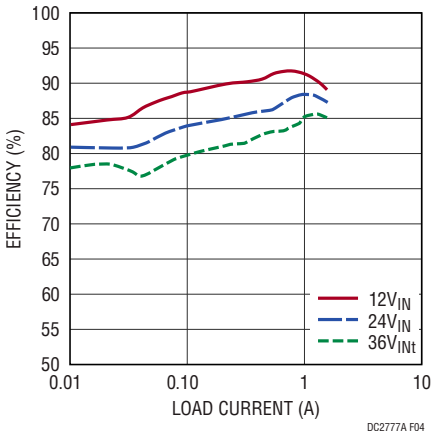


Figure 4. 3.3V Efficiency vs Load Current (Burst Mode Operation, 1.6MHz, Channel 1 No Load)

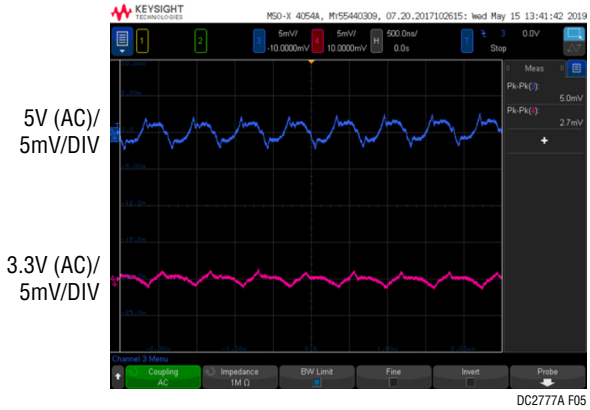


Figure 5. Output Voltage Ripples ($12V_{IN}$, 1.4A Load on Each Output, SYNC Pin Floated)

QUICK START PROCEDURE

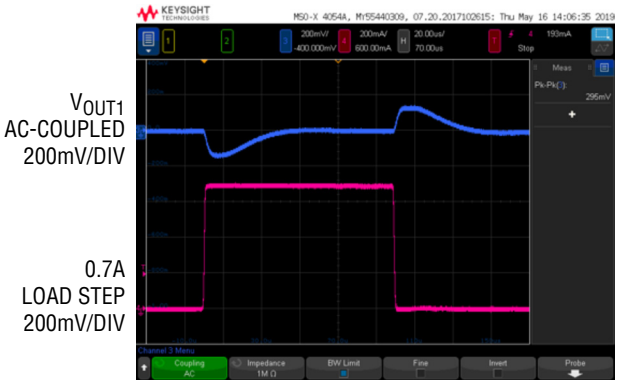


Figure 6. Load Step Transient Test (V_{IN} = 12V, V_{OUT1} = 5V)

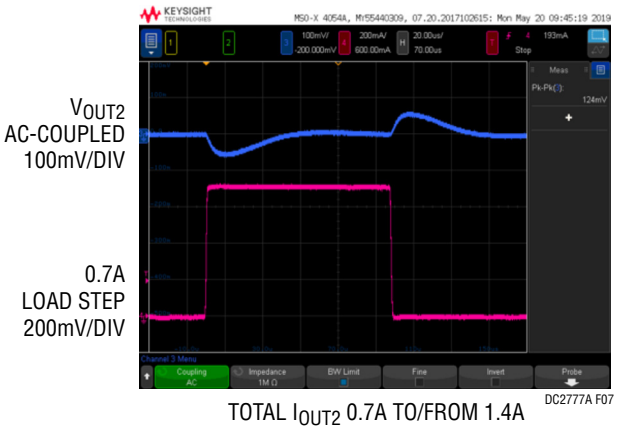


Figure 7. Load step transient test (V_{IN} =12V, V_{OUT2} = 3.3V)

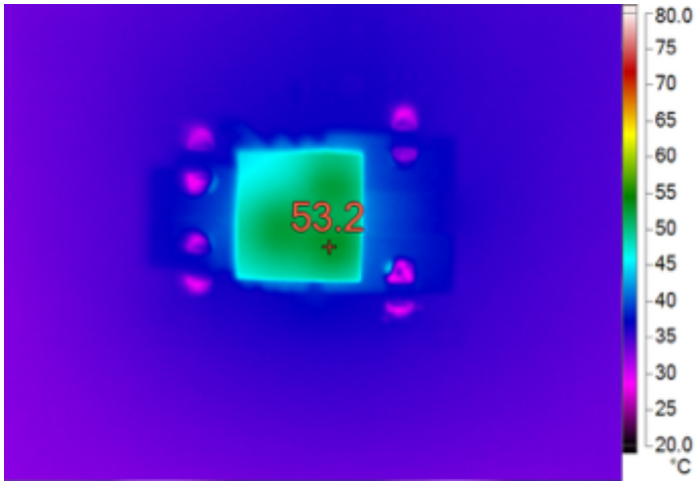
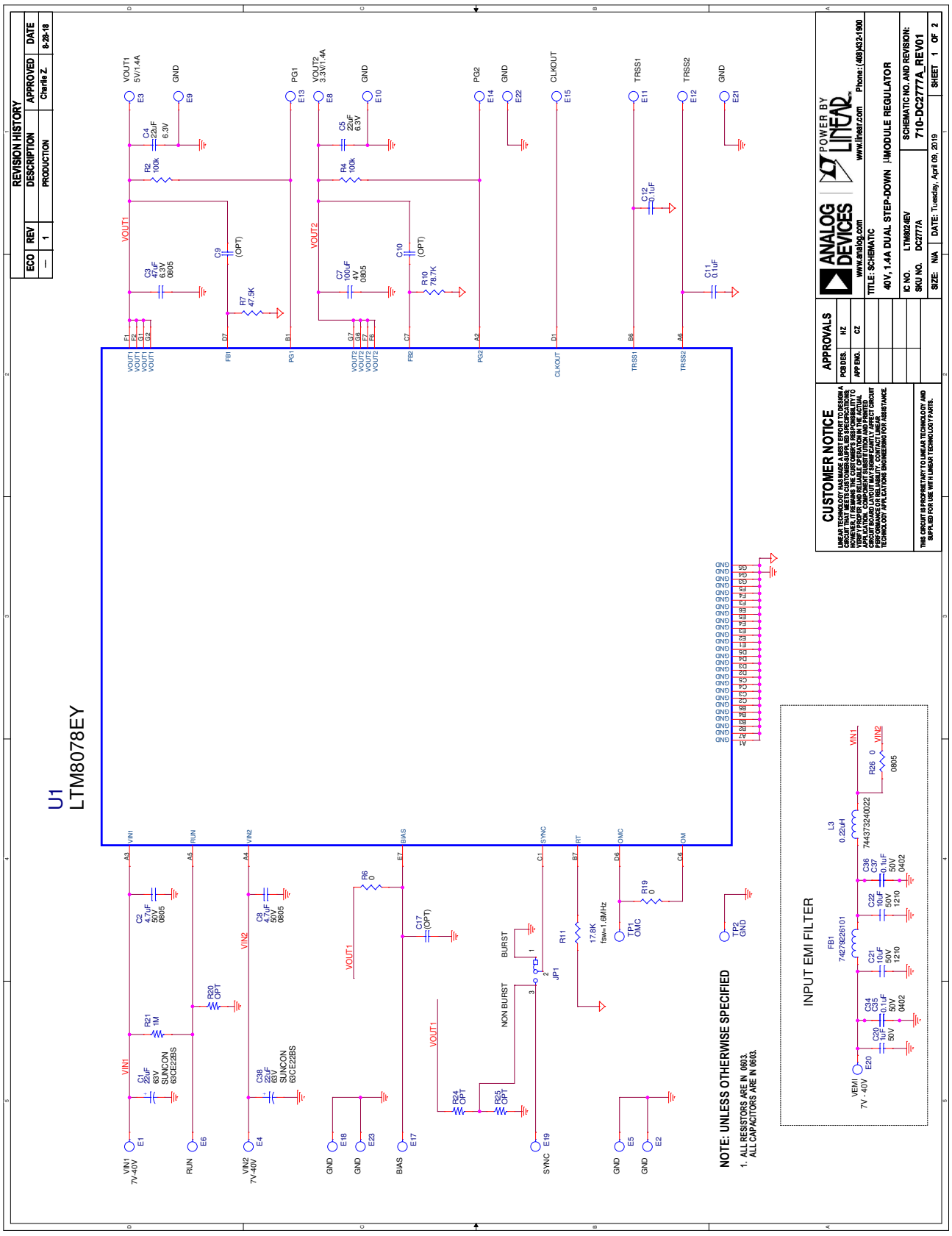


Figure 8. Thermal Picture (V_{IN} = 12V, V_{OUT1} = 5V, V_{OUT2} = 3.3V, 1.4A Load on Each Channel)

PARTS LIST

ITEM	QTY	REFERENCE	PART DESCRIPTION	MANUFACTURER/PART NUMBER
Required Circuit Components				
1	2	C1, C38	CAP., 22µF, ALUM, 63V	SUN ELECT., 63CE22BS
2	2	C2, C8	Cap., 4.7µF X5R 50V 10% 0805	MURATA, GRM21BR61H475KE51L
3	1	C3	Cap., 47µF X5R 6.3V 20% 0805	MURATA, GRM219R60J476ME44D
4	2	C4,C5	Cap., 22µF X5R 6.3V 20% 0603	MURATA, GRM188R60J226MEA0D
5	1	C7	Cap., 100µF X5R 4V 20% 0805	MURATA, GRM21BR60G107ME11L
7	2	C11, C12	CAP., 0.1µF, X5R, 50V, 10%, 0603	MURATA, GRM188R61H104KA93D
8	1	C20	CAP., 1µF, X7R, 50V, 10%, 0603	TAIYO YUDEN, UMK107AB7105KA-T
9	2	C21, C22	CAP., 10µF, X7R, 50V, 10% 1210	MURATA, GRM32ER71H106KA12L
10	4	C34, C35, C36, C37	CAP., 0.1µF, X7R, 50V, 10%, 0402	MURATA, GRM155R71H104KE14D
12	1	FB1	IND., PWR. BEAD, 25% 8000mA 6mΩ 1812	WURTH ELEKTRONIK, 74279226101
14	1	L3	INDUCTOR, 0.22µH	WURTH ELEKTRONIK, 744373240022
15	2	R2, R4	RES., CHIP, 100k, 0.1W ,1%, 0603	VISHAY, CRCW0603100KFKEA
16	2	R6, R19	RES., CHIP, 0Ω, 0.1W, 1%, 0603	VISHAY, CRCW06030000Z0EA
17	1	R7	RES., CHIP, 47.5k, 0.1W,1%, 0603	VISHAY, CRCW060347K5FKEAC
18	1	R10	RES., CHIP, 78.7k, 0.1W, 1%, 0603	VISHAY, CRCW060378K7FKEA
19	1	R11	RES., CHIP, 17.8k, 0.1W, 1%, 0603	PANASONIC, ERJ-3EKF1782V
21	1	R21	RES., CHIP, 1MΩ, 0.1W, 1%, 0603	VISHAY, CRCW06031M00FKEA
22	1	R26	RES., CHIP, 0Ω, 0.1W, 1%, 0805	VISHAY, CRCW08050000Z0EA
24	1	U1	I.C., VOLTAGE REG. BGA	ANALOG DEVICES, LTM8078EY#PBF
Additional Demo Board Circuit Components				
6	0	C9, C10, C17	CAP	OPT
20	0	R20, R24, R25	RES.	OPT
Hardware for Demo Board Only				
11	21	E1-E15, E17-E23	TESTPOINT, TURRET, 0.094" PBF	MILL-MAX, 2501-2-00-80-00-00-07-0
13	2	JP1, JP3	HEADERS, 3 PINS, 2mm CTRS.	WURTH ELEKTRONIK, 62000311121
23	2	XJP1,XJP3	SHUNT, 2mm CTRS.	WURTH ELEKTRONIK, 60800213421
25	4	MH1-MH4	STANDOFF, NYLON, 0.25"	WURTH ELEKTRONIK, 702931000
26	1		FAB, PRINTED CIRCUIT BOARD	DEMO CIRCUIT 2777A
27	2		STENCILS (TOP AND BOTTOM)	STENCIL DC2777A

SCHEMATIC DIAGRAM



ESD Caution

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

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