Mars AX3 FPGA Module

User Manual

Purpose

The purpose of this document is to present the characteristics of Mars AX3 FPGA module to the user, and to provide the user with a comprehensive guide to understanding and using the Mars AX3 FPGA module.

Summary

This document first gives an overview of the Mars AX3 FPGA module followed by a detailed description of its features and configuration options. In addition, references to other useful documents are included.

Product Information	Code	Name
Product	MA-AX3	Mars AX3 FPGA Module

Document Information	Reference	Version	Date
Reference / Version / Date	D-0000-426-004	06	16.02.2021

Approval Information	Name	Position	Date
Written by	DIUN	Design Engineer	05.08.2016
Verified by	GLAC	Design Expert	29.08.2016
Approved by	DIUN	Manager, BU SP	16.02.2021

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Document History

Version	Date	Author	Comment
06	16.02.2021	DIUN	Cleaned-up product variants, added information on FPGA fuses and warranty, on differential I/Os, on voltage monitoring outputs, other style updates
05	25.07.2019	DIUN	Added information on voltage monitoring, power supplies, heat sink, other style updates
04	21.08.2018	DIUN	Minor corrections and style updates
03	04.05.2017	DIUN	Updated EEPROM map, block diagram and footprint information
02	27.12.2016	DIUN	Added tool support information
01	09.12.2016	DIUN	Version 01

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1 Overview

1.1 General

1.1.1 Introduction

The Mars AX3 FPGA module combines the Xilinx Artix-7® All Programmable FPGA device with fast DDR3 SDRAM, quad SPI flash, Gigabit Ethernet, high-speed LVDS I/O, and is available in industrial temperature range, forming a complete and powerful embedded processing system. It is ideal for high-speed communication and DSP applications, offering high-performance and low cost.

The SO-DIMM form factor allows space-saving hardware designs and quick and simple integration of the module into the target application.

The use of the Mars AX3 FPGA module, in contrast to building a custom FPGA hardware, significantly reduces development effort and redesign risk and improves time-to-market for the embedded system.

Together with Mars base boards, the Mars AX3 FPGA module allows the user to quickly build a system prototype and start with application development.

1.1.2 Warranty

Please refer to the General Business Conditions, available on the Enclustra website [1].

Warning!

Please note that the warranty of an Enclustra module is voided if the FPGA fuses are blown. This operation is done at own risk, as it is irreversible. Enclustra cannot test the module in case of a warranty product return.

1.1.3 RoHS

The Mars AX3 FPGA module is designed and produced according to the Restriction of Hazardous Substances (RoHS) Directive (2011/65/EC).

1.1.4 Disposal and WEEE

The Mars AX3 FPGA module must be properly disposed of at the end of its life.

The Waste Electrical and Electronic Equipment (WEEE) Directive (2002/96/EC) is not applicable for the Mars AX3 FPGA module.

1.1.5 Safety Recommendations and Warnings

Mars modules are not designed to be "ready for operation" for the end-user. These can only be used in combination with suitable base boards. Proper configuration of the hardware before usage is required.

Ensure that the power supply is disconnected from the board before inserting or removing the Mars AX3 FPGA module, connecting interfaces, or connecting jumpers.

Touching the capacitors of the DC-DC converters can lead to voltage peaks and permanent damage; overvoltage on power or signal lines can also cause permanent damage to the module.

Warning!

Use the Mars AX3 FPGA module only with base boards designed for the Enclustra Mars module family. Inserting the Mars AX3 FPGA module into a SO-DIMM connector designed for memory (e.g. a computer main board) may damage the module and the carrier board.

1.1.6 Electrostatic Discharge

Electronic boards are sensitive to electrostatic discharge (ESD). Please ensure that the product is handled with care and only in an ESD-protected environment.

1.1.7 Electromagnetic Compatibility

The Mars AX3 FPGA module is a Class A product (as defined in IEC 61000-3-2 standard) and is not intended for use in domestic environments. The product may cause electromagnetic interference, for which appropriate measures must be taken.

1.2 Features

- Xilinx Artix-7 28 nm FPGA, CSG324 package
- 108 user I/Os (single-ended, differential or analog) up to 3.3 V
- 256 MB DDR3 SDRAM
- 64 MB quad SPI flash
- Gigabit Ethernet
- 50 MHz oscillator
- Real-time clock (optional)
- SO-DIMM form factor (30 × 67.6 mm, 200 pins)
- The module can be operated using a single 3.3 V supply voltage

1.3 Deliverables

- Mars AX3 FPGA module
- Mars AX3 FPGA module documentation, available via download:
  - Mars AX3 FPGA Module User Manual (this document)
  - Mars AX3 FPGA Module Reference Design [2]
  - Mars AX3 FPGA Module IO Net Length Excel Sheet [3]
  - Mars AX3 FPGA Module FPGA Pinout Excel Sheet [4]
  - Mars AX3 FPGA Module User Schematics (PDF) [5]
  - Mars AX3 FPGA Module Known Issues and Changes [6]
  - Mars AX3 FPGA Module Footprint (Altium, Eagle, Orcad and PADS) [7]
  - Mars AX3 FPGA Module 3D Model (PDF) [8]
  - Mars AX3 FPGA Module STEP 3D Model [9]
  - Mercury Mars Module Pin Connection Guidelines [10]
  - Mars Master Pinout [11]
  - Mars Heatsink Mounting Guide [16]

1.4 Accessories

1.4.1 Reference Design

The Mars AX3 FPGA module reference design features an example configuration for the Artix-7 FPGA device, together with an example top level HDL file for the user logic.

A number of software applications are available for the reference design, that show how to initialize the peripheral controllers and how to access the external devices. Pre-compiled binaries are included in the archive, so that the user can easily check that the hardware is functional.

The reference design can be downloaded from Github: `https://github.com/enclustra`.

1.4.2 Enclustra Heat Sink

For Mars modules an Enclustra heat sink is available for purchase along with the product. Please refer to section 2.10.6 for further information on the available cooling options.

1.4.3 Mars ST3 Base Board

- Mars 200-pin SO-DIMM socket
- MIPI D-PHY connector (requires FPGA support)
- Mini DisplayPort connector (requires FPGA support)
- HDMI connector (requires FPGA support)
- USB 3.0 host connector
- RJ45 Ethernet connector
- 2 × 40-pin GPIO connector (Anios)
- 1 × 8-pin and 1 × 4-pin GPIO connectors (Pmod™ compatible pinout)
- FTDI USB 2.0 device controller with micro USB device connector
- microSD card holder
- User LEDs
- Integrated Xilinx compatible JTAG adapter
- Support for low I/O voltages (1.2 V, 1.8 V)
- Single 12 V DC supply voltage
- Form factor: 100 × 80 mm

Please note that the available features depend on the equipped Mars module type.

1.4.4 Mars EB1 Base Board

- Mars 200-pin SO-DIMM socket
- 2 × Mini Camera Link connectors (requires FPGA support)
- HDMI 1.3 connector (requires FPGA support)
- 40-pin GPIO connector (Anios)
- 3 × 12-pin GPIO connector (two of the connectors with Pmod™ compatible pinout)
- RJ45 Ethernet connector
- USB 2.0 A host connector
- Micro USB 2.0 device connector (shared)
- FTDI USB 2.0 device controller with micro USB device connector
- microSD card holder
- Various switches and LEDs
- Integrated Xilinx compatible JTAG adapter
- Single 12 V DC supply voltage or USB bus-powered (with restrictions)
- Form factor: 120 × 80 mm

Please note that the available features depend on the equipped Mars module type.

1.4.5 Mars PM3 Base Board

- Mars 200-pin SO-DIMM socket
- FMC LPC (Low Pin Count) connector (72 I/Os)
- 40-pin GPIO connector (optional, shared with FMC I/Os)
- RJ45 Gigabit Ethernet connector
- Mini HDMI connector for PCIe and LVDS applications (module dependent)
- Cypress FX3 USB 3.0 device controller (16-bit Slave-FIFO interface or 32-bit Slave-FIFO interface shared with FMC I/Os)
- USB 3.0 B device connector
- USB 2.0 A host connector
- Micro USB 2.0 B device connector with FTDI USB device controller
- Battery holder for the real-time clock
- microSD card holder
- Fan connector, various switches and LEDs
- Single 12 V DC supply voltage or USB bus-powered (with restrictions)
- Form factor: 100 $\times$ 72 mm (pico-ITX)

Please note that the available features depend on the equipped Mars module type.

1.5 Xilinx Tool Support

The FPGA devices equipped on the Mars AX3 FPGA module are supported by the Vivado HL WebPACK Edition software, which is available free of charge. Please contact Xilinx for further information.

2 Module Description

2.1 Block Diagram

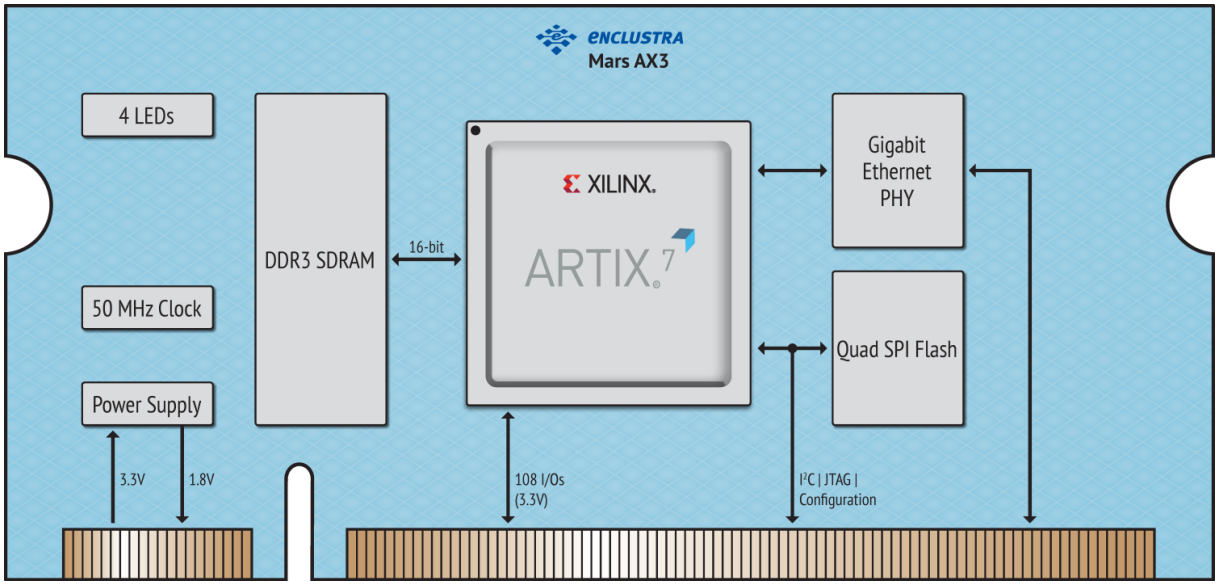

Figure 1: Hardware Block Diagram

The main component of the Mars AX3 FPGA module is the Xilinx Artix-7 FPGA device. Most of its I/O pins are connected to the Mars module connector, making 108 user I/Os available to the user. With some hardware changes, four additional FPGA pins can be routed to the module connector, in case the application requires 112 user I/Os and a custom base board is used.

The FPGA device can be configured with a bitstream residing in the on-board QSPI flash, via an external microcontroller or another SPI master device or via the JTAG interface connected to Mars module connector.

The available standard configurations include 256 MB DDR3 SDRAM and 64 MB quad SPI flash.

Further, the module is equipped with a Gigabit Ethernet PHY, making it ideal for communication applications.

On-board clock generation is based on a 50 MHz crystal oscillator.

The module can be operated using a single input supply of 3.3 V DC. All other necessary supply voltages are generated on-board. Some of these voltages are available on the Mars module connector to supply circuits on the base board.

A real-time clock may be optionally equipped on the module and connected to the global I2C bus.

Four LEDs are connected to the FPGA pins for status signaling.

2.2 Module Configuration and Product Codes

Table 1 describes the available standard module configurations. Custom configurations are available; please contact Enclustra for further information.

Product Code	FPGA	DDR3/DDR3L SDRAM	Temperature Range
MA-AX3-35-1I-D8	XC7A35T-1CSG324I	256 MB	-40 to +85° C
MA-AX3-50-1I-D8	XC7A50T-1CSG324I	256 MB	-40 to +85° C
MA-AX3-100-2I-D8	XC7A100T-2CSG324I	256 MB	-40 to +85° C

Table 1: Standard Module Configurations

The product code indicates the module type and main features. Figure 2 describes the fields within the product code.

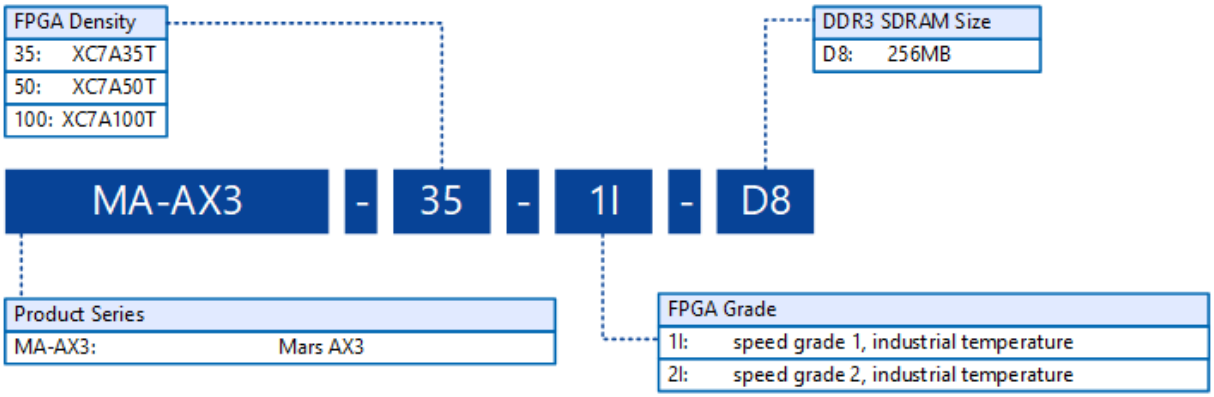

Figure 2: Product Code Fields

Please note that for the first revision modules or early access modules, the product code may not respect entirely this naming convention. Please contact Enclustra for details on this aspect.

2.3 Article Numbers and Article Codes

Every module is uniquely labeled, showing the article number and serial number. An example is presented in Figure 3.

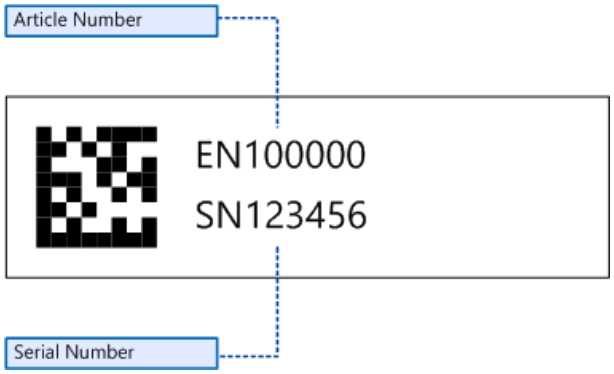

Figure 3: Module Label

The correspondence between article number and article code is shown in Table 2. The article code represents the product code, followed by the revision; the R suffix and number represent the revision number.

The revision changes and product known issues are described in the Mars AX3 FPGA Module Known Issues and Changes document [6].

Article Number	Article Code
EN100030	MA-AX3-100-2I-D8-R1
EN100081	MA-AX3-100-1C-D8-R1
EN100587	MA-AX3-100-1C-D8-R1
EN100655	MA-AX3-35-1I-D8-R2
EN100656	MA-AX3-50-1C-D8-R2
EN100657	MA-AX3-50-1I-D8-R2
EN100722	MA-AX3-100-1C-D8-R2
EN100723	MA-AX3-100-2I-D8-R2
EN100908	MA-AX3-35-1C-D8-R2
EN100909	MA-AX3-50-1C-D8-R2
EN101294	MA-AX3-35-1C-D8-R3
EN101295	MA-AX3-35-1I-D8-R3
EN101296	MA-AX3-50-1C-D8-R3
EN101297	MA-AX3-50-1I-D8-R3
EN101298	MA-AX3-100-1C-D8-R3
EN101299	MA-AX3-100-2I-D8-R3

Table 2: Article Numbers and Article Codes

2.4 Top and Bottom Views

2.4.1 Top View

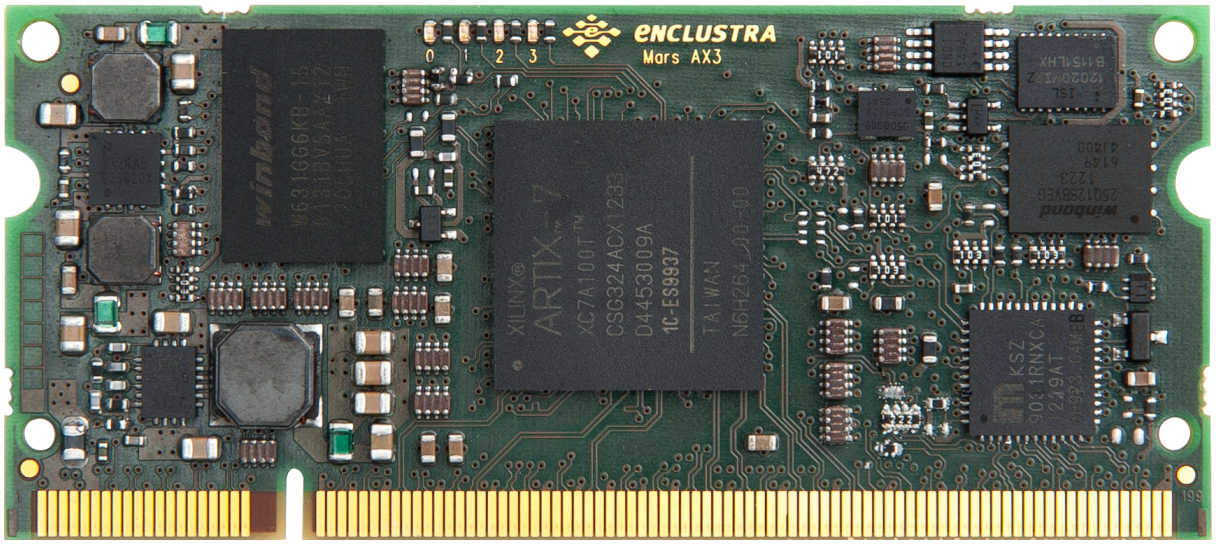

Figure 4: Module Top View

2.4.2 Bottom View

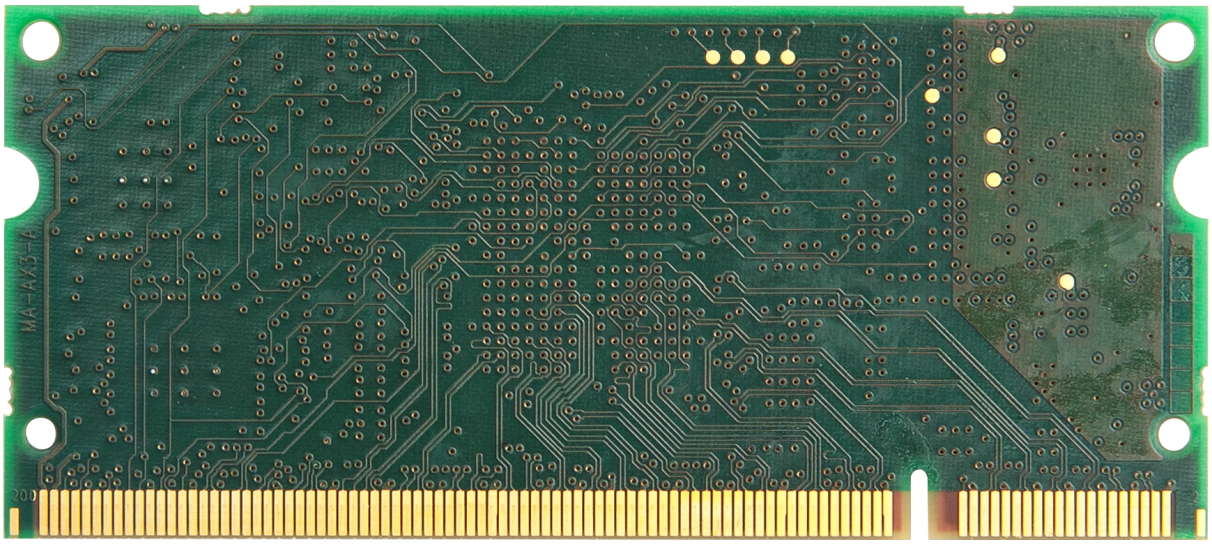

Figure 5: Module Bottom View

Please note that depending on the hardware revision and configuration, the module may look slightly different than shown in this document.

2.5 Top and Bottom Assembly Drawings

2.5.1 Top Assembly Drawing

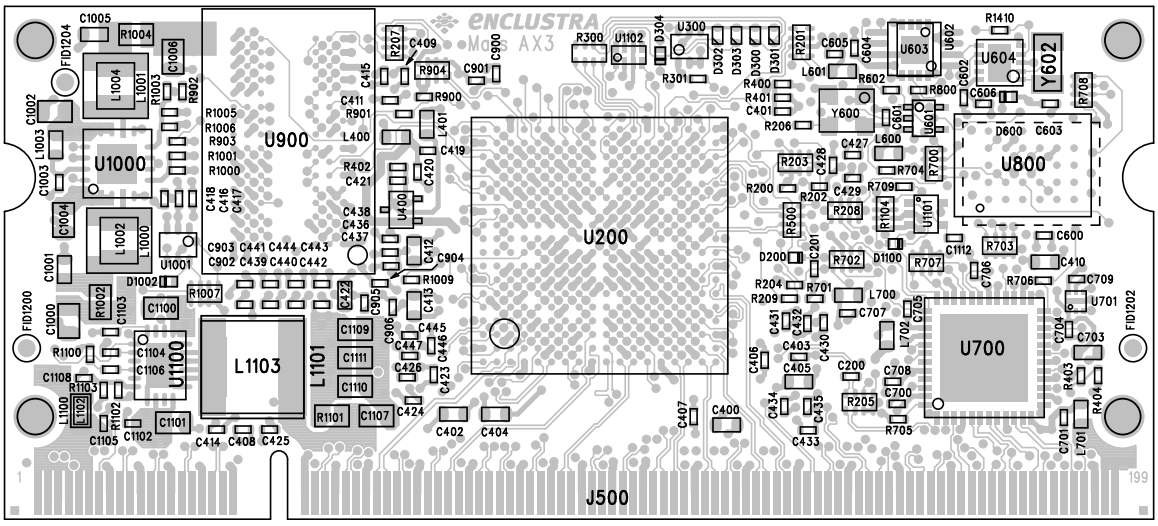

Figure 6: Module Top Assembly Drawing

2.5.2 Bottom Assembly Drawing

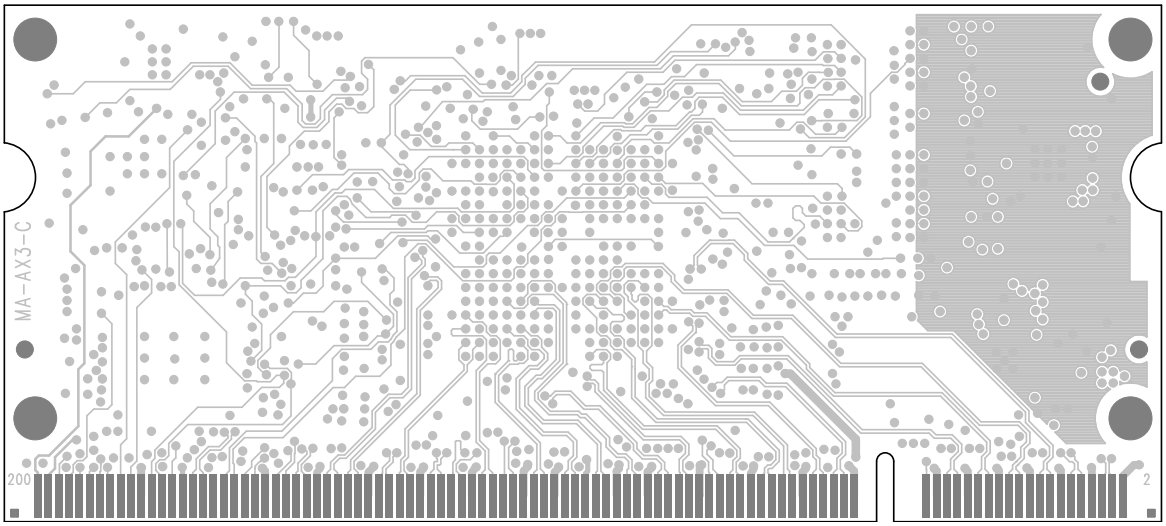

Figure 7: Module Bottom Assembly Drawing

Please note that depending on the hardware revision and configuration, the module may look slightly different than shown in this document.

2.6 Module Footprint

Figure 8 shows the dimensions of the module footprint on the base board.

The maximum component height under the module is dependent on the connector type - refer to Section 2.8 for detailed connector information.

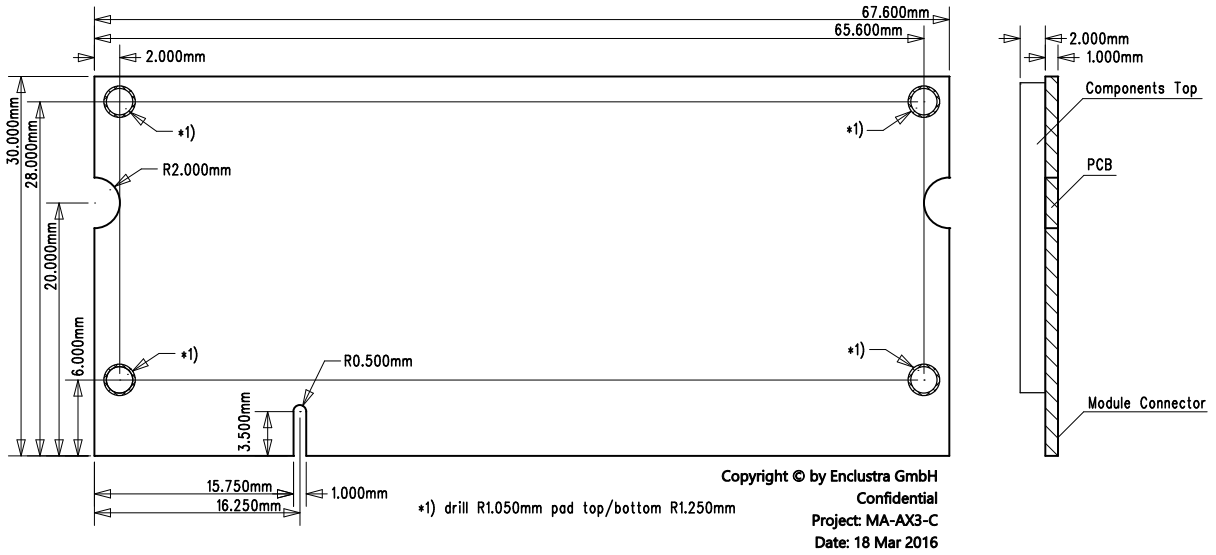

Figure 8: Module Footprint - Top View

The footprint of the module connector is available for different PCB design tools (Altium, Eagle, Orcad, PADS) [7].

2.7 Mechanical Data

Table 3 describes the mechanical characteristics of the Mars AX3 FPGA module. A 3D model (PDF) and a STEP 3D model are available [8], [9].

Symbol	Value
Size	67.6 × 30 mm
Component height top	2.0 mm
Component height bottom	0 mm
Weight	8 g

Table 3: Mechanical Data

2.8 Module Connector

The Mars AX3 FPGA module fits into a 200-pin DDR2 SO-DIMM (1.8 V) socket. Up to four M2 screws may be used to mechanically fasten the module to the base board. Do not use excessive force to tighten the screws, as this could damage the module.

The pinout of the module connector is found in the Mars Master Pinout Excel Sheet [11]. The connector to be mounted on the base board is available in different heights. Some examples are presented in Table 4. Please refer to the connector datasheet for more information.

Height	Type	Description	Max component height under the module
4.0 mm	TE 292406-4	DDR2-SODIMM, 1.8 V	1 mm
5.2 mm	TE 1565917-4	DDR2-SODIMM, 1.8 V	2 mm
6.5 mm	TE 5-1746530-4	DDR2-SODIMM, 1.8 V	3 mm
8.0 mm	TE 1827341-4	DDR2-SODIMM, 1.8 V	5 mm

Table 4: Module Connector Types

2.9 User I/O

2.9.1 Pinout

Information on the Mars AX3 FPGA module pinout can be found in the Enclustra Mars Master Pinout [11], and in the additional document Enclustra Module Pin Connection Guidelines [10].

Warning!

Please note that the pin types on the schematics symbol of the module connector and in the Master Pinout document are for reference only. On the Mars AX3 FPGA module it may be possible that the connected pins do not have the targeted functions (such as primary clocks, differential pins, MGT signals, etc).

The naming convention for the user I/Os is:
IO_B<BANK>_L<PAIR><_SPECIAL_FUNCTION>_<PACKAGE_PIN>_<POLARITY>.

For example, IO_B35_L1_AD4_C6_P is located on pin C6 of I/O bank 35, pair 1, it is an XADC auxiliary analog input capable pin and it has positive polarity, when used in a differential pair.

The multi-region clock capable pins are marked with "MRCC", while the single region clock capable pins are marked with "SRCC" in the signal name. For details on their function and usage, please refer to the Xilinx documentation.

Table 5 includes information related to the total number of I/Os available in each I/O bank and possible limitations.

Signal Name	Signals	Pairs	Differential	Single-ended	I/O Bank
IO_B14_<...>	12	6	In/Out	In/Out	14
IO_B34_<...>	48	24	In/Out	In/Out	34
IO_B35_<...>	48	24	In/Out	In/Out	35
Total	**108**	**54**	-	-	-

Table 5: User I/Os

Please note that for the 7 Series FPGAs there are restrictions on the VCCO voltage when using LVDS I/Os; refer to Xilinx AR# 43989 for details.

2.9.2 Differential I/Os

When using differential pairs, a differential impedance of 100 Ω must be matched on the base board, and the two nets of a differential pair must have the same length.

The information regarding the length of the signal lines from the FPGA device to the module connector is available in Mars AX3 FPGA Module IO Net Length Excel Sheet [3]. This enables the user to match the total length of the differential pairs on the base board if required by the application.

Warning!

Please note that the trace length of various signals may change between revisions of the Mars AX3 FPGA module. Please use the information provided in the Mars AX3 FPGA Module IO Net Length Excel Sheet [3] to check which signals are affected. The differential signals will still be routed differentially in subsequent product revisions.

2.9.3 I/O Banks

Table 6 describes the main attributes of the FPGA I/O banks, and indicates which peripherals are connected to each I/O bank. All I/O pins within a particular I/O bank must use the same I/O (VCC_IO) and reference (VREF) voltages.

Bank	Connectivity	VCC_IO	VREF
Bank 0	Configuration (JTAG, QSPI)	User selectable VCC_CFG_B14	-
Bank 14	Ethernet PHY, QSPI flash, I2C, LEDs, module connector	User selectable VCC_CFG_B14	-
Bank 34	Module connector	User selectable VCC_IO_B34	IO_B34_L6_VREF_L5_N IO_B34_L19_VREF_R5_N
Bank 35	Module connector	User selectable VCC_IO_B35	IO_B35_L6_VREF_D7_N IO_B35_L19_VREF_F6_N
Bank 15	DDR3 SDRAM	User selectable[1] VCC_DDR3	0.5 × VREF_DDR3
Bank 16	DDR3_VSEL	User selectable VCC_CFG_B14	-

Table 6: I/O Banks

[1]The DDR3 SDRAM supports voltages of 1.5 or 1.35 V. Please refer to Section 2.14 for details.

2.9.4 VREF Usage

I/O standards referenced using VREF can be used on the Mars module connector. The reference voltage has to be applied to all VREF pins of the respective I/O banks. If a bank is configured to use an I/O standard that does not need a reference voltage, the VREF pins of this bank on the module connector are available as user I/O pins.

The VREF pins are listed in the Mars Master Pinout Excel Sheet [11].

Warning!

Use only VREF voltages compliant with the equipped FPGA device; any other voltages may damage the equipped FPGA device, as well as other devices on the Mars AX3 FPGA module.

Do not leave a VREF pin floating when the used I/O standard requires a reference voltage, as this may damage the equipped FPGA device, as well as other devices on the Mars AX3 FPGA module.

2.9.5 VCC_IO Usage

The VCC_IO voltages for the I/O banks located on the module connector are configurable by applying the required voltage to the VCC_IO_B[x], respectively VCC_CFG_[x] pins. All VCC_IO_B[x] or VCC_CFG_[x] pins of the same bank must be connected to the same voltage.

For compatibility with other Enclustra Mars base boards and modules, it is recommended to use a single I/O voltage.

Signal Name	FPGA Pins	Supported Voltages	Connector Pins
VCC_CFG_B14	VCCO_0, VCCO_14, VCCO_16	1.8 V[2], 2.5 V - 3.3 V ±5%	137, 146
VCC_IO_B34	VCCO_34	1.2 V - 3.3 V ±5%	82, 117, 126
VCC_IO_B35	VCCO_35	1.2 V - 3.3 V ±5%	53, 62, 73

Table 7: VCC_IO Pins

Note that the CFGBVS_0 pin is set automatically to GND (if VCC_CFG_B14 is less than or equal to 1.8 V) or to VCCO (if VCC_CFG_B14 is 2.5 V or 3.3 V).

Warning!

Use only VCC_IO voltages compliant with the equipped FPGA device; any other voltages may damage the equipped FPGA device, as well as other devices on the Mars AX3 FPGA module.

Do not leave a VCC_IO pin floating, as this may damage the equipped FPGA device, as well as other devices on the Mars AX3 FPGA module.

[2] 1.8 V support is only available for modules of revision 3 and newer.

Warning!

Do not power the VCC_IO pins when PWR_GOOD and PWR_EN signals are not active. If the module is not powered, you need to make sure that the VCC_IO voltages are disabled (for example, by using a switch on the base board, which uses PWR_GOOD as enable signal). Figure 9 illustrates the VCC_IO power requirements.

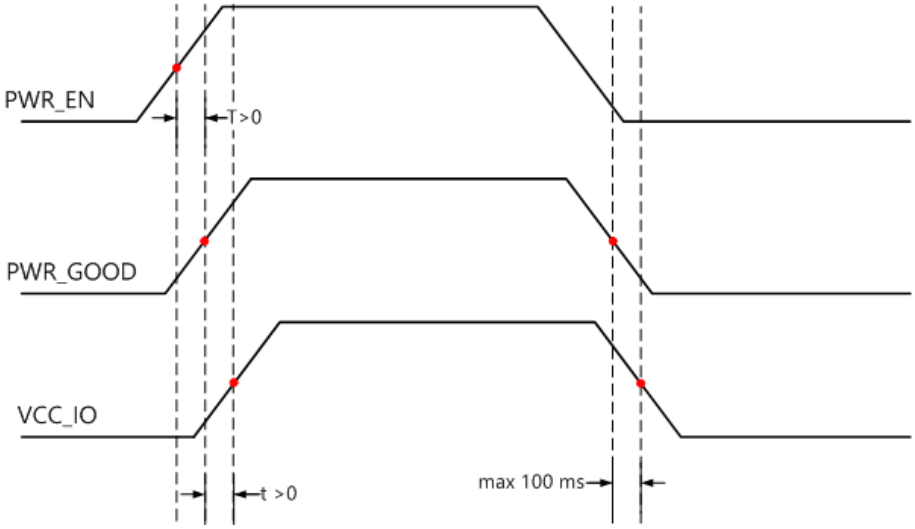

Figure 9: Power-Up Sequence - VCC_IO in Relation with PWR_GOOD and PWR_EN Signals

2.9.6 Signal Terminations

Differential Inputs

There are no external differential termination resistors on the Mars AX3 FPGA module for differential inputs. Differential input pairs on the module connector may be terminated either by external termination resistors on the base board (close to the module pins), or by the FPGA device's internal termination resistors.

Internal differential termination is available only for certain VCCO voltages; please refer to Xilinx AR# 43989 for details.

Single-Ended Outputs

There are no series termination resistors on the Mars AX3 FPGA module for single-ended outputs. If required, series termination resistors may be equipped on the base board (close to the module pins).

2.9.7 Analog Inputs

The Artix-7 FPGA devices provide a dual 12-bit ADC. Eight of the auxiliary analog lines of the FPGA device are connected to the module connector; these I/Os have the abbreviation "AD" followed by the ADC channel in the signal name.

The two dedicated ADC pins VP and VN are available on the module connector on pins 168 and 170 (FPGA_V_P/N). The ADC can also be used for internal voltage and temperature monitoring. For detailed information, refer to the Xilinx 7 Series XADC User Guide [17].

The ADC lines are always used differentially; for single-ended applications, the *_N line must be connected to GND.

Table 8 presents the ADC Parameters.

Parameter	Value
VCC_ADC	1.8 V
GND_ADC	0 V (connected to GND via ferrite)
VREF_ADC	Internal (optionally an external 1.25 V reference circuit can be mounted)
ADC Range	0-1 V
Sampling Rate per ADC	1 MSPS
Total number of channels available on the module connector	9 (1 dedicated channel, 8 auxiliary inputs)

Table 8: ADC Parameters

2.10 Power

2.10.1 Power Generation Overview

The Mars AX3 FPGA module uses a 3.3 - 5.0 V DC power input for generating the on-board supply voltages (1.0 V, 1.35 V/1.5 V, 1.8 V). These internally-generated voltages are accessible on the module connector. In addition, a separate 3.3 V power input is used to supply peripherals, such as the Ethernet PHY, QSPI flash, oscillator, RTC (optional), EEPROM and LEDs.

The Mars AX3 FPGA module can be powered using a single power supply. In this case, the two voltage supply inputs VCC_MOD and VCC_3V3 must be connected together to a 3.3 V supply. Please refer to Section 2.10.3 for details on the voltage supply inputs.

Table 9 describes the power supplies generated on the module.

Voltage Supply Name	Voltage Value	Rated Current	Voltage Source	Shut down via PWR_EN	Influences PWR_GOOD
VCC_1V0	1.0 V	4 A	VCC_MOD	Yes	Yes
VCC_DDR3	1.35 V/1.5 V	2 A	VCC_MOD	Yes	Yes
VCC_1V8	1.8 V	2 A	VCC_MOD	Yes	Yes

Table 9: Generated Power Supplies

Please refer to the Enclustra Module Pin Connection Guidelines for general rules on the power pins [10].

2.10.2 Power Enable/Power Good

The Mars AX3 FPGA module provides a power enable input on the module connector. This input may be used to shut down the DC/DC converters for 1.0 V, 1.35 V/1.5 V and 1.8 V, leaving the FPGA device and the DDR3 SDRAM unpowered.

The PWR_EN input is pulled to VCC_3V3 on the Mars AX3 FPGA module with a 10 kΩ resistor. The PWR_GOOD signal is pulled to VCC_3V3 on the Mars AX3 FPGA module with a 10 kΩ resistor.

PWR_GOOD is an open collector signal and must not be used to drive a load directly. This signal is pulled to GND if the on-board regulators fail or if the module is disabled via PWR_EN. The list of regulators that influence the state of PWR_GOOD signal is provided in Section 2.10.1.

The PWR_GOOD signal is also connected to an FPGA pin via a 47 kΩ resistor.

Pin Name	Module Connector Pin	Remarks
PWR_EN	13	Floating/3.3 V: Module power enabled Driven low: Module power disabled
PWR_GOOD	40	0 V: Module supply not ok 3.3 V: Module supply ok

Table 10: Module Power Status and Control Pins

Warning!

Do not apply any other voltages to the PWR_EN pin than 3.3 V or GND, as this may damage the Mars AX3 FPGA module. PWR_EN pin can be left unconnected.

Do not power the VCC_IO pins when PWR_EN is driven low to disable the module. In this case, VCC_IO needs to be switched off in the manner indicated in Figure 9.

2.10.3 Voltage Supply Inputs

Table 11 describes the power supply inputs on the Mars AX3 FPGA module. The VCC voltages used as supplies for the I/O banks are described in Section 2.9.5.

Pin Name	Module Connector Pins	Voltage	Description
VCC_MOD	1, 3, 5, 7, 9, 11	3.3 - 5.0 V ±10%	Supply for the 1.0 V, 1.35 V/1.5 V and 1.8 V voltage regulators. The input current is rated at 1.8 A (0.3 A per connector pin).
VCC_3V3	197, 199	3.3 V ±5%	Supply for Ethernet PHY, QSPI flash, oscillator, RTC (optional), EEPROM and LEDs
VCC_BAT	200	2.0 - 3.6 V	Battery voltage for the RTC and FPGA encryption key storage

Table 11: Voltage Supply Inputs

2.10.4 Voltage Supply Outputs

Table 12 presents the supply voltages generated on the Mars AX3 FPGA module, that are available on the module connector.

Pin Name	Module Connector Pins	Voltage	Maximum Current[3]
VCC_1V0	42	1.0 V ±5%	0.3 A
VCC_DDR3	41	1.35 V/1.5 V ±5%	0.3 A
VCC_1V8	89, 94, 101, 106	1.8 V ±5%	1 A (and max 0.3 A per connector pin)

Table 12: Voltage Supply Outputs

The voltage supply for the DDR3 SDRAM can be set to 1.35 V for low power operation - for details, please refer to Section 2.14.5.

Warning!

Do not connect any power supply to the voltage supply outputs nor short circuit them to GND, as this may damage the Mars AX3 FPGA module.

2.10.5 Power Consumption

Please note that the power consumption of any FPGA device strongly depends on the application (on the configured bitstream and I/O activity).

To estimate the power consumption of your design, please use the Xilinx Power Estimator available on the Xilinx website.

[3] The maximum available output current depends on your FPGA design. See sections 2.10.1 and 2.10.5 for details.

2.10.6 Heat Dissipation

High performance devices like the Xilinx Artix-7 FPGA need cooling in most applications; always make sure the FPGA is adequately cooled.

For Mars modules an Enclustra heat sink is available for purchase along with the product. It represents an optimal solution to cool the Mars AX3 FPGA module - it is low profile (less than 7 mm tall) and covers the whole module surface. It comes with a gap pad for the FPGA device and four screws to attach it to the module PCB. With additional user configured gap pads, it is possible to cool other components on board as well.

Alternatively, if the Enclustra heat sink does not match the application requirements, a third-party heat sink body (ATS) and an additional gap pad (t-Global) may be used. Please note that the Enclustra heat sink kit already contains all necessary items for cooling the module (heat sink body, gap pad, mounting material).

Table 13 lists the heat sink and thermal pad part numbers that are compatible with the Mars AX3 FPGA module. Details on the Mars heat sink kit can be found in the Mars Heatsink Mounting Guide [16].

Product Name	Package Name	Enclustra Heat Sink	ATS Heat Sink	t-Global Thermal Pad
Mars AX3	CSG324 [21]	HS-MA1	ATS-52150G-C1-R0	TG-A6200-16-16-1

Table 13: Heat Sink Type

Please note that the adhesive heat sink part is recommended only for prototyping purposes. In cases where the module in used in environments subject to vibrations, a heat sink with mounting screws or clips may be required for optimal fixation.

Warning!

Depending on the user application, the Mars AX3 FPGA module may consume more power than can be dissipated without additional cooling measures; always make sure the FPGA is adequately cooled by installing a heat sink and/or providing air flow.

2.10.7 Voltage Monitoring

Several pins on the module connector on the Mars AX3 FPGA module are marked as VMON. These are voltage monitoring outputs that are used in the production test for measuring some of the on-board voltages.

It is not allowed to draw power from the voltage monitoring outputs.

Table 14 presents the VMON pins on the Mars AX3 FPGA module.

Pin Name	Module Connector Pin	Connection	Description
VMON_1V2	198	VCC_1V2	1.2 V on-board voltage (default)/FPGA battery voltage (assembly option)

Table 14: Voltage Monitoring Outputs

Warning!

The voltage monitoring outputs are for Enclustra-use only. Pinout changes may be applied between revisions.

2.11 Clock Generation

A 50 MHz oscillator is used for the Mars AX3 FPGA module clock generation; the 50 MHz clock is fed to the FPGA logic. The 25 MHz clock for the Ethernet PHYs is generated from the 50 MHz system oscillator. Table 15 describes the clock connections.

Signal Name	Frequency	FPGA Pin	FPGA Pin Type	Remark
CLK50	50 MHz	L16	IO_L3N_T0_DQS_EMCCLK_14	External configuration clock
		P17	IO_L12P_T1_MRCC_14	Main clock

Table 15: Module Clock Resources

2.12 Reset

The FPGA configuration clear signal (FPGA_PROG#) and the FPGA delay configuration signal (FPGA_INIT#) of the Artix-7 device are available on the module connector.

Pulling FPGA_PROG# low clears the FPGA configuration. Please refer to the Enclustra Module Pin Connection Guidelines [10] for general rules regarding the connection of reset pins and to the Xilinx documentation for details on the functions of the PROGRAM_B_0 and INIT_B_0 signals.

Table 16 presents the available reset signals. Both signals, FPGA_PROG# and FPGA_INIT#, have on-board 4.7 kΩ pull-up resistors to VCC_CFG_B14.

Signal Name	Connector Pin	FPGA Pin Type	Description
FPGA_PROG#	196	PROGRAM_B_0	Configuration clear signal
FPGA_INIT#	192	INIT_B_0	Delay configuration signal

Table 16: Reset Resources

FPGA_INIT# signal is also connected to a regular FPGA pin (FPGA_INIT#_R, package pin N15) via a 47 kΩ resistor and can be used to reset the FPGA logic. In this case, internal pull-up must not be used for this signal, in order to be able to reset the logic via FPGA_INIT# pin available on the module connector.

2.13 LEDs

The four LEDs on the Mars AX3 FPGA module are connected to the FPGA logic, and they are active-low.

Signal Name	FPGA Pin	Remarks
LED0#	M16	User function/active-low
LED1#	M17	User function/active-low
LED2#	L18	User function/active-low
LED3#	M18	User function/active-low

Table 17: LEDs

2.14 DDR3 SDRAM

The DDR3 SDRAM on the Mars AX3 FPGA module is operated at 1.35 V (low power mode) or at 1.5 V, depending on a selection signal. The DDR bus width is 16-bit.

The maximum memory bandwidth on the Mars AX3 FPGA module is:
800 Mbit/sec × 16 bit = 1600 MB/sec
For DDR3 low power mode (DDR3L) the speed can be lower than mentioned above. Details are available in the Artix-7 FPGAs DC and AC Switching Characteristics document [19].

2.14.1 DDR3 SDRAM Type

Table 18 describes the memory availability and configuration on the Mars AX3 FPGA module.

Module	SDRAM Type	Density	Configuration	Manufact.
MA-AX3-D8 (commercial)	MT41K128M16JT-125:K	2 Gbit	128 M × 16 bit	Micron
MA-AX3-D8 (commercial)	NT5CC128M16IP-DI	2 Gbit	128 M × 16 bit	Nanya
MA-AX3-D8 (industrial)	MT41K128M16JT-125 IT:K	2 Gbit	128 M × 16 bit	Micron
MA-AX3-D8 (industrial)	NT5CC128M16IP-DII	2 Gbit	128 M × 16 bit	Nanya

Table 18: DDR3 SDRAM Types

Warning!

Other DDR3 memory devices may be equipped in future revisions of the Mars AX3 FPGA module. Please check the user manual regularly for updates. Any parts with different speed bins or temperature ranges that fulfill the requirements for the module variant may be used.

2.14.2 Signal Description

Please refer to the Mars AX3 FPGA Module FPGA Pinout Excel Sheet [4] for detailed information on the DDR3 SDRAM connections.

2.14.3 Termination

Warning!

No external termination is implemented on the Mars AX3 FPGA module. Therefore, it is strongly recommended to enable the on-die termination (ODT) feature of the DDR3 SDRAM device.

2.14.4 Parameters

Please refer to the Mars AX3 FPGA module reference design [2] for DDR3 settings guidelines. The DDR3 SDRAM parameters to be set in Vivado project are presented in Table 19. If the memory part equipped on the module is not available in Vivado, a custom memory part can be created and configured as described in the table.

The values given in Table 19 are for reference only. Depending on the equipped memory device on the Mars AX3 FPGA module and on the DDR3 SDRAM frequency, the configuration may be different to the one in the reference design. Please refer to the memory device datasheet for details.

Parameter	Value
Memory voltage	1.5 V (for DDR3)/1.35 V (for DDR3L)
Data width	16 bit
Clock period	2500 - 3300 ps (range depending on the FPGA speedgrade)
Bank address bits	3
Row address bits	14
Column address bits	10
tcke	5.625 ns
tfaw	40.0 ns
tras	37.5 ns
trcd	15 ns
trefi	7.8 us
trfc	160 ns
trp	15 ns

Table 19: DDR3 SDRAM Parameters

2.14.5 DDR3 Low Voltage Operation

Low voltage operation for the DDR3 SDRAM is available only for modules revision 2 and newer.

The default voltage of the DDR3 is 1.5 V. In order to enable low voltage mode (1.35 V), DDR3_VSEL (pin D9) must be driven logic 0 by the FPGA logic, and a memory voltage of 1.35 V must be selected in the Memory Interface Generator (MIG) parameters in Vivado.

For 1.5 V operation, DDR3_VSEL must be set to high impedance (not driven logic 1).

2.15 QSPI Flash

The QSPI flash can be used to store the FPGA bitstream, Microblaze application code and other user data.

2.15.1 QSPI Flash Type

Table 20 describes the memory availability and configuration on the Mars AX3 FPGA module.

The bigger flash device introduced starting with revision 3 has bigger erase sectors (256 kB instead of 4 kB) and the 4 kB/32 kB/64 kB erase commands are not supported anymore. Further, the programming buffer is 512 bytes instead of 256 bytes. This may require adjustments of the programming algorithm.

Module	Flash Type	Size	Manufacturer
MA-AX3 - R1 and R2	W25Q128FVEIG	128 Mbit	Winbond
MA-AX3 - R3 and newer	S25FL512S	512 Mbit	Cypress (Spansion)

Table 20: QSPI Flash Types

Warning!

Other flash memory devices may be equipped in future revisions of the Mars AX3 FPGA module. Please check the user manual regularly for updates. Any parts with different speeds and temperature ranges that fulfill the requirements for the module variant may be used.

2.15.2 Signal Description

Signal Name	FPGA Pin Type	FPGA Pin	QSPI Pin Type Flash Pin	Module Connector Pin
FLASH_CLK_FPGA_CCLK	CCLK_0 IO_25_14	E9 R10	SCK	182
FLASH_CS#	IO_L6P_T0_FCS_B_14	L13	CS#	188
FLASH_DI	IO_L1P_T0_D00_MOSI_14	K17	SI/IO0	186
FLASH_DO_FPGA_DIN	IO_L1N_T0_D01_DIN_14	K18	SO/IO1	184
FLASH_WP#	IO_L2P_T0_D02_14	L14	WP#/IO2	-
FLASH_HOLD#	IO_L2N_T0_D03_14	M14	HOLD#/IO4	-

Table 21: QSPI Flash Interface

The QSPI flash is connected to the FPGA pins. Some of the signals are available on the module connector, allowing the user to program the QSPI flash from an external master.

Please refer to Section 3 for details on programming the flash memory.

Warning!

Special care must be taken when connecting the QSPI flash signals on the base board. Long traces or high capacitance may disturb the data communication between the FPGA and the flash device.

2.16 Gigabit Ethernet

A 10/100/1000 Mbit Ethernet PHY is available on the Mars AX3 FPGA module, connected to the FPGA via RGMII interface.

2.16.1 Ethernet PHY Type

Table 22 describes the equipped Ethernet PHY device type on the Mars AX3 FPGA module.

PHY Type	Manufacturer	Type
KSZ9031RNX	Microchip (Micrel)	10/100/1000 Mbit

Table 22: Gigabit Ethernet PHY Type

2.16.2 Signal Description

The RGMII interface is connected to FPGA bank 14. The reset pin for the PHYs has a pull-down resistor and needs to be driven high to release the PHYs from reset.

The active low ETH_LED2# signal is connected to the FPGA as link indicator. The interrupt output of the Ethernet PHY is connected to the ETH_INT# signal which is routed to an FPGA pin.

2.16.3 External Connectivity

The Ethernet signal lines can be connected directly to the magnetics. Please refer to the Enclustra Module Pin Connection Guidelines [10] for details regarding the connection of Ethernet signals.

2.16.4 MDIO Address

The MDIO address assigned to the Gigabit Ethernet PHY is 3. The MDIO interface is connected to the FPGA bank 14.

2.16.5 PHY Configuration

The configuration of the Ethernet PHY is bootstrapped when the PHY is released from reset. Make sure all I/Os on the RGMII interface are initialized and all pull-up or pull-down resistors are disabled at that moment.

The bootstrap options of the Ethernet PHY are set as indicated in Table 23.

Depending on the used IP core, configuration of the RGMII delays in the Ethernet PHYs may be required to achieve proper timing. For details on the RGMII delays, please refer to the PHY datasheet.

An example of PHY configuration is shown in the lwIP application provided in the Mars AX3 FPGA module reference design [2].

Pin	Signal Value	Description
MODE[3-0]	1110	RGMII mode: advertise all capabilities (10/100/1000, half/full duplex) except 1000Base-T half duplex.
PHYAD[2-0]	011	MDIO address 3
Clk125_EN	0	125 MHz clock output disabled
LED_MODE	1	Single LED mode
LED1/LED2	1	Active-low LEDs

Table 23: Gigabit Ethernet PHY Configuration

For the Ethernet PHY configuration via the MDIO interface, the MDC clock frequency must not exceed 1 MHz.

2.17 Real-Time Clock (RTC)

The real-time clock is not equipped by default on the Mars AX3 FPGA module revision 2 and newer. The RTC may be optionally equipped and connected to the I2C bus.

2.17.1 RTC Type

Table 24 describes the equipped/optional RTC device type on the Mars AX3 FPGA module.

Module	Type	Manufacturer	Equipped by default
MA-AX3 - R1	ISL12020M	Intersil	Yes
MA-AX3 - R2	ISL12020M	Intersil	No
MA-AX3 - R3 and newer	PCF85063ATL/1,118	NXP Semiconductors	No

Table 24: RTC Type

RTC on Revision 1
The RTC from Intersil features a battery-buffered 128 bytes user SRAM and a temperature sensor. See Section 4 for details on the I2C bus and devices on the Mars AX3 FPGA module.

VBAT pin of the RTC is connected to VCC_BAT on the module connector, and can be connected directly to a 3 V battery. Please refer to the Enclustra Module Pin Connection Guidelines [10] for details.

The interrupt output of the RTC is connected to the I2C interrupt line available on an FPGA pin. Note that the frequency output mode of the RTC must be disabled when using I2C interrupt system. Otherwise, I2C_INT# is periodically pulled down by the RTC. The disabling of this function can be done by setting bits [3:0] of the RTC register 8 to logic low.

RTC on Revision 2
On the Mars AX3 FPGA module revision 2 the interrupt line from the RTC is not active by default. In order to perform this connection, resistor R600 must be assembled; please contact Enclustra support for details.

RTC on Revision 3 and newer
The VCC pin of the RTC is connected to VCC_BAT on the module connector, and can be connected directly to a 3 V battery. The interrupt output of the RTC is connected to the I2C interrupt line available on an FPGA pin.

An example demonstrating how to use the RTC is included in the Mars AX3 FPGA module reference design [2], in the I2C example program. Note that the software does not perform automatically the reading of the RTC, as this circuit is not equipped in the standard configuration; however, the code can be easily modified to call the function that reads the values from the real-time clock.

2.18 Secure EEPROM

The secure EEPROM is used to store the module type and serial number, as well as the Ethernet MAC address and other information. It is connected to the I2C bus.

The secure EEPROM must not be used to store user data.

Please refer to Section 4.4 for details on the content of the EEPROM.

2.18.1 EEPROM Type

Table 25 describes the equipped EEPROM device type on the Mars AX3 FPGA module.

Module	Type	Manufacturer
MA-AX3 - R1 and R2	DS28CN01	Maxim
MA-AX3 - R3 and newer	ATSHA204A-MAHDA-T (default)	Atmel
MA-AX3 - R3 and newer	DS28CN01 (assembly option)	Maxim

Table 25: EEPROM Type

An example demonstrating how to read data from the EEPROM is included in the Mars AX3 FPGA module reference design [2].

3 Device Configuration

3.1 Configuration Signals

Table 26 describes the most important configuration pins.

Some of the pins are connected to a user I/O, as well as to a special purpose configuration pin. This is done for compatibility with other Mars modules, on which the configuration pins can be used as user I/Os after configuration.

Signal Name	FPGA Pin Type	FPGA Pin	QSPI Flash Pin	Mod. Conn. Pin	Comments
FLASH_CLK_FPGA_CCLK	CCLK_0 IO_25_14	E9 R10	SCK	182	10 kΩ pull-up to VCC_CFG_B14
FLASH_CS#	IO_L6P_T0_FCS_B_14	L13	CS#	188	10 kΩ pull-up to VCC_CFG_B14
FLASH_DI	IO_L1P_T0_D00_MOSI_14	K17	SI/IO0	186	10 kΩ pull-up to VCC_CFG_B14
FLASH_DO_FPGA_DIN	IO_L1N_T0_D01_DIN_14	K18	SO/IO1	184	10 kΩ pull-up to VCC_CFG_B14
FPGA_INIT#	INIT_B_0 IO_L11P_T1_SRCC_14[4]	P7 N15	-	192	4.7 kΩ pull-up to VCC_CFG_B14
FPGA_DONE	DONE_0	P10	-	194	1 kΩ pull-up to VCC_CFG_B14
FPGA_PROG#	PROGRAM_B_0	P9	-	196	4.7 kΩ pull-up to VCC_CFG_B14

Continued on next page...

Signal Name	FPGA Pin Type	FPGA Pin	QSPI Flash Pin	Mod. Conn. Pin	Comments
FPGA_MODE	M1_0 M2_0	P13 P11	-	190	4.7 kΩ pull-up to VCC_CFG_B14
FPGA_CFGBVS	CFGBVS_0[5]	P8	-	-	10 kΩ pull-up to VCC_CFG_B14

Table 26: FPGA Configuration Pins

Warning!

All configuration signals except for FPGA_MODE must be high impedance as soon as the device is released from reset. Violating this rule may damage the equipped FPGA device, as well as other devices on the Mars AX3 FPGA module.

3.2 Configuration Mode

The FPGA_MODE signals determine whether the FPGA device is configured from the QSPI flash or serially via SPI from an external device.

Table 27 describes the available configuration modes and the corresponding mode signals.

FPGA_MODE	Mode Straps [2:0]	Configuration Mode
0	001	Master serial configuration (boot from QSPI flash)
1	111	Slave serial configuration

Table 27: Configuration Modes

3.3 Pull-Up During Configuration

The Pull-Up During Configuration signal (PUDC) is pulled to GND on the module; as PUDC is an active-low signal, all FPGA I/Os will have the internal pull-up resistors enabled during device configuration.

If the application requires the pull-up during configuration to be disabled, this can be achieved by removing R202 component and by mounting R200 - in this configuration the PUDC pin is connected to VCC_CFG_B14.

[4]Not connected on revision 1 modules. For revision 2 or newer, FPGA_INIT# signal is connected to a regular FPGA pin via a 47 kΩ resistor.

[5]Note that the CFGBVS_0 (configuration bank voltage select) pin is set automatically to GND (if VCC_CFG_B14 is less than or equal to 1.8 V) or to VCCO (if VCC_CFG_B14 is 2.5 V or 3.3 V).

Figure 10 illustrates the configuration of the I/O signals during power-up. Figure 11 indicates the location of the pull-up/pull-down resistors on the module PCB - upper right part on the top view drawing.

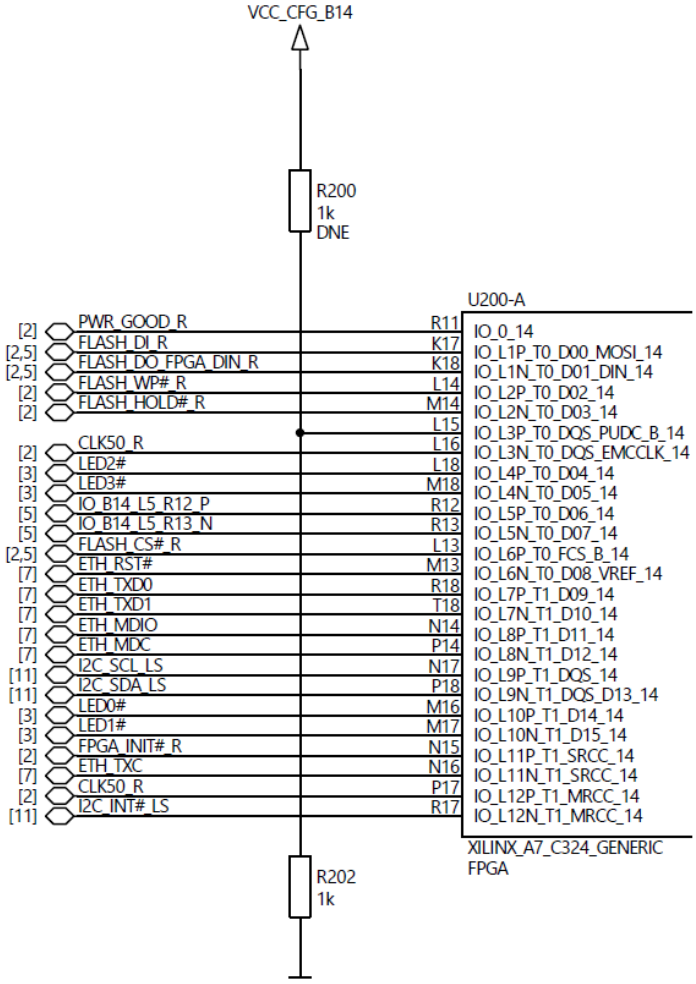

Figure 10: Pull-Up During Configuration (PUDC)

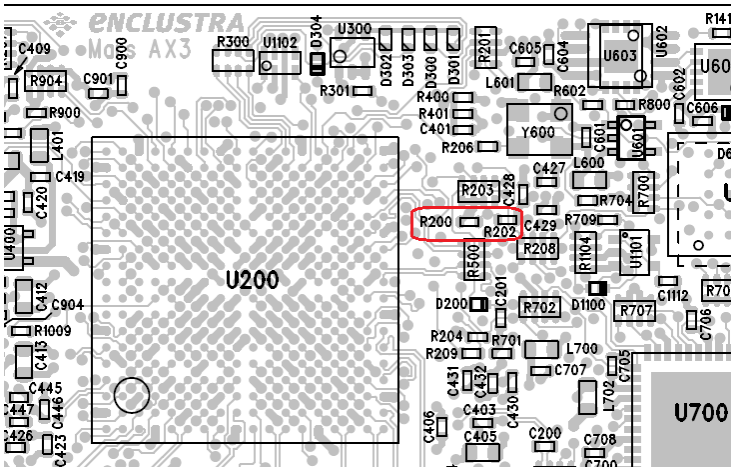

Figure 11: Pull-Up During Configuration (PUDC) Resistors - Assembly Drawing Top View (upper right part) for Revision 3 Modules

For details on the PUDC signal please refer to the 7 Series FPGAs Configuration User Guide [18].

3.4 JTAG

The JTAG interface can be used for configuring and debugging the FPGA logic. The JTAG signals on the FPGA are directly connected to the module connector.

The FPGA device and the QSPI flash can be configured via JTAG using Xilinx tools.

Please note that Xilinx ISE has limited support on the Artix-7 family; please use Xilinx Vivado to configure the FPGA.

The Winbond flash equipped on revisions 1 and 2 is not supported by Vivado (and only partially supported in iMPACT); please use Enclustra MCT [15] to program the QSPI flash. Section 3.7 gives a detailed description on the QSPI flash configuration options via JTAG.

3.4.1 JTAG on Module Connector

Signal Name	Module Connector Pin	Resistor
JTAG_TCK	158	4.7 kΩ pull-up to VCC_CFG_B14
JTAG_TMS	162	FPGA internal pull-up
JTAG_TDI	160	FPGA internal pull-up
JTAG_TDO	164	-

Table 28: JTAG Interface

3.4.2 External Connectivity

JTAG signals can be connected directly on the base board to a JTAG connector. No pull-up/pull-down resistors are necessary. The VREF pin of the programmer must be connected to VCC_CFG_B14.

It is recommended to add 22 Ω series termination resistors between the module and the JTAG header, close to the source. Please refer to the Enclustra Module Pin Connection Guidelines for details on JTAG interface.

3.5 Master Serial Configuration

In the master serial configuration mode, the FPGA reads the bitstream from the QSPI flash. The configuration clock can be configured up to 26 MHz and quad-SPI booting is supported. Higher configuration clocks can be achieved by using the advanced configuration settings of the Xilinx tools. For more information on the configuration modes, please refer to the 7 Series FPGAs Configuration User Guide [18].

3.5.1 Signal Description

Signal Name	Description
FLASH_CLK_FPGA_CCLK	Must be high impedance during configuration and operation
FLASH_DO_FPGA_DIN	Must be high impedance during configuration and operation
FPGA_INIT#	Is pulled low by the FPGA if any CRC error occurs during the configuration; it may be used as an input to delay the start of the FPGA configuration.
FPGA_DONE	Goes high after a successful FPGA configuration
FPGA_PROG#	When pulled low, the FPGA configuration sequence is cleared and all pins are tri-stated. The rising edge of FPGA_PROG# initializes the configuration.
FPGA_MODE	Must be pulled low during configuration
FLASH_DI	Must be high impedance during configuration and operation
FLASH_CS#	Must be high impedance during configuration and operation

Table 29: Master Serial Configuration - Signals Description

3.6 Slave Serial Configuration

In the slave serial configuration mode, the bitstream must be transmitted from an external device to the FPGA. The configuration pins of the FPGA are connected directly to the module connector, allowing the configuration of the FPGA from a microcontroller or another SPI capable device. For more information on the configuration modes, please refer to the 7 Series FPGAs Configuration User Guide [18].

For slave serial configuration the bitstream generation option “SPI_buswidth” must be set to 1 in the Xilinx tools.

3.6.1 Signal Description

Signal Name	Description
FLASH_CLK_FPGA_CCLK	Configuration clock
FLASH_DO_FPGA_DIN	Configuration data
FPGA_INIT#	Is pulled low by the FPGA if any CRC error occurs during the configuration; it may be used as an input to delay the start of the FPGA configuration.
FPGA_DONE	Goes high after a successful FPGA configuration
FPGA_PROG#	When pulled low, the FPGA configuration sequence is cleared and all pins are tri-stated. The rising edge of FPGA_PROG# initializes the configuration.
FPGA_MODE	Must be pulled high or left open during configuration

Table 30: Slave Serial Configuration - Signals Description

Warning!

Note that after the rising edge of FPGA_DONE, the FPGA still requires a number of clock cycles to finish the configuration. Therefore, if the FPGA_CCLK and FPGA_DIN pins are used in the FPGA design, the user must ensure that these are tri-stated by the FPGA logic for the appropriate amount of time. Details on the configuration time are available in Xilinx AR #42128.

3.7 QSPI Flash Programming via JTAG

Enclustra MCT [15] can be used to program the QSPI flash equipped on any Mars AX3 FPGA module revision as an alternative to programming via JTAG.

To use quad-mode for the SPI flash, the bitstream generation option "SPI_buswidth" must be set to 4 in the Xilinx tools. In addition, the SPI flash must be configured to 4-bit mode when programming the flash.

Please note that the FPGA_MODE pin must be pulled low for a successful flash programming using Xilinx iMPACT. Otherwise, iMPACT will report an error, as it tries to configure the FPGA from the flash after programming.

Modules Revisions 1 and 2
Please note that Xilinx iMPACT has limited support on the Artix-7 family and on the Winbond flash equipped on revision 1 and 2 modules.

The QSPI Flash on the MA-AX3-100 module can be programmed with the Xilinx iMPACT tool via JTAG. The 128 Mbit Winbond flash device W25Q128FV is not supported by all versions of iMPACT; in some versions the flash programming only works if the "W25Q128BV" is selected.

There is currently no Xilinx tool to configure the QSPI Flash on the MA-AX3-50 and MA-AX3-35 modules from revisions 1 and 2. This is because the Xilinx iMPACT tool does not have support for the equipped Artix-7 devices and Vivado has no support for the W25Q128FV flash.

Modules Revision 3 and newer
Modules revision 3 and newer are equipped with Cypress (Spansion) QSPI flash, which is supported by the Vivado and SDK tools. For more information, please refer to the Xilinx Documentation [20].

3.8 QSPI Flash Programming from an External SPI Master

The signals of the QSPI flash are directly connected to the module connector for flash access. As the flash signals are connected to the FPGA device as well, the FPGA device pins must be tri-stated while accessing the QSPI flash directly from an external device.

This is ensured by pulling the FPGA_PROG# to GND, which puts the FPGA device into reset state and tri-states all I/O pins during flash programming.

Figure 12 shows the signal diagrams corresponding to flash programming from an external master.

To use quad-mode for the SPI flash, the bitstream generation option "SPI_buswidth" must be set to 4 in the Xilinx tools. In addition, the SPI flash must be configured to 4-bit mode by the programmer.

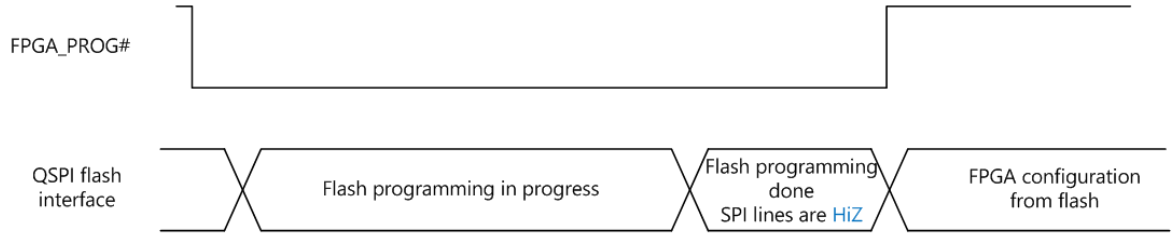

Figure 12: QSPI Flash Programming from an External SPI Master - Signal Diagrams

Warning!

Accessing the QSPI flash directly without putting the FPGA device into reset may damage the equipped FPGA device, as well as other devices on the Mars AX3 FPGA module.

3.8.1 Signal Description

Signal Name	QSPI Flash Pin	Description
FLASH_CLK_FPGA_CCLK	SCK	SPI CLK
FLASH_DO_FPGA_DIN	SO/IO1	SPI MISO
FPGA_PROG#	-	Must be pulled low during QSPI flash programming. When released, all other pins of the SPI interface must be high impedance.
FLASH_DI	SI/IO0	SPI MOSI
FLASH_CS#	CS#	SPI CS#

Table 31: Flash Programming from an External Master - Signals Description

3.9 Enclustra Module Configuration Tool

In combination with an Enclustra base board, the QSPI flash can be programmed using the Enclustra Module Configuration Tool (MCT) [15]. Slave serial configuration is also supported by the Enclustra MCT software.

4 I2C Communication

4.1 Overview

The I2C bus on the Mars AX3 FPGA module is connected to the FPGA device, EEPROM and RTC, and is available on the module connector. This allows external devices to read the module type and to connect more devices to the I2C bus.

Please note that for revision 1 and 2 modules (with equipped RTC) the RTC must be configured correctly to use I2C interrupts - for details, refer to Section 2.17.

The I2C clock frequency should not exceed 400 kHz.

Warning!

Maximum I2C speed may be limited by the routing path and additional loads on the base board.

Warning!

If the I2C traces on the base board are very long, 100 Ω series resistors should be added between module and I2C device on the base board.

4.2 Signal Description

Table 32 describes the signals of the I2C interface. All signals have on-board pull-up resistors to VCC_3V3. Level shifters are used between the I2C bus and the FPGA pins, to allow I/O voltages lower than 3.3 V. Please make sure that all pins are configured correctly and no pull-down resistors are enabled.

All signals must be connected to open collector outputs and must not be driven high from any source. I2C_INT# is an input to the FPGA and must not be driven from the FPGA device.

Signal Name	FPGA Pin	Connector Pin	Resistor
I2C_SDA	P18	176	2.2 kΩ pull-up
I2C_SCL	N17	178	2.2 kΩ pull-up
I2C_INT#	R17	174	4.7 kΩ pull-up

Table 32: I2C Signal Description

4.3 I2C Address Map

Table 33 describes the addresses for several devices connected on I2C bus.

Address (7-bit)	Description	Revision	Comments
0x5C 0x64	Secure EEPROM	1 and 2 3 and newer	Equipped Equipped
0x57	RTC user SRAM[6]	1 2	Equipped Optional
0x6F 0x6F 0x51	RTC registers	1 2 3 and newer	Equipped Optional Optional

Table 33: I2C Addresses

4.4 Secure EEPROM

The secure EEPROM is used to store the module serial number and configuration. In the future, the EEPROM will be used for copy protection and licensing features. Please contact us for further information.

An example demonstrating how to read the module information from the EEPROM memory is included in the Mars AX3 FPGA module reference design.

Warning!

The secure EEPROM is for Enclustra use only. Any attempt to write data to the secure EEPROM causes the warranty to be rendered void.

4.4.1 Memory Map

Address	Length (bits)	Description
0x00	32	Module serial number
0x04	32	Module product information
0x08	32	Module configuration
0x0C	32	Reserved
0x10	48	Ethernet MAC address
0x16	48	Reserved
0x1C	32	Checksum (only for DS28CN01 EEPROM type)

Table 34: EEPROM Sector 0 Memory Map

[6] RTC user SRAM is only available on the Intersil RTC equipped/optionally equipped on revisions 1 and 2.

Module Serial Number

The module serial number is a unique 32-bit number that identifies the module. It is stored using big-endian byte order (MSB on the lowest address).

Module Product Information

This field indicates the type of module and hardware revision.

Module	Product Family	Reserved	Revision	Product Information
Mars AX3 FPGA module	0x0324	0x[XX]	0x[YY]	0x0324 [XX][YY]

Table 35: Product Information

Module Configuration

Addr.	Bits	Comment	Min. Value	Max. Value	Comment
0x08	7-4	FPGA type	0	4	See FPGA type table (Table 37)
	3-0	FPGA device speed grade	1	3	
0x09	7	Temperature range	0 (Commercial)	1 (Industrial)	
	6	Power grade	0 (Normal)	1 (Low power)	
	5-4	Ethernet port count	0	1	
	3	Ethernet speed	0 (Fast Ethernet)	1 (Gigabit Ethernet)	
	2	RTC equipped	0	1	
	1-0	Reserved	-	-	
0x0A	7-0	Reserved	-	-	
0x0B	7-4	DDR3 RAM size (MB)	0 (0 MB)	7 (512 MB)	Resolution = 8 MB
	3-0	QSPI flash memory size (MB)	0 (0 MB)	7 (64 MB)	Resolution = 1 MB

Table 36: Module Configuration

The memory sizes are defined as Resolution$\times 2^{(Value-1)}$ (e.g. DRAM=0: not equipped, DRAM=1: 8 MB, DRAM=2: 16 MB, DRAM=3: 32 MB, etc).

Table 37 shows the available FPGA types.

Value	FPGA Device Type
0	Not used
1	XC7A35T
2	XC7A50T
3	XC7A75T
4	XC7A100T

Table 37: FPGA Device Types

Ethernet MAC Address

The Ethernet MAC address is stored using big-endian byte order (MSB on the lowest address). Each module is assigned two sequential MAC addresses; only the lower one is stored in the EEPROM.

5 Operating Conditions

5.1 Absolute Maximum Ratings

Table 38 indicates the absolute maximum ratings for Mars AX3 FPGA module. The values given are for reference only; for details please refer to the Artix-7 Datasheet [19].

Symbol	Description	Rating	Unit
VCC_MOD	Supply voltage relative to GND	-0.5 to 6	V
VCC_3V3	3.3 V supply voltage relative to GND	-0.5 to 3.6	V
VCC_BAT	Supply voltage for the RTC and encryption key storage	-0.3 to 3.6	V
VCC_IO_[x] VCC_CFG_[x]	Output drivers supply voltage relative to GND	-0.5 to 3.6	V
V_IO	I/O input voltage relative to GND	-0.5 to V_{CCO}+0.5	V
V_ADC	Analog I/O input voltage for the ADC	-0.5 to 2.3	V
Temperature	Temperature range for commercial modules (C)* Temperature range for industrial modules (I)*	0 to +70 -40 to +85	°C °C

Table 38: Absolute Maximum Ratings

5.2 Recommended Operating Conditions

Table 39 indicates the recommended operating conditions for Mars AX3 FPGA module. The values given are for reference only; for details please refer to the Artix-7 Datasheet [19].

Symbol	Description	Rating	Unit
VCC_MOD	Supply voltage relative to GND	3.0 to 5.5	V
VCC_3V3	3.3 V supply voltage relative to GND	3.15 to 3.45	V
VCC_BAT	Supply voltage for the RTC and encryption key storage	2.0 to 3.45	V
VCC_IO_[x] VCC_CFG_[x]	Output drivers supply voltage relative to GND	Refer to Section 2.9.5	V
V_IO	I/O input voltage relative to GND	-0.2 to V_{CCO}+0.2	V
V_ADC	Analog I/O input voltage for the ADC	0 to 1.5	V
Temperature	Temperature range for commercial modules (C)* Temperature range for industrial modules (I)*	0 to +70 -40 to +85	°C °C

Table 39: Recommended Operating Conditions

Warning!

** The components used on the hardware are specified for the relevant temperature range. The user must provide adequate cooling in order to keep the temperature of the components within the specified range.*

6 Ordering and Support

6.1 Ordering

Please use the Enclustra online request/order form for ordering or requesting information:
`http://www.enclustra.com/en/order/`

6.2 Support

Please follow the instructions on the Enclustra online support site:
`http://www.enclustra.com/en/support/`

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References

[1] Enclustra General Business Conditions
http://www.enclustra.com/en/products/gbc/
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→ Ask Enclustra for details
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