Wide Supply Range, Rail-to-Rail Output Instrumentation Amplifier

AD8426

FEATURES

- 2 channels in a small, 4 mm × 4 mm LFCSP
- LFCSP package has no metal pad
  - More routing room
  - No current leakage to pad
- Gain set with 1 external resistor
  - Gain range: 1 to 1000
- Input voltage goes below ground
- Inputs protected beyond supplies
- Very wide power supply range
  - Single supply: 2.2 V to 36 V
  - Dual supply: ±1.35 V to ±18 V
- Bandwidth (G = 1): 1 MHz
- CMRR (G = 1): 80 dB minimum
- Input noise: 24 nV/√Hz
- Typical supply current (per amplifier): 350 µA
- Specified temperature range: −40°C to +125°C

APPLICATIONS

- Industrial process controls
- Bridge amplifiers
- Medical instrumentation
- Portable data acquisition
- Multichannel systems

CONNECTION DIAGRAM

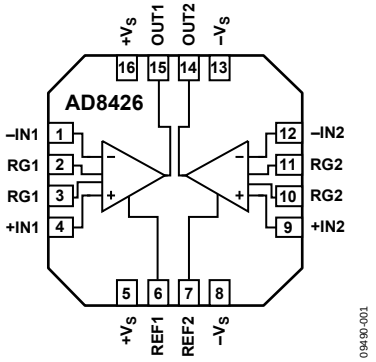

Figure 1.

Table 1. Instrumentation Amplifiers by Category[1]

General-Purpose	Zero Drift	Military Grade	Low Power	High Speed PGA
AD8220	AD8231	AD620	AD627	AD8250
AD8221	AD8290	AD621	AD623	AD8251
AD8222	AD8293	AD524	AD8235	AD8253
AD8224	AD8553	AD526	AD8236	
AD8228	AD8556	AD624	AD8426	
AD8295	AD8557		AD8226	
			AD8227	

[1] See www.analog.com for the latest instrumentation amplifiers.

GENERAL DESCRIPTION

The AD8426 is a dual-channel, low cost, wide supply range instrumentation amplifier that requires only one external resistor to set any gain from 1 to 1000.

The AD8426 is designed to work with a variety of signal voltages. A wide input range and rail-to-rail output allow the signal to make full use of the supply rails. Because the input range can also go below the negative supply, small signals near ground can be amplified without requiring dual supplies. The AD8426 operates on supplies ranging from ±1.35 V to ±18 V for dual supplies and 2.2 V to 36 V for a single supply.

The robust AD8426 inputs are designed to connect to real-world sensors. In addition to its wide operating range, the AD8426 can handle voltages beyond the rails. For example, with a ±5 V supply, the part is guaranteed to withstand ±35 V at the input with no damage. Minimum and maximum input bias currents are specified to facilitate open-wire detection.

The AD8426 is designed to make PCB routing easy and efficient. The two amplifiers are arranged in a logical way so that typical application circuits have short routes and few vias. Unlike most chip scale packages, the AD8426 does not have an exposed metal pad on the bottom of the part, which frees additional space for routing and vias. The AD8426 offers two in-amps in the equivalent board space of a typical MSOP package.

The AD8426 is ideal for multichannel, space-constrained industrial applications. Unlike other low cost, low power instrumentation amplifiers, the AD8426 is designed with a minimum gain of 1 and can easily handle ±10 V signals. With its space-saving LFCSP package and 125°C temperature rating, the AD8426 thrives in tightly packed, zero airflow designs.

The AD8226 is the single-channel version of the AD8426.

Rev. 0

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REVISION HISTORY

7/11—Revision 0: Initial Version

SPECIFICATIONS

DUAL-SUPPLY OPERATION

$+V_S$ = +15 V, $-V_S$ = −15 V, V_{REF} = 0 V, T_A = 25°C, G = 1, R_L = 10 kΩ, specifications referred to input, unless otherwise noted.

Table 2.

Parameter	Test Conditions/ Comments	A Grade			B Grade			Unit
		Min	Typ	Max	Min	Typ	Max	
COMMON-MODE REJECTION RATIO (CMRR)	V_{CM} = −10 V to +10 V							
CMRR, DC to 60 Hz								
G = 1		80			90			dB
G = 10		100			105			dB
G = 100		105			110			dB
G = 1000		105			110			dB
CMRR at 5 kHz								
G = 1		80			80			dB
G = 10		90			90			dB
G = 100		90			90			dB
G = 1000		100			100			dB
NOISE	Total noise: $e_N = \sqrt{(e_{NI}^2 + (e_{NO}/G)^2)}$							
Voltage Noise	f = 1 kHz							
Input Voltage Noise, e_{NI}			24	27		24	27	nV/√Hz
Output Voltage Noise, e_{NO}			120	125		120	125	nV/√Hz
RTI Noise	f = 0.1 Hz to 10 Hz							
G = 1			2			2		μV p-p
G = 10			0.5			0.5		μV p-p
G = 100 to 1000			0.4			0.4		μV p-p
Current Noise	f = 1 kHz		100			100		fA/√Hz
	f = 0.1 Hz to 10 Hz		3			3		pA p-p
VOLTAGE OFFSET	Total offset voltage: $V_{OS} = V_{OSI} + (V_{OSO}/G)$							
Input Offset, V_{OSI}	V_S = ±5 V to ±15 V			200			100	μV
Average Temperature Coefficient	T_A = −40°C to +125°C		0.5	2		0.5	1	μV/°C
Output Offset, V_{OSO}	V_S = ±5 V to ±15 V			1000			500	μV
Average Temperature Coefficient	T_A = −40°C to +125°C		2	10		1	5	μV/°C
Offset RTI vs. Supply (PSR)	V_S = ±5 V to ±15 V							
G = 1		80			90			dB
G = 10		100			105			dB
G = 100		105			110			dB
G = 1000		105			110			dB
INPUT CURRENT								
Input Bias Current[1]	T_A = +25°C	5	20	27	5	20	27	nA
	T_A = +125°C	5	15	25	5	15	25	nA
	T_A = −40°C	5	30	35	5	30	35	nA
Average Temperature Coefficient	T_A = −40°C to +125°C		70			70		pA/°C
Input Offset Current	T_A = +25°C			1.5			0.5	nA
	T_A = +125°C			1.5			0.5	nA
	T_A = −40°C			2			0.5	nA
Average Temperature Coefficient	T_A = −40°C to +125°C		5			5		pA/°C

Parameter	Test Conditions/ Comments	A Grade			B Grade			Unit
		Min	Typ	Max	Min	Typ	Max	
REFERENCE INPUT								
R_{IN}			100			100		kΩ
I_{IN}			7			7		μA
Voltage Range		$-V_S$		$+V_S$	$-V_S$		$+V_S$	V
Reference Gain to Output			1			1		V/V
Reference Gain Error			0.01			0.01		%
GAIN	$G = 1 + (49.4\ k\Omega/R_G)$							
Gain Range		1		1000	1		1000	V/V
Gain Error	$V_{OUT} \pm 10$ V							
G = 1				0.04			0.01	%
G = 5 to 1000				0.3			0.1	%
Gain Nonlinearity	$V_{OUT} = -10$ V to +10 V							
G = 1 to 10	$R_L \geq 2$ kΩ			20			20	ppm
G = 100	$R_L \geq 2$ kΩ			75			75	ppm
G = 1000	$R_L \geq 2$ kΩ			750			750	ppm
Gain vs. Temperature[2]								
G = 1	$T_A = -40°C$ to +85°C			5			1	ppm/°C
	$T_A = +85°C$ to +125°C			5			2	ppm/°C
G > 1	$T_A = -40°C$ to +125°C			−100			−100	ppm/°C
INPUT	$V_S = \pm 1.35$ V to +36 V							
Input Impedance								
Differential			0.8||2			0.8||2		GΩ||pF
Common Mode			0.4||2			0.4||2		GΩ||pF
Input Operating Voltage Range[3]	$T_A = +25°C$	$-V_S - 0.1$		$+V_S - 0.8$	$-V_S - 0.1$		$+V_S - 0.8$	V
	$T_A = +125°C$	$-V_S - 0.05$		$+V_S - 0.6$	$-V_S - 0.05$		$+V_S - 0.6$	V
	$T_A = -40°C$	$-V_S - 0.15$		$+V_S - 0.9$	$-V_S - 0.15$		$+V_S - 0.9$	V
Input Overvoltage Range	$T_A = -40°C$ to +125°C	$+V_S - 40$		$-V_S + 40$	$+V_S - 40$		$-V_S + 40$	V
OUTPUT								
Output Swing								
$R_L = 2$ kΩ to Ground	$T_A = +25°C$	$-V_S + 0.4$		$+V_S - 0.7$	$-V_S + 0.4$		$+V_S - 0.7$	V
	$T_A = +125°C$	$-V_S + 0.4$		$+V_S - 1.0$	$-V_S + 0.4$		$+V_S - 1.0$	V
	$T_A = -40°C$	$-V_S + 1.2$		$+V_S - 1.1$	$-V_S + 1.2$		$+V_S - 1.1$	V
$R_L = 10$ kΩ to Ground	$T_A = +25°C$	$-V_S + 0.2$		$+V_S - 0.2$	$-V_S + 0.2$		$+V_S - 0.2$	V
	$T_A = +125°C$	$-V_S + 0.3$		$+V_S - 0.3$	$-V_S + 0.3$		$+V_S - 0.3$	V
	$T_A = -40°C$	$-V_S + 0.2$		$+V_S - 0.2$	$-V_S + 0.2$		$+V_S - 0.2$	V
$R_L = 100$ kΩ to Ground	$T_A = -40°C$ to +125°C	$-V_S + 0.1$		$+V_S - 0.1$	$-V_S + 0.1$		$+V_S - 0.1$	V
Short-Circuit Current			13			13		mA
POWER SUPPLY								
Operating Range	Dual-supply operation	±1.35		±18	±1.35		±18	V
Quiescent Current (Per Amplifier)	$T_A = +25°C$		350	425		350	425	μA
	$T_A = -40°C$		250	325		250	325	μA
	$T_A = +85°C$		450	525		450	525	μA
	$T_A = +125°C$		525	600		525	600	μA
TEMPERATURE RANGE		−40		+125	−40		+125	°C

[1] The input stage uses PNP transistors; therefore, input bias current always flows into the part.
[2] The values specified for G > 1 do not include the effects of the external gain-setting resistor, R_G.
[3] Input voltage range of the AD8426 input stage. The input range depends on the common-mode voltage, the differential voltage, the gain, and the reference voltage. See the Input Voltage Range section for more information.

Dynamic Performance Specifications

$+V_S$ = +15 V, $-V_S$ = −15 V, V_{REF} = 0 V, T_A = 25°C, G = 1, R_L = 10 kΩ, specifications referred to input, unless otherwise noted.

Table 3. Single-Ended Output Configuration (Both Amplifiers)

Parameter	Test Conditions/ Comments	A Grade			B Grade			Unit
		Min	Typ	Max	Min	Typ	Max	
DYNAMIC RESPONSE								
Small Signal −3 dB Bandwidth								
G = 1			1000			1000		kHz
G = 10			160			160		kHz
G = 100			20			20		kHz
G = 1000			2			2		kHz
Settling Time 0.01%	10 V step							
G = 1			25			25		µs
G = 10			15			15		µs
G = 100			40			40		µs
G = 1000			750			750		µs
Slew Rate								
G = 1			0.4			0.4		V/µs
G = 5 to 100			0.6			0.6		V/µs

Table 4. Differential Output Configuration

Parameter	Test Conditions/ Comments	A Grade			B Grade			Unit
		Min	Typ	Max	Min	Typ	Max	
DYNAMIC RESPONSE								
Small Signal −3 dB Bandwidth								
G = 1			850			850		kHz
G = 10			300			300		kHz
G = 100			30			30		kHz
G = 1000			2			2		kHz
Settling Time 0.01%	10 V step							
G = 1			25			25		µs
G = 10			15			15		µs
G = 100			80			80		µs
G = 1000			300			300		µs
Slew Rate								
G = 1			0.4			0.4		V/µs
G = 5 to 100			0.6			0.6		V/µs

SINGLE-SUPPLY OPERATION

$+V_S$ = 2.7 V, $-V_S$ = 0 V, V_{REF} = 0 V, T_A = 25°C, G = 1, R_L = 10 kΩ, specifications referred to input, unless otherwise noted.

Table 5.

Parameter	Test Conditions/ Comments	A Grade			B Grade			Unit
		Min	Typ	Max	Min	Typ	Max	
COMMON-MODE REJECTION RATIO (CMRR)	V_{CM} = 0 V to 1.7 V							
CMRR, DC to 60 Hz								
G = 1			80			90		dB
G = 10			100			105		dB
G = 100			105			110		dB
G = 1000			105			110		dB
CMRR at 5 kHz								
G = 1			80			80		dB
G = 10			90			90		dB
G = 100			90			90		dB
G = 1000			100			100		dB
NOISE	Total noise: $e_N = \sqrt{(e_{NI}^2 + (e_{NO}/G)^2)}$							
Voltage Noise	f = 1 kHz							
Input Voltage Noise, e_{NI}			24	27		24	27	nV/√Hz
Output Voltage Noise, e_{NO}			120	125		120	125	nV/√Hz
RTI Noise	f = 0.1 Hz to 10 Hz							
G = 1			2			2		μV p-p
G = 10			0.5			0.5		μV p-p
G = 100 to 1000			0.4			0.4		μV p-p
Current Noise	f = 1 kHz		100			100		fA/√Hz
	f = 0.1 Hz to 10 Hz		3			3		pA p-p
VOLTAGE OFFSET	Total offset voltage: $V_{OS} = V_{OSI} + (V_{OSO}/G)$							
Input Offset, V_{OSI}				300			150	μV
Average Temperature Coefficient	T_A = −40°C to +125°C		0.5	3		0.5	1.5	μV/°C
Output Offset, V_{OSO}				1000			500	μV
Average Temperature Coefficient	T_A = −40°C to +125°C		2	12		1	8	μV/°C
Offset RTI vs. Supply (PSR)	V_S = 2.7 V to 36 V							
G = 1		80			90			dB
G = 10		100			105			dB
G = 100		105			110			dB
G = 1000		105			110			dB
INPUT CURRENT								
Input Bias Current[1]	T_A = +25°C	5	20	30	5	20	30	nA
	T_A = +125°C	5	15	28	5	15	28	nA
	T_A = −40°C	5	30	38	5	30	38	nA
Average Temperature Coefficient	T_A = −40°C to +125°C		70			70		pA/°C
Input Offset Current	T_A = +25°C			2			1	nA
	T_A = +125°C			2			1	nA
	T_A = −40°C			3			1	nA
Average Temperature Coefficient	T_A = −40°C to +125°C		5			5		pA/°C

Parameter	Test Conditions/ Comments	A Grade			B Grade			Unit
		Min	Typ	Max	Min	Typ	Max	
REFERENCE INPUT								
R_{IN}			100			100		kΩ
I_{IN}			7			7		μA
Voltage Range		$-V_S$		$+V_S$	$-V_S$		$+V_S$	V
Reference Gain to Output			1			1		V/V
Reference Gain Error			0.01			0.01		%
GAIN	G = 1 + (49.4 kΩ/R_G)							
Gain Range		1		1000	1		1000	V/V
Gain Error								
G = 1	V_{OUT} = 0.8 V to 1.8 V			0.05			0.05	%
G = 5 to 1000	V_{OUT} = 0.2 V to 2.5 V			0.3			0.1	%
Gain vs. Temperature[2]								
G = 1	T_A = −40°C to +85°C			5			1	ppm/°C
	T_A = +85°C to +125°C			5			2	ppm/°C
G > 1	T_A = −40°C to +125°C			−100			−100	ppm/°C
INPUT	$-V_S$ = 0 V, $+V_S$ = 2.7 V to 36 V							
Input Impedance								
Differential			0.8||2			0.8||2		GΩ||pF
Common Mode			0.4||2			0.4||2		GΩ||pF
Input Operating Voltage Range[3]	T_A = +25°C	−0.1		$+V_S$ − 0.7	−0.1		$+V_S$ − 0.7	V
	T_A = +125°C	−0.05		$+V_S$ − 0.6	−0.05		$+V_S$ − 0.6	V
	T_A = −40°C	−0.15		$+V_S$ − 0.9	−0.15		$+V_S$ − 0.9	V
Input Overvoltage Range	T_A = −40°C to +125°C	$+V_S$ − 40		$-V_S$ + 40	$+V_S$ − 40		$-V_S$ + 40	V
OUTPUT								
Output Swing								
R_L = 10 kΩ to 1.35 V	T_A = −40°C to +125°C	0.1		$+V_S$ − 0.1	0.1		$+V_S$ − 0.1	V
Short-Circuit Current			13			13		mA
POWER SUPPLY								
Operating Range	Single-supply operation	2.2		36	2.2		36	V
Quiescent Current (Per Amplifier)	$-V_S$ = 0 V, $+V_S$ = 2.7 V							
	T_A = +25°C		325	400		325	400	μA
	T_A = −40°C		250	325		250	325	μA
	T_A = +85°C		425	500		425	500	μA
	T_A = +125°C		475	550		475	550	μA
TEMPERATURE RANGE		−40		+125	−40		+125	°C

[1] The input stage uses PNP transistors; therefore, input bias current always flows into the part.
[2] The values specified for G > 1 do not include the effects of the external gain-setting resistor, R_G.
[3] Input voltage range of the AD8426 input stage. The input range depends on the common-mode voltage, the differential voltage, the gain, and the reference voltage. See the Input Voltage Range section for more information.

Dynamic Performance Specifications

$+V_S$ = 2.7 V, $-V_S$ = 0 V, V_{REF} = 0 V, T_A = 25°C, G = 1, R_L = 10 kΩ, specifications referred to input, unless otherwise noted.

Table 6. Single-Ended Output Configuration (Both Amplifiers)

Parameter	Test Conditions/ Comments	A Grade			B Grade			Unit
		Min	Typ	Max	Min	Typ	Max	
DYNAMIC RESPONSE								
Small Signal −3 dB Bandwidth								
G = 1			1000			1000		kHz
G = 10			160			160		kHz
G = 100			20			20		kHz
G = 1000			2			2		kHz
Settling Time 0.01%	2 V step							
G = 1			6			6		µs
G = 10			6			6		µs
G = 100			35			35		µs
G = 1000			750			750		µs
Slew Rate								
G = 1			0.4			0.4		V/µs
G = 5 to 100			0.6			0.6		V/µs

Table 7. Differential Output Configuration

Parameter	Test Conditions/ Comments	A Grade			B Grade			Unit
		Min	Typ	Max	Min	Typ	Max	
DYNAMIC RESPONSE								
Small Signal −3 dB Bandwidth								
G = 1			850			850		kHz
G = 10			300			300		kHz
G = 100			30			30		kHz
G = 1000			2			2		kHz
Settling Time 0.01%	2 V step							
G = 1			25			25		µs
G = 10			15			15		µs
G = 100			80			80		µs
G = 1000			300			300		µs
Slew Rate								
G = 1			0.4			0.4		V/µs
G = 5 to 100			0.6			0.6		V/µs

ABSOLUTE MAXIMUM RATINGS

Table 8.

Parameter	Rating
Supply Voltage	±18 V
Output Short-Circuit Current	Indefinite
Maximum Voltage at −INx or +INx	$-V_S$ + 40 V
Minimum Voltage at −INx or +INx	$+V_S$ − 40 V
REFx Voltage	$\pm V_S$
Storage Temperature Range	−65°C to +150°C
Specified Temperature Range	−40°C to +125°C
Maximum Junction Temperature	130°C
ESD	
Human Body Model	1.5 kV
Charged Device Model	1.5 kV
Machine Model	100 V

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

THERMAL RESISTANCE

The θ_{JA} value in Table 9 assumes a 4-layer JEDEC standard board with zero airflow.

Table 9.

Package	θ_{JA}	Unit
16-Lead LFCSP (CP-16-19)	86	°C/W

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

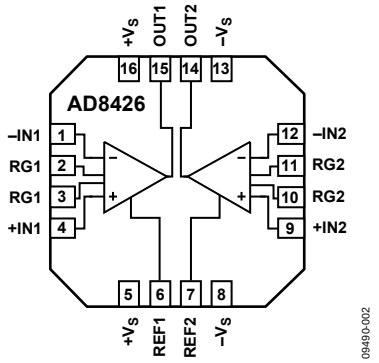


Figure 2. Pin Configuration

Table 10. Pin Function Descriptions

Pin No.	Mnemonic	Description
1	–IN1	Negative Input, In-Amp 1
2	RG1	Gain-Setting Resistor Terminal, In-Amp 1
3	RG1	Gain-Setting Resistor Terminal, In-Amp 1
4	+IN1	Positive Input, In-Amp 1
5	$+V_S$	Positive Supply
6	REF1	Reference Adjust, In-Amp 1
7	REF2	Reference Adjust, In-Amp 2
8	$-V_S$	Negative Supply
9	+IN2	Positive Input, In-Amp 2
10	RG2	Gain-Setting Resistor Terminal, In-Amp 2
11	RG2	Gain-Setting Resistor Terminal, In-Amp 2
12	–IN2	Negative Input, In-Amp 2
13	$-V_S$	Negative Supply
14	OUT2	Output, In-Amp 2
15	OUT1	Output, In-Amp 1
16	$+V_S$	Positive Supply

TYPICAL PERFORMANCE CHARACTERISTICS

T_A = 25°C, V_S = ±15 V, R_L = 10 kΩ, unless otherwise noted.

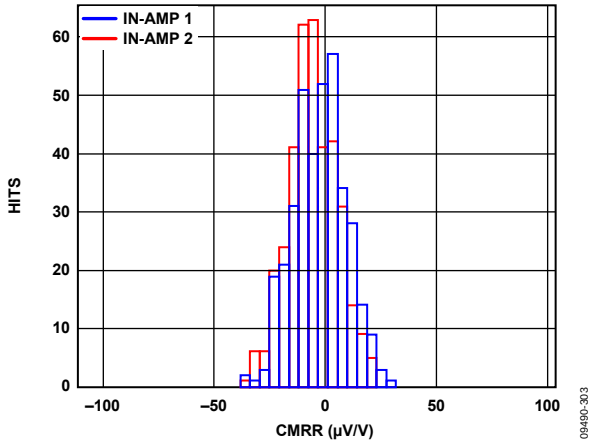


Figure 3. Typical Distribution for CMRR (G = 1)

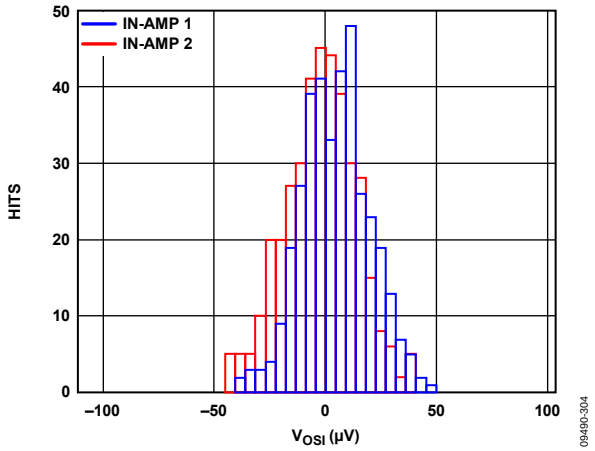


Figure 4. Typical Distribution of Input Offset Voltage

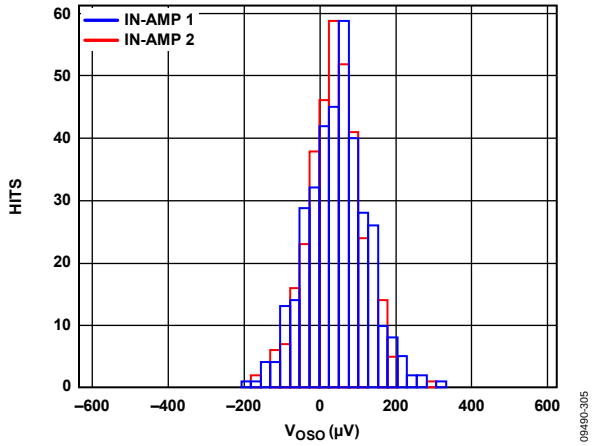


Figure 5. Typical Distribution of Output Offset Voltage

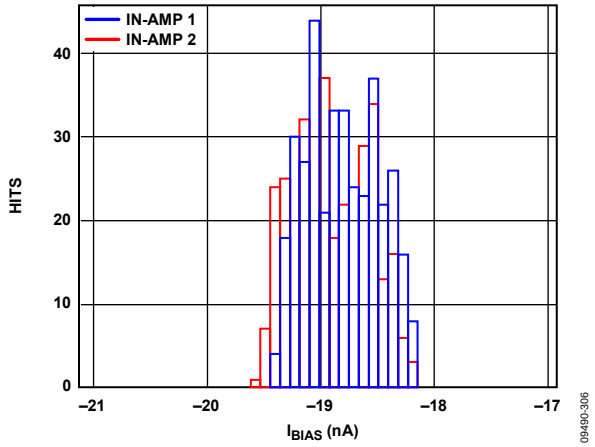


Figure 6. Typical Distribution of Input Bias Current, Inverting Input

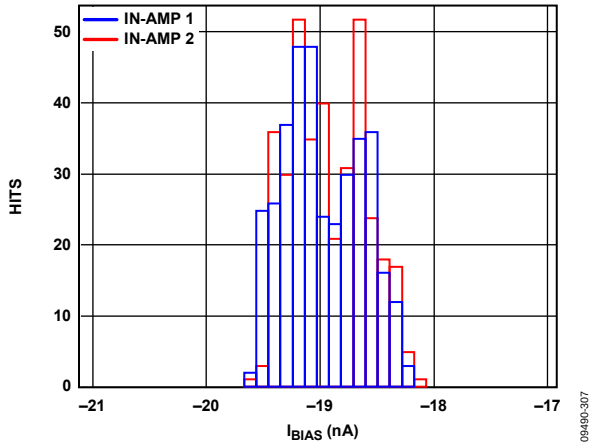


Figure 7. Typical Distribution of Input Bias Current, Noninverting Input

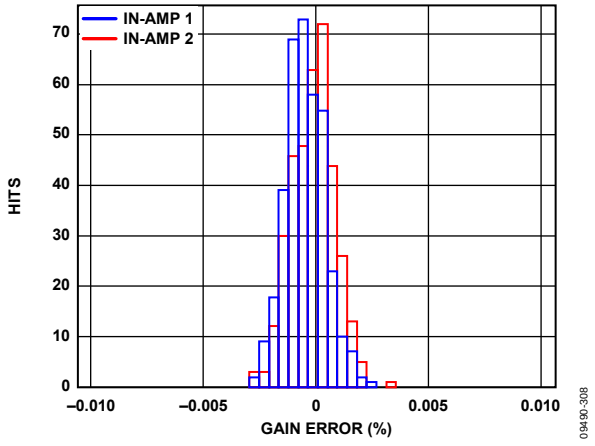


Figure 8. Typical Distribution of Gain Error (G = 1)

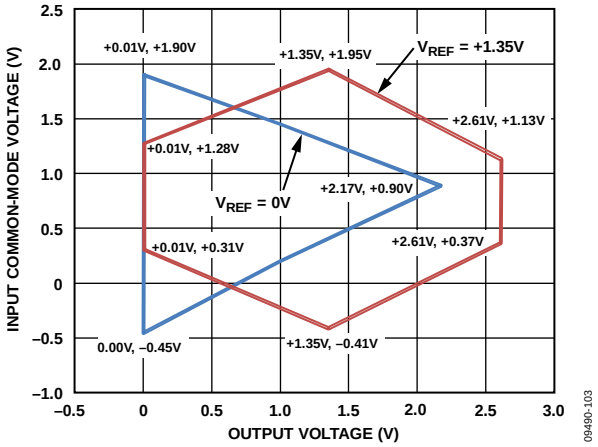


Figure 9. Input Common-Mode Voltage vs. Output Voltage, Single Supply, V_S = 2.7 V, G = 1

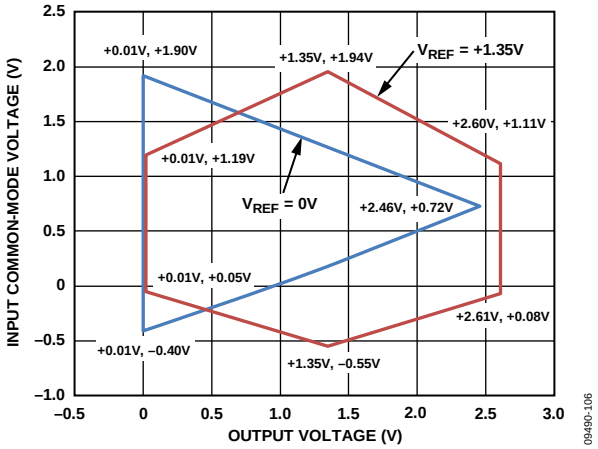


Figure 12. Input Common-Mode Voltage vs. Output Voltage, Single Supply, V_S = 2.7 V, G = 100

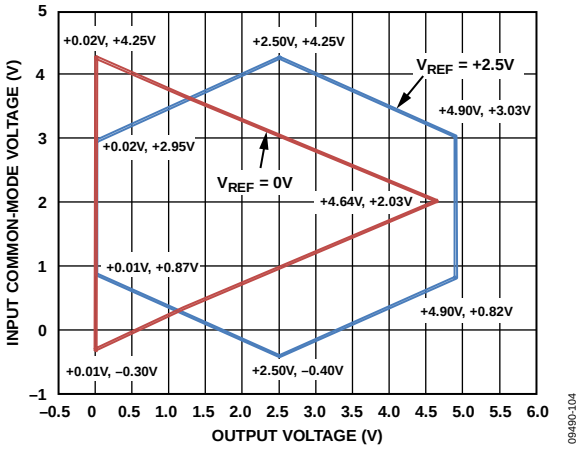


Figure 10. Input Common-Mode Voltage vs. Output Voltage, Single Supply, V_S = 5 V, G = 1

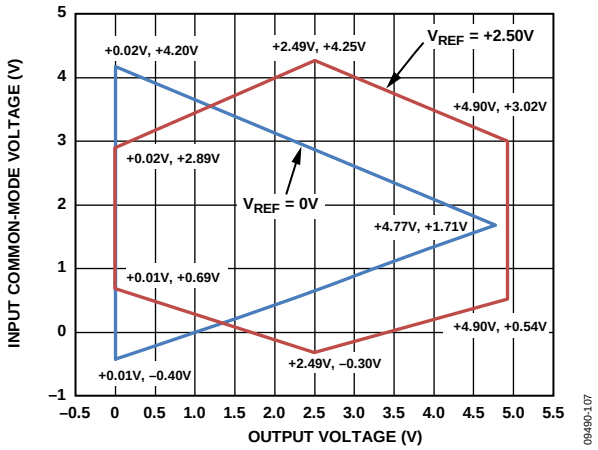


Figure 13. Input Common-Mode Voltage vs. Output Voltage, Single Supply, V_S = 5 V, G = 100

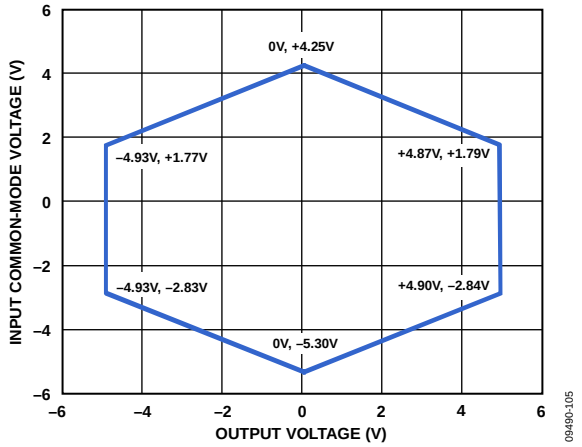


Figure 11. Input Common-Mode Voltage vs. Output Voltage, Dual Supply, V_S = ±5 V, G = 1

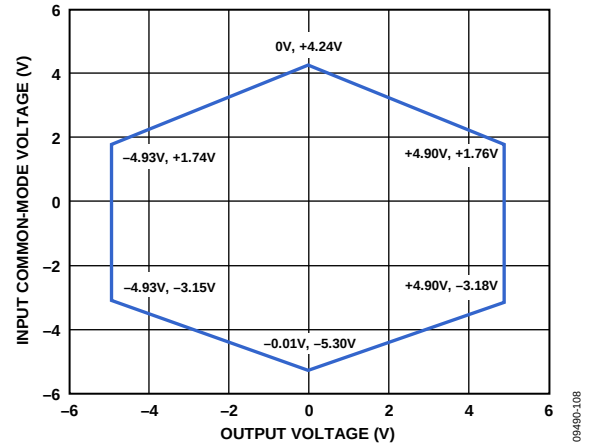


Figure 14. Input Common-Mode Voltage vs. Output Voltage, Dual Supply, V_S = ±5 V, G = 100

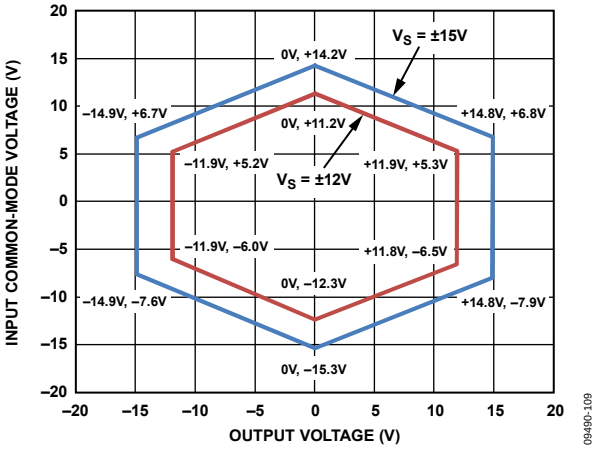


Figure 15. Input Common-Mode Voltage vs. Output Voltage, Dual Supply, V_S = ±15 V and V_S = ±12 V, G = 1

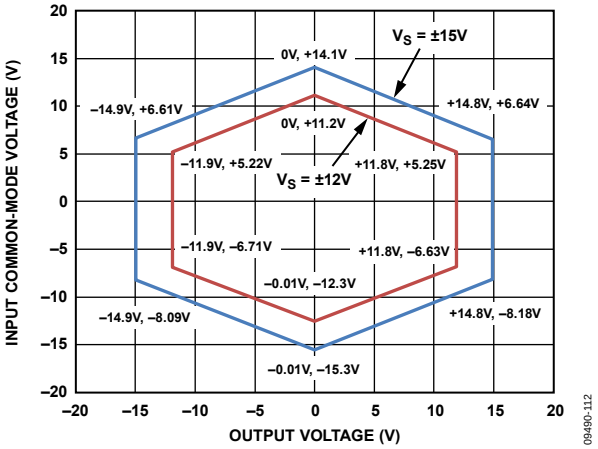


Figure 18. Input Common-Mode Voltage vs. Output Voltage, Dual Supply, V_S = ±15 V and V_S = ±12 V, G = 100

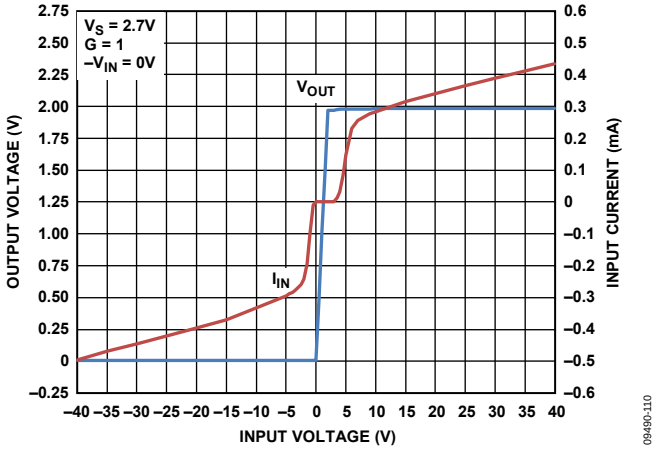


Figure 16. Input Overvoltage Performance, Single Supply, V_S = 2.7 V, G = 1

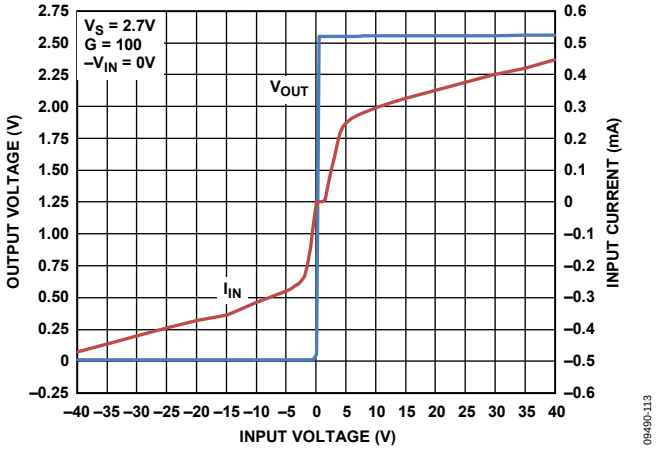


Figure 19. Input Overvoltage Performance, Single Supply, V_S = 2.7 V, G = 100

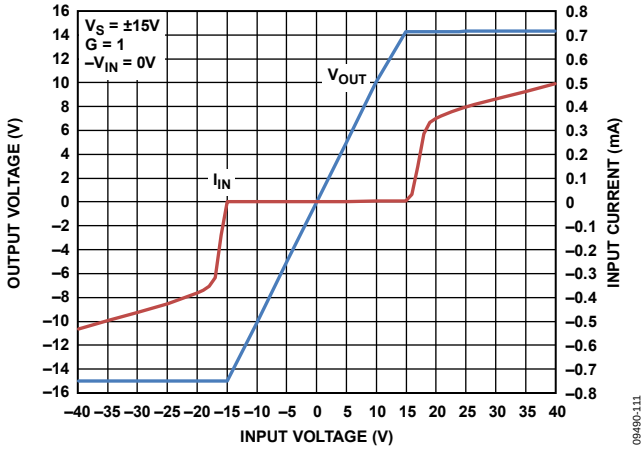


Figure 17. Input Overvoltage Performance, Dual Supply, V_S = ±15 V, G = 1

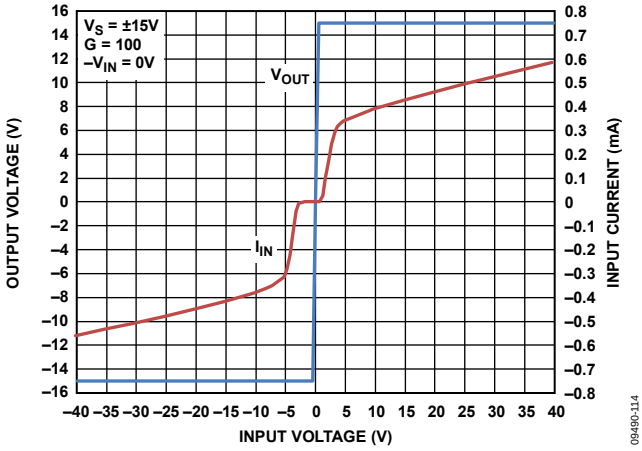


Figure 20. Input Overvoltage Performance, Dual Supply, V_S = ±15 V, G = 100

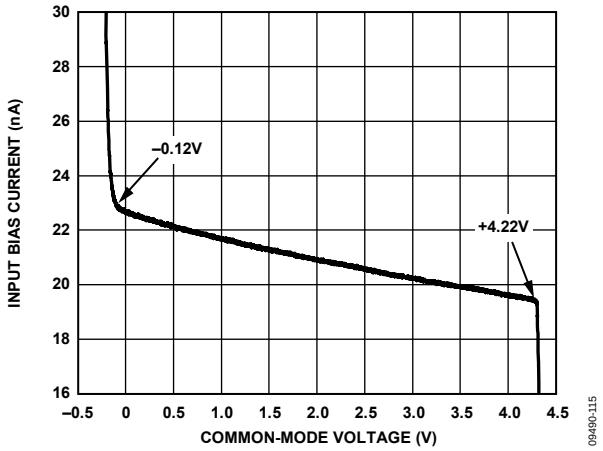


Figure 21. Input Bias Current vs. Common-Mode Voltage, Single Supply, V_S = 5 V

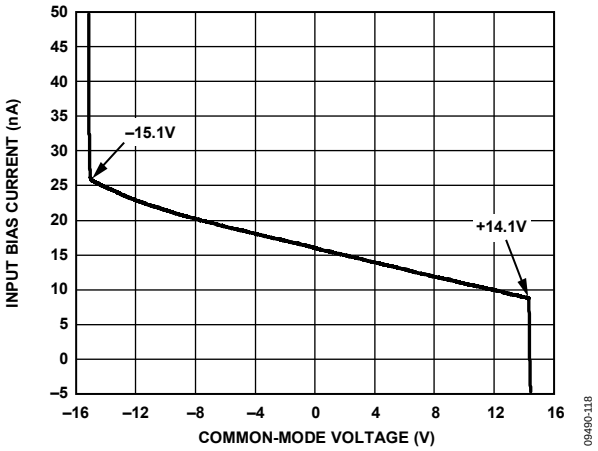


Figure 24. Input Bias Current vs. Common-Mode Voltage, Dual Supply, V_S = ±15 V

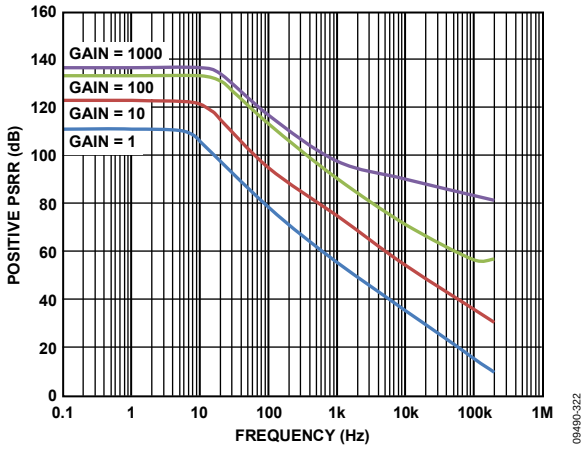


Figure 22. Positive PSRR vs. Frequency, RTI

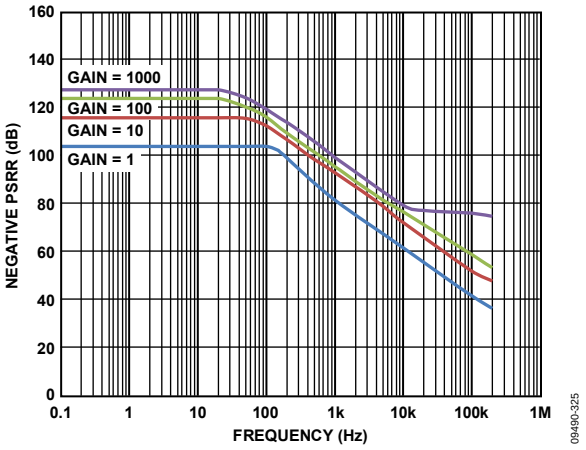


Figure 25. Negative PSRR vs. Frequency

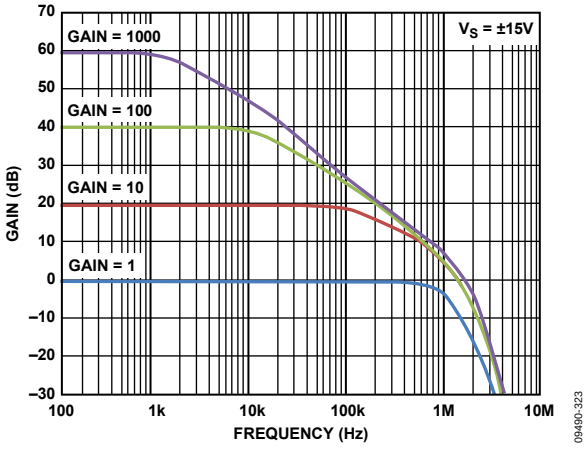


Figure 23. Gain vs. Frequency, Dual Supply, V_S = ±15 V

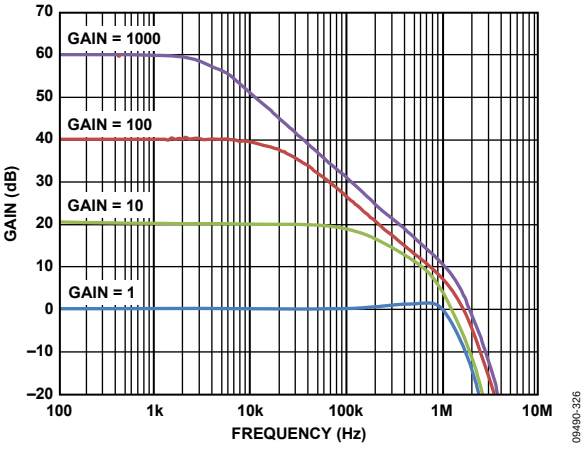


Figure 26. Gain vs. Frequency, Single Supply, V_S = 2.7 V

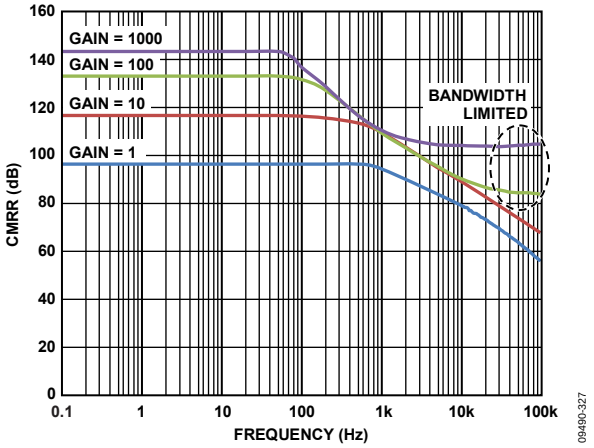


Figure 27. CMRR vs. Frequency, RTI

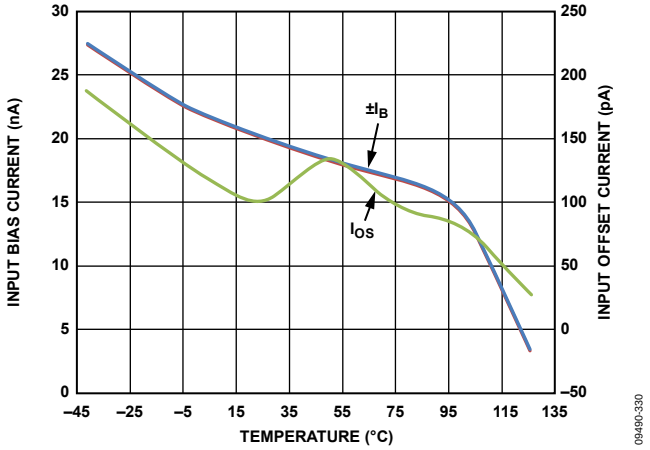


Figure 30. Input Bias Current and Input Offset Current vs. Temperature

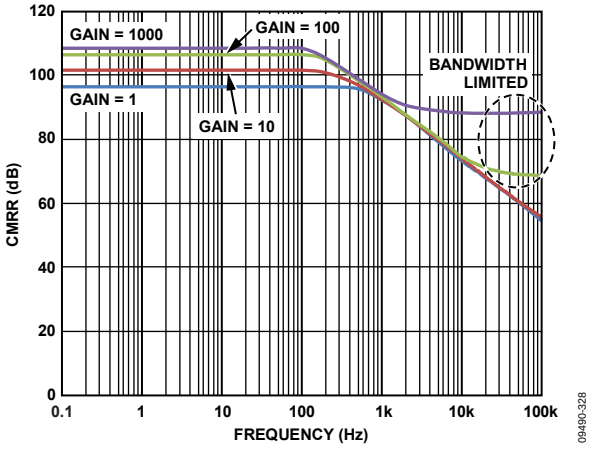


Figure 28. CMRR vs. Frequency, RTI, 1 kΩ Source Imbalance

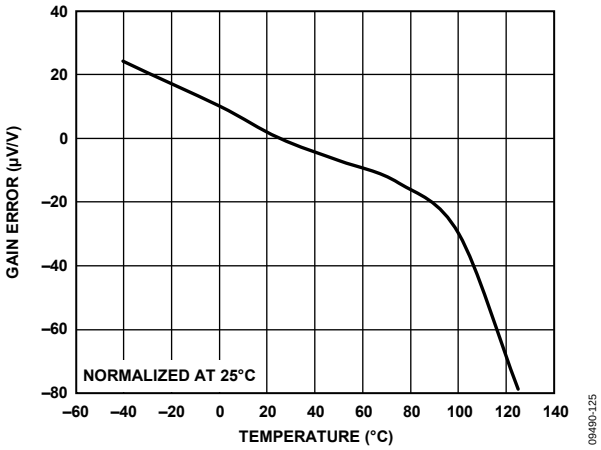


Figure 31. Gain Error vs. Temperature, G = 1

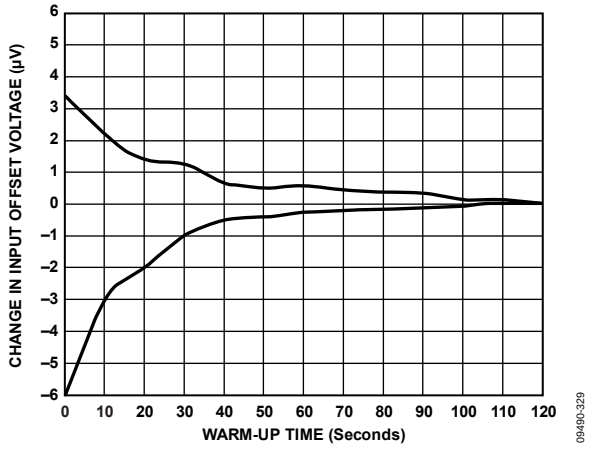


Figure 29. Change in Input Offset Voltage vs. Warm-Up Time

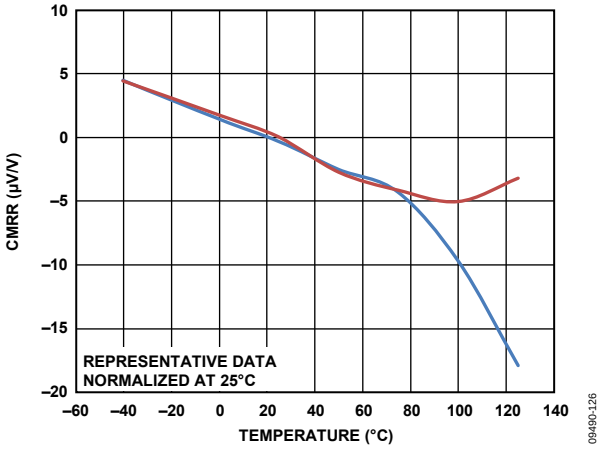


Figure 32. CMRR vs. Temperature, G = 1

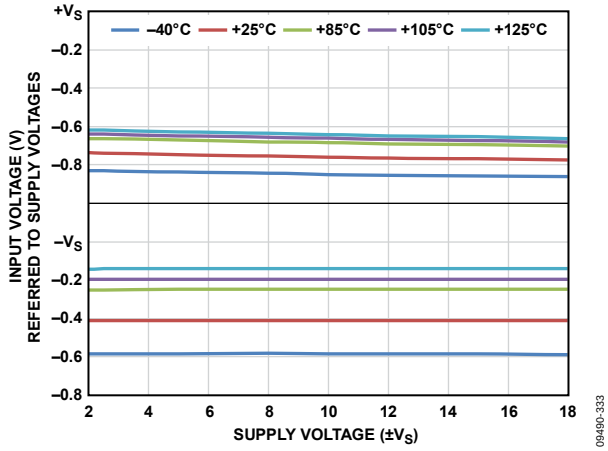


Figure 33. Input Voltage Limit vs. Supply Voltage

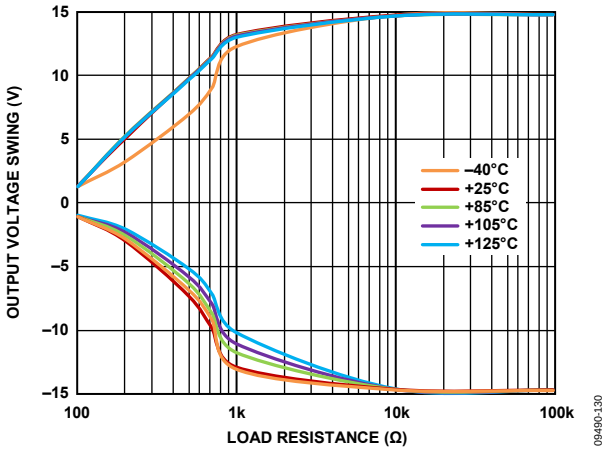


Figure 36. Output Voltage Swing vs. Load Resistance

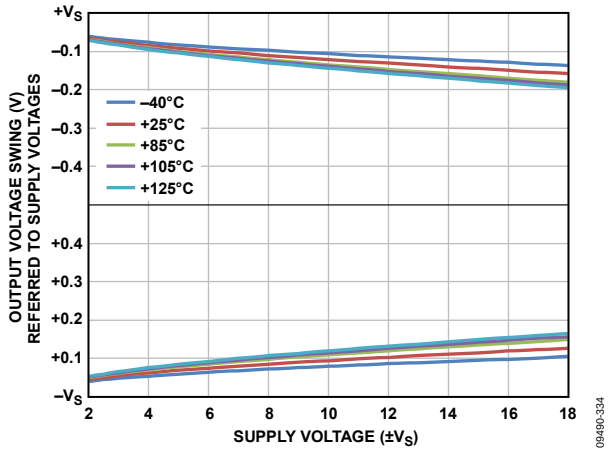


Figure 34. Output Voltage Swing vs. Supply Voltage, R_L = 10 kΩ

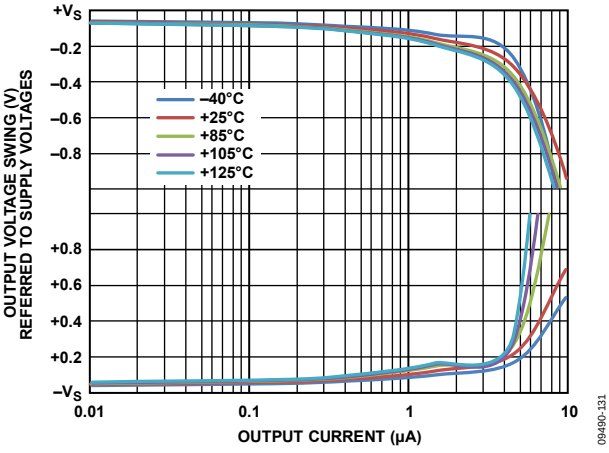


Figure 37. Output Voltage Swing vs. Output Current, G = 1

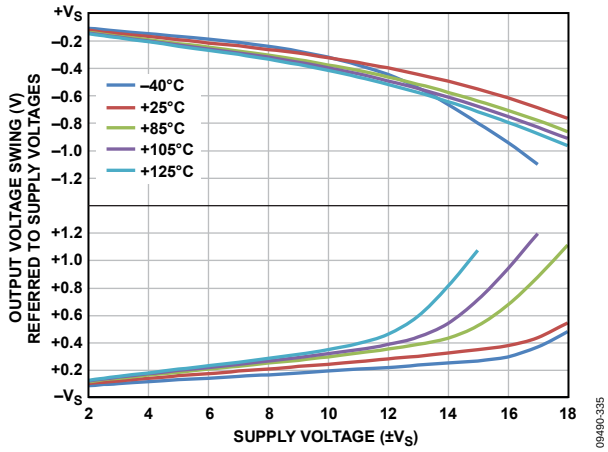


Figure 35. Output Voltage Swing vs. Supply Voltage, R_L = 2 kΩ

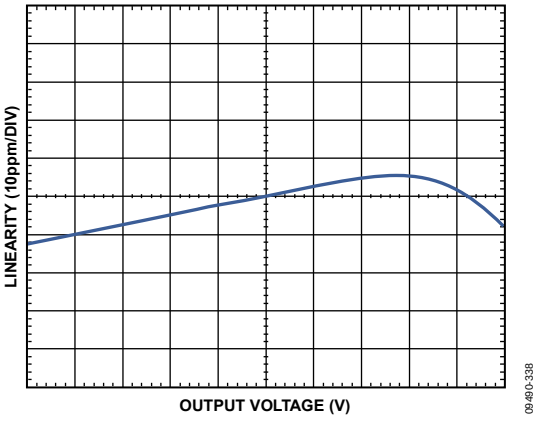


Figure 38. Gain Nonlinearity, R_L ≥ 10 kΩ, G = 1

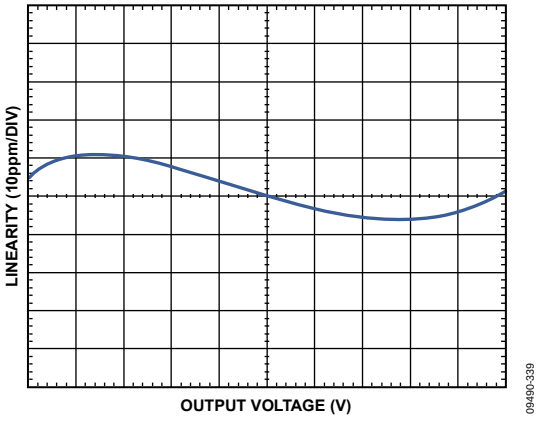


Figure 39. Gain Nonlinearity, $R_L \geq 10$ kΩ, G = 10

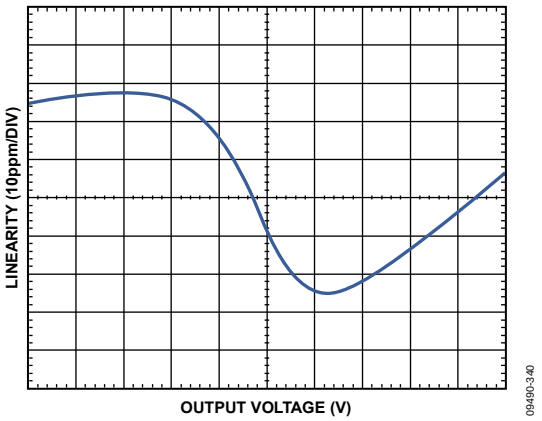


Figure 40. Gain Nonlinearity, $R_L \geq 10$ kΩ, G = 100

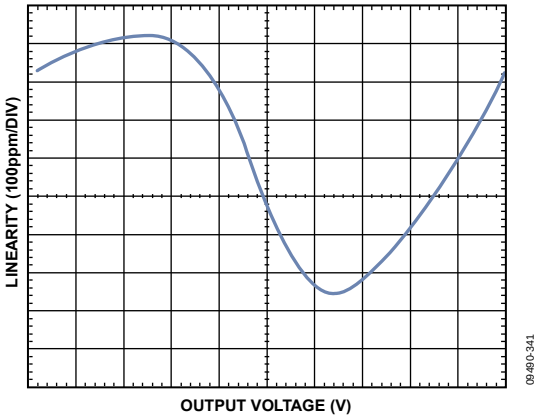


Figure 41. Gain Nonlinearity, $R_L \geq 10$ kΩ, G = 1000

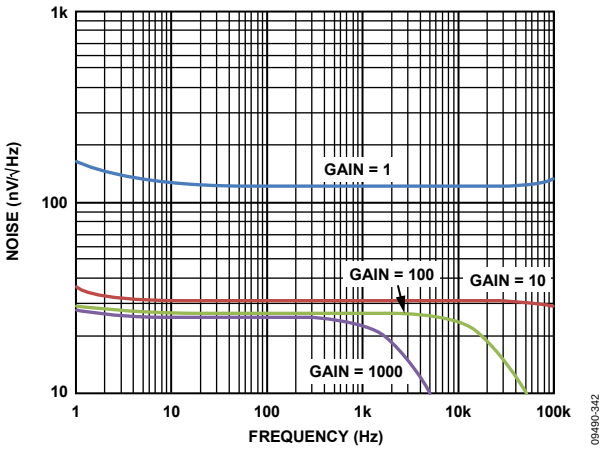


Figure 42. Voltage Noise Spectral Density vs. Frequency

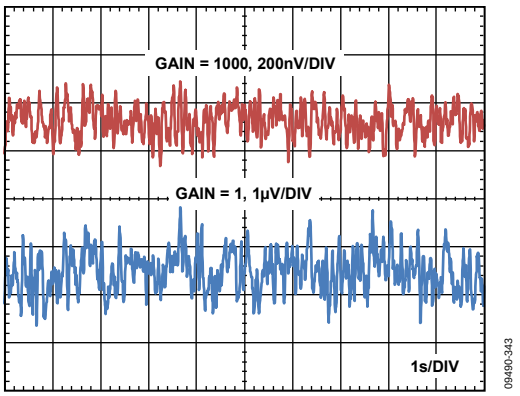


Figure 43. 0.1 Hz to 10 Hz RTI Voltage Noise, G = 1, G = 1000

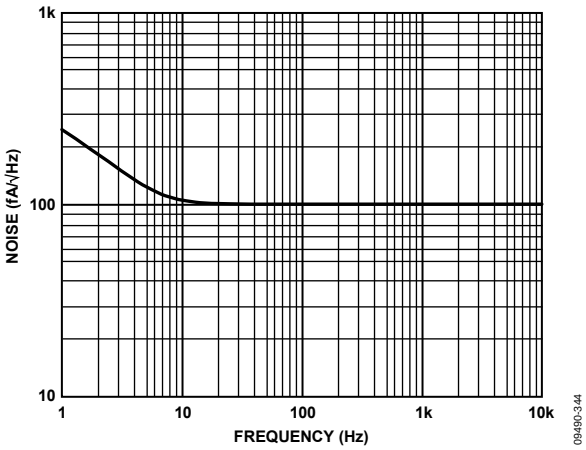


Figure 44. Current Noise Spectral Density vs. Frequency

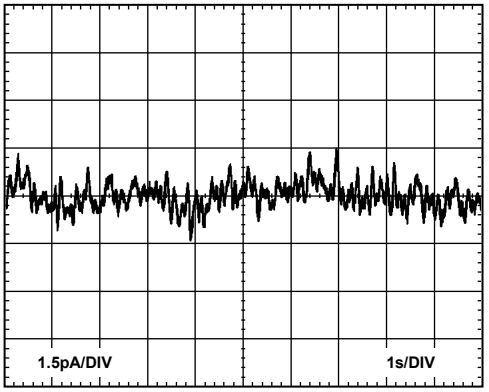


Figure 45. 0.1 Hz to 10 Hz Current Noise

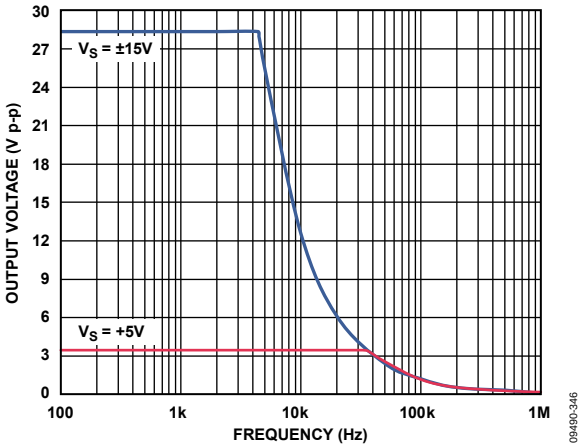


Figure 46. Large Signal Frequency Response

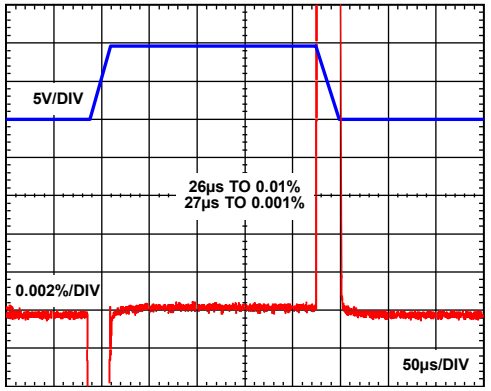


Figure 47. Large Signal Pulse Response and Settling Time, 10 V Step, Dual Supply, V_S = ±15 V, G = 1

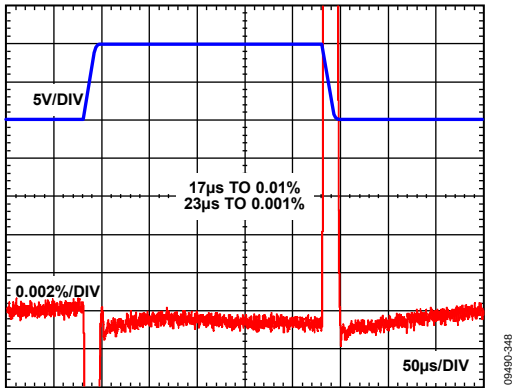


Figure 48. Large Signal Pulse Response and Settling Time, 10 V Step, Dual Supply, V_S = ±15 V, G = 10

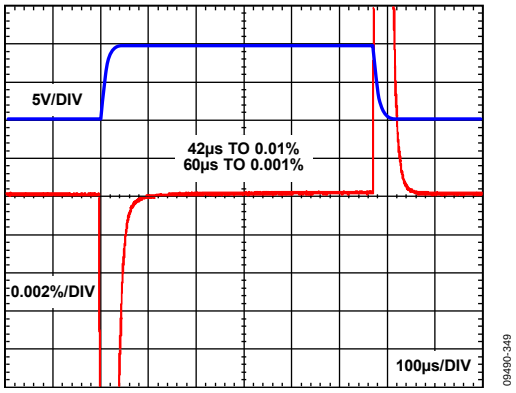


Figure 49. Large Signal Pulse Response and Settling Time, 10 V Step, Dual Supply, V_S = ±15 V, G = 100

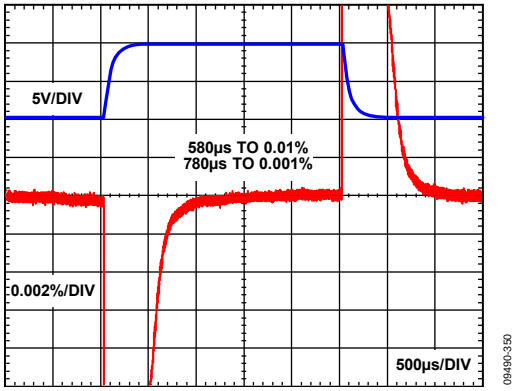


Figure 50. Large Signal Pulse Response and Settling Time, 10 V Step, Dual Supply, V_S = ±15 V, G = 1000

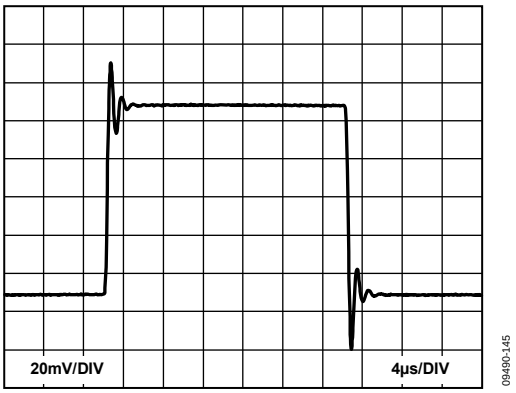


Figure 51. Small Signal Pulse Response, R_L = 10 kΩ, C_L = 100 pF, G = 1

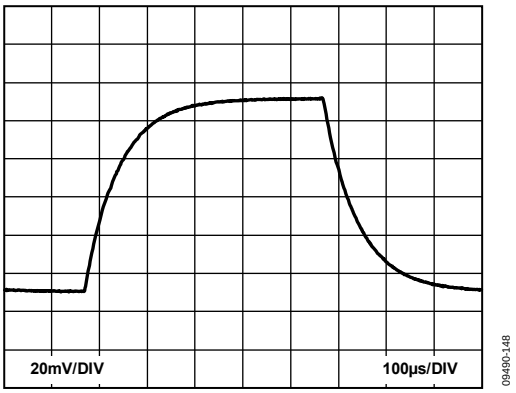


Figure 54. Small Signal Pulse Response, R_L = 10 kΩ, C_L = 100 pF, G = 1000

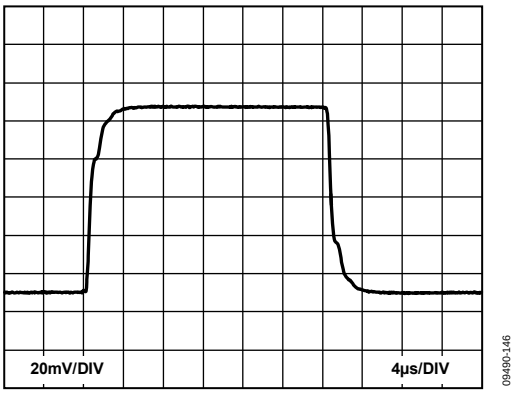


Figure 52. Small Signal Pulse Response, R_L = 10 kΩ, C_L = 100 pF, G = 10

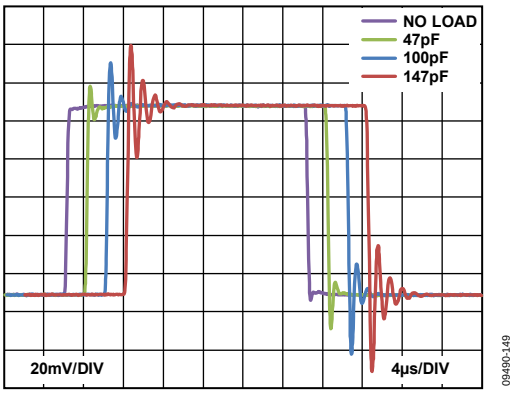


Figure 55. Small Signal Pulse Response with Various Capacitive Loads, G = 1, R_L = Infinity

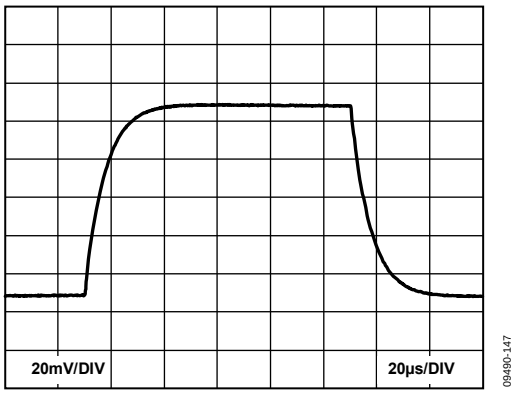


Figure 53. Small Signal Pulse Response, R_L = 10 kΩ, C_L = 100 pF, G = 100

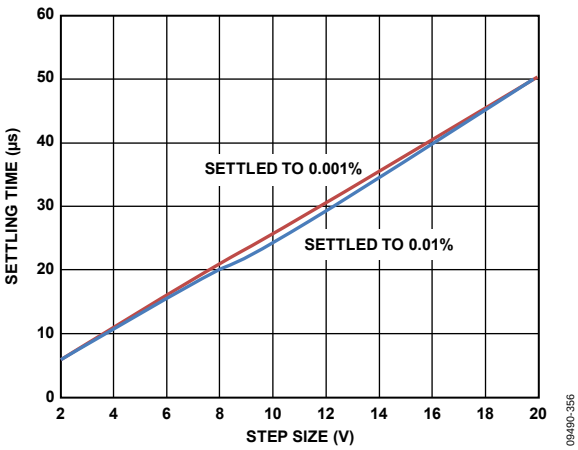


Figure 56. Settling Time vs. Step Size, Dual Supply, V_S = ±15 V

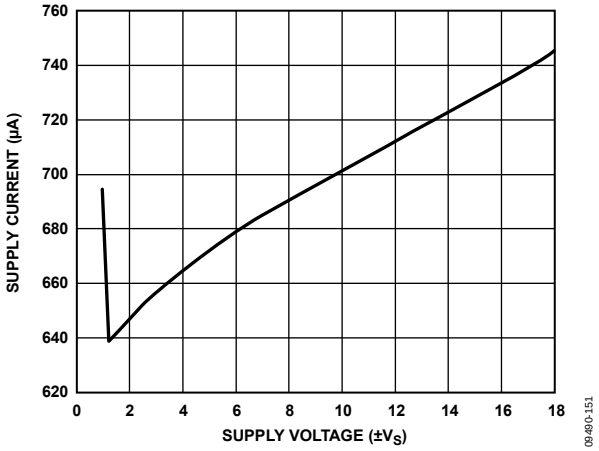


Figure 57. Supply Current vs. Supply Voltage (Both Amplifiers)

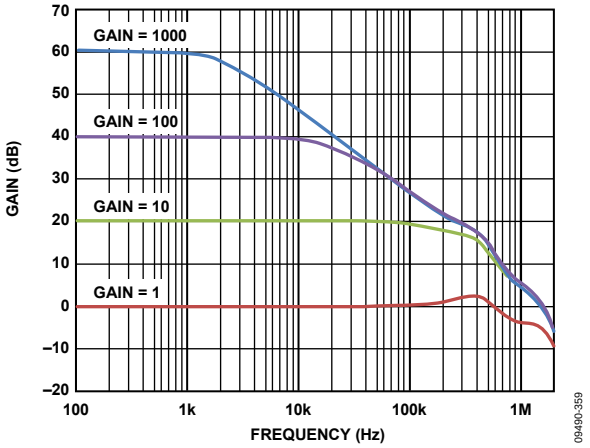


Figure 59. Gain vs. Frequency, Differential Output Configuration

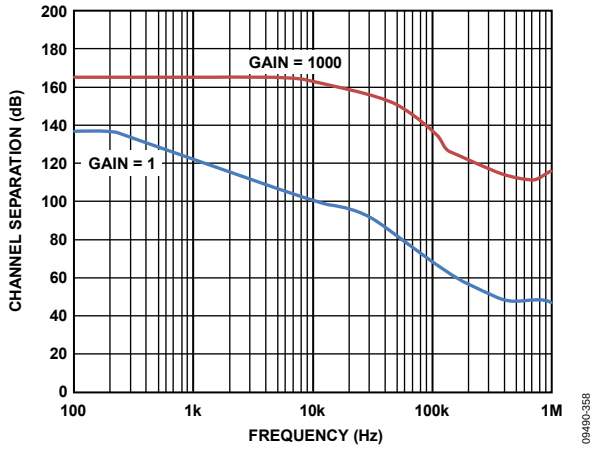


Figure 58. Channel Separation vs. Frequency, R_L = 2 kΩ, Source Channel at G = 1 and G = 1000

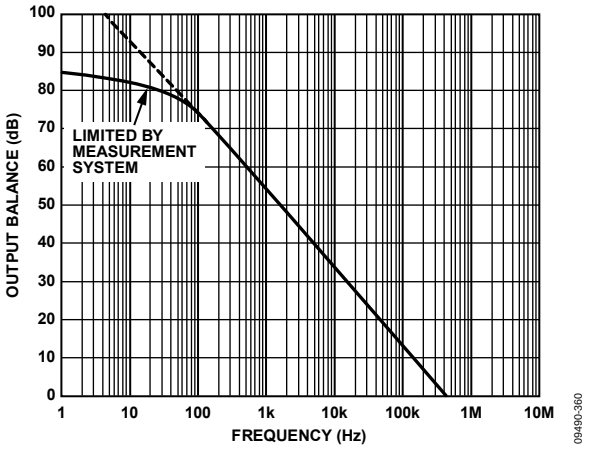


Figure 60. Output Balance vs. Frequency, Differential Output Configuration

THEORY OF OPERATION

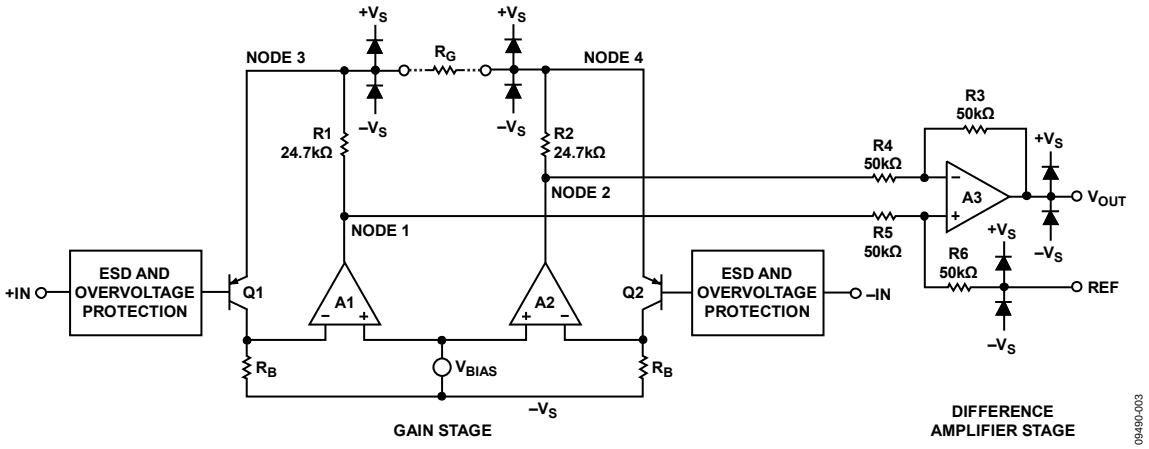


Figure 61. Simplified Schematic

ARCHITECTURE

The AD8426 is based on the classic 3-op-amp topology. This topology has two stages: a gain stage (preamplifier) to provide differential amplification, followed by a difference amplifier stage to remove the common-mode voltage. Figure 61 shows a simplified schematic of one of the instrumentation amplifiers in the AD8426.

The first stage works as follows. To maintain a constant voltage across the bias resistor, R_B, A1 must keep Node 3 at a constant diode drop above the positive input voltage. Similarly, A2 keeps Node 4 at a constant diode drop above the negative input voltage. Therefore, a replica of the differential input voltage is placed across the gain setting resistor, R_G. The current that flows across this resistance must also flow through the R1 and R2 resistors, creating a gained differential signal between the A2 and A1 outputs. Note that, in addition to a gained differential signal, the original common-mode signal, shifted up by a diode drop, is also still present.

The second stage is a difference amplifier, composed of A3 and four 50 kΩ resistors. The purpose of this stage is to remove the common-mode signal from the amplified differential signal.

The transfer function of the AD8426 is

$$V_{OUT} = G \times (V_{IN+} - V_{IN-}) + V_{REF}$$

where:

$$G = 1 + \frac{49.4\ \text{k}\Omega}{R_G}$$

GAIN SELECTION

Placing a resistor across the R_G terminals sets the gain of the AD8426. The gain can be calculated by referring to Table 11 or by using the following gain equation:

$$R_G = \frac{49.4\ \text{k}\Omega}{G - 1}$$

Table 11. Gains Achieved Using 1% Resistors

1% Standard Table Value of R_G	Calculated Gain
49.9 kΩ	1.990
12.4 kΩ	4.984
5.49 kΩ	9.998
2.61 kΩ	19.93
1.00 kΩ	50.40
499 Ω	100.0
249 Ω	199.4
100 Ω	495.0
49.9 Ω	991.0

The AD8426 defaults to G = 1 when no gain resistor is used. The tolerance and gain drift of the R_G resistor should be added to the AD8426 specifications to determine the total gain accuracy of the system. When the gain resistor is not used, gain error and gain drift are minimal.

REFERENCE TERMINAL

The output voltage of the AD8426 is developed with respect to the potential on the reference terminal. This is useful when the output signal needs to be offset to a precise midsupply level. For example, a voltage source can be tied to the REF pin to level-shift the output so that the AD8426 can drive a single-supply ADC. The REF pin is protected with ESD diodes and should not exceed either $+V_S$ or $-V_S$ by more than 0.3 V.

For the best performance, source impedance to the REF terminal should be kept below 2 Ω. As shown in Figure 62, the reference terminal, REF, is at one end of a 50 kΩ resistor. Additional impedance at the REF terminal adds to this 50 kΩ resistor and results in amplification of the signal connected to the positive input. The amplification from the additional R_{REF} can be computed by $2 \times (50\ k\Omega + R_{REF})/100\ k\Omega + R_{REF}$.

Only the positive signal path is amplified; the negative path is unaffected. This uneven amplification degrades the CMRR of the amplifier.

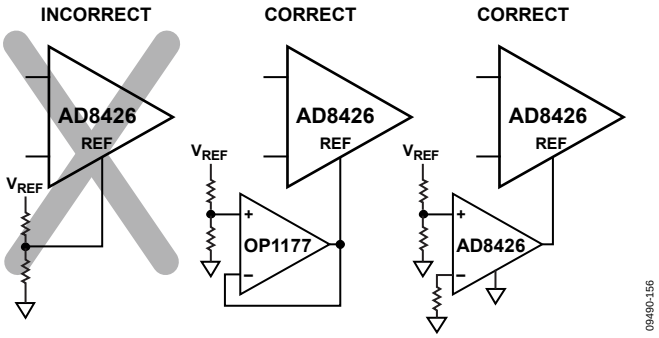


Figure 62. Driving the Reference Pin

INPUT VOLTAGE RANGE

The 3-op-amp architecture of the AD8426 applies gain in the first stage before removing common-mode voltage in the difference amplifier stage. In addition, the input transistors in the first stage shift the common-mode voltage up one diode drop. Therefore, internal nodes between the first and second stages (Node 1 and Node 2 in Figure 61) experience a combination of gained signal, common-mode signal, and a diode drop. This combined signal can be limited by the voltage supplies even when the individual input and output signals are not limited. Figure 9 to Figure 15 and Figure 18 show the allowable common-mode input voltage ranges for various output voltages and supply voltages.

Equation 1 to Equation 3 can be used to understand the interaction of the gain (G), common-mode input voltage (V_{CM}), differential input voltage (V_{DIFF}), and reference voltage (V_{REF}). The values for the constants (V_{-LIMIT}, V_{+LIMIT}, and V_{REF_LIMIT}) at different temperatures are shown in Table 12. These three equations, along with the input and output voltage range specifications in Table 2 and Table 5, set the operating boundaries of the part.

$$V_{CM} - \left| \frac{V_{DIFF} \times G}{2} \right| > -V_S + V_{-LIMIT} \quad (1)$$

$$V_{CM} + \left| \frac{V_{DIFF} \times G}{2} \right| < +V_S - V_{+LIMIT} \quad (2)$$

$$\left(\frac{\frac{V_{DIFF} \times G}{2} + V_{CM} + V_{REF}}{2} \right) < +V_S - V_{REF\_LIMIT} \quad (3)$$

Table 12. Input Voltage Range Constants for Various Temperatures

Temperature	V_{-LIMIT} (V)	V_{+LIMIT} (V)	V_{REF_LIMIT} (V)
−40°C	−0.55	+0.8	+1.3
+25°C	−0.35	+0.7	+1.15
+85°C	−0.15	+0.65	+1.05
+125°C	−0.05	+0.6	+0.9

The common-mode input voltage range shifts upward with temperature. At cold temperatures, the part requires extra headroom from the positive supply, whereas operation near the negative supply has more margin. Conversely, at hot temperatures, the part requires less headroom from the positive supply but is subject to the worst-case conditions for input voltages near the negative supply.

A typical part functions up to the boundaries described in this section. However, for best performance, designing with a few hundred millivolts of extra margin is recommended. As signals approach the boundary, internal transistors begin to saturate, which can affect frequency and linearity performance.

LAYOUT

To ensure optimum performance of the AD8426 at the PCB level, care must be taken in the design of the board layout. The AD8426 pins are arranged in a logical manner to aid in this task.

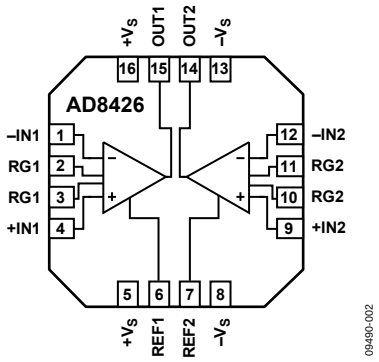


Figure 63. Pinout Diagram

Package Considerations

The AD8426 is available in a 16-lead, 4 mm × 4 mm LFCSP with no exposed paddle. The footprint from another 4 mm × 4 mm LFCSP part should not be copied because it may not have the correct lead pitch and lead width dimensions. Refer to the Outline Dimensions section to verify that the corresponding dimensional symbol has the correct dimensions.

Hidden Paddle Package

The AD8426 is available in an LFCSP package with a hidden paddle. Unlike chip scale packages where the pad limits routing capability, this package allows routes and vias directly beneath the chip. In this way, the full space savings of the small LFCSP can be realized. Although the package has no metal in the center of the part, the manufacturing process leaves a very small section of exposed metal at each of the package corners, as shown in Figure 64 and in Figure 73 in the Outline Dimensions section. This metal is connected to $-V_S$ through the part. Because of the possibility of a short, vias should not be placed beneath these exposed metal tabs.

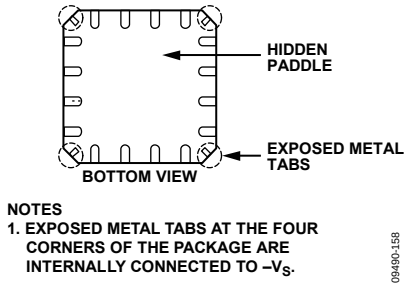


Figure 64. Hidden Paddle Package, Bottom View

Common-Mode Rejection Ratio over Frequency

Poor layout can cause some of the common-mode signals to be converted to differential signals before reaching the in-amp. Such conversions occur when one input path has a frequency response that is different from the other. To keep CMRR over frequency high, the input source impedance and capacitance of each path should be closely matched. Additional source resistance in the input paths (for example, for input protection) should be placed close to the in-amp inputs to minimize the interaction of the inputs with parasitic capacitance from the PCB traces.

Parasitic capacitance at the gain setting pins can also affect CMRR over frequency. If the board design has a component at the gain setting pins (for example, a switch or jumper), the component should be chosen so that the parasitic capacitance is as small as possible.

Power Supplies

A stable dc voltage should be used to power the instrumentation amplifier. Noise on the supply pins can adversely affect performance. See the PSRR performance curves in Figure 22 and Figure 25 for more information.

A 0.1 µF capacitor should be placed as close as possible to each supply pin. As shown in Figure 65, a 10 µF capacitor can be used farther away from the part. In most cases, it can be shared by other precision integrated circuits.

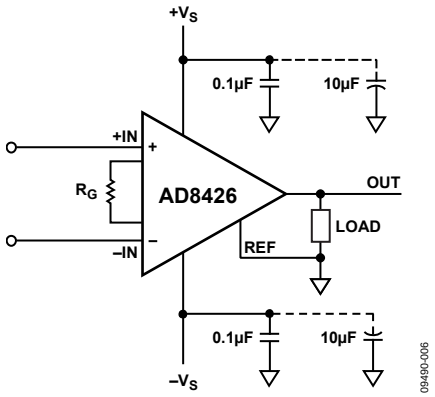


Figure 65. Supply Decoupling, REF, and Output Referred to Local Ground

References

The output voltage of the AD8426 is developed with respect to the potential on the reference terminal. Care should be taken to tie the REFx pins to the appropriate local ground. This should also help minimize crosstalk between the two channels.

INPUT BIAS CURRENT RETURN PATH

The input bias current of the AD8426 must have a return path to ground. When the source, such as a thermocouple, cannot provide a current return path, one should be created, as shown in Figure 66.

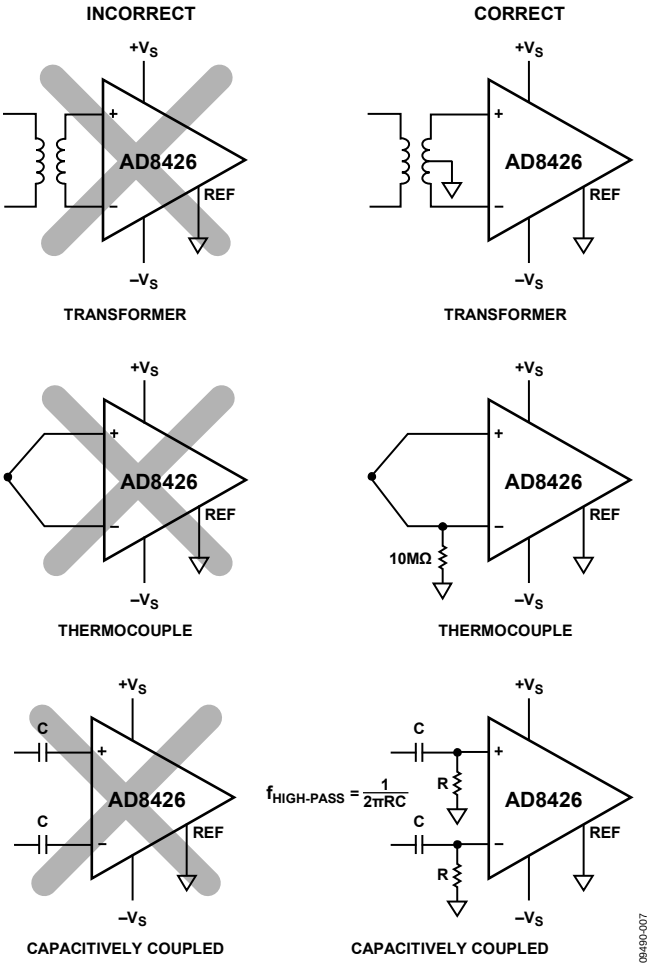


Figure 66. Creating an Input Bias Current Return Path

INPUT PROTECTION

The AD8426 has very robust inputs and typically does not need additional input protection. Input voltages can be up to 40 V from the opposite supply rail. For example, with a +5 V positive supply and a −8 V negative supply, the part can safely withstand voltages from −35 V to +32 V. Unlike some other instrumentation amplifiers, the part can handle large differential input voltages even when the part is in high gain. Figure 16, Figure 17, Figure 19, and Figure 20 show the behavior of the part under overvoltage conditions.

The other AD8426 terminals should be kept within the supplies. All terminals of the AD8426 are protected against ESD.

For applications where the AD8426 encounters voltages beyond the allowed limits, external current limiting resistors and low leakage diode clamps such as the BAV199L, the FJH1100, or the SP720 should be used.

RADIO FREQUENCY INTERFERENCE (RFI)

RF interference is often a problem when amplifiers are used in applications where there are strong RF signals. The precision circuits in the AD8426 can rectify the RF signals so that they appear as a dc offset voltage error. To avoid this rectification, place a low-pass RC filter at the input of the instrumentation amplifier (see Figure 67). The filter limits both the differential and common-mode bandwidth, as shown in the following equations:

$$FilterFrequency_{DIFF} = \frac{1}{2\pi R(2C_D + C_C)}$$

$$FilterFrequency_{CM} = \frac{1}{2\pi RC_C}$$

where $C_D \geq 10\ C_C$.

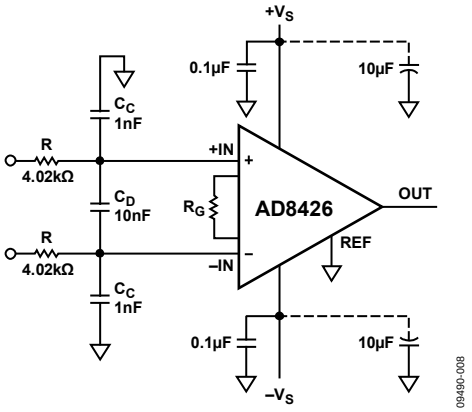


Figure 67. RFI Suppression

C_D affects the differential signal, and C_C affects the common-mode signal. Values of R and C_C should be chosen to minimize RFI. Any mismatch between the R × C_C at the positive input and the R × C_C at the negative input degrades the CMRR of the AD8426. By using a value of C_D one order of magnitude larger than C_C, the effect of the mismatch is reduced, and performance is improved.

APPLICATIONS INFORMATION

PRECISION STRAIN GAGE

The low offset and high CMRR over frequency of the AD8426 make it an excellent candidate for bridge measurements. The bridge can be connected directly to the inputs of the amplifier (see Figure 68).

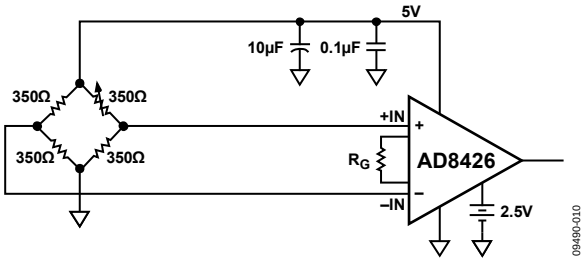


Figure 68. Precision Strain Gage

DIFFERENTIAL DRIVE

The differential output configuration of the AD8426 has the same excellent dc precision specifications as the single-ended output configuration.

Differential Output Using Both AD8426 Amplifiers

The circuit configuration is shown in Figure 69. The differential output specifications in Table 2, Table 4, Table 5, and Table 7 refer to this configuration only. The circuit includes an RC filter that maintains the stability of the loop.

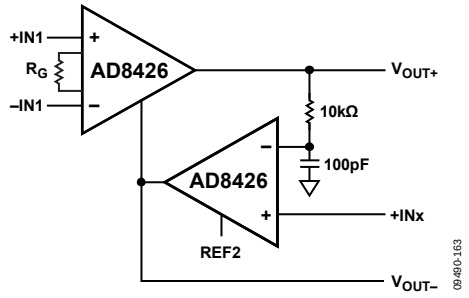


Figure 69. Differential Circuit Schematic

The differential output voltage is set by the following equation:

$$V_{DIFF\_OUT} = V_{OUT+} - V_{OUT-} = G \times (V_{IN+} - V_{IN-})$$

where:

$$G = 1 + \frac{49.4\,\text{k}\Omega}{R_G}$$

The common-mode output voltage is set by the average of +IN2 and REF2. The transfer function is

$$V_{CM\_OUT} = (V_{OUT+} + V_{OUT-})/2 = (V_{+IN2} + V_{REF2})/2$$

A common application sets the common-mode output voltage to the midscale of a differential ADC. In this case, the ADC reference voltage is sent to the +IN2 terminal, and ground is connected to the REF2 terminal. This produces a common-mode output voltage of half the ADC reference voltage.

2-Channel Differential Output Using a Dual Op Amp

Another differential output topology is shown in Figure 70. Instead of a second in-amp, one-half of a dual op amp creates the inverted output. The recommended dual op amps (the AD8642 and the AD822) are packaged in an MSOP. This configuration allows the creation of a dual-channel, precision differential output in-amp with little board area.

Figure 70 shows how to configure the AD8426 for differential output.

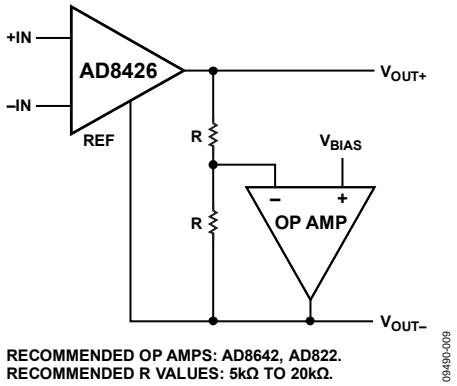


Figure 70. Differential Output Using an Op Amp

The differential output voltage is set by the following equation:

$$V_{DIFF\_OUT} = V_{OUT+} - V_{OUT-} = G \times (V_{IN+} - V_{IN-})$$

where:

$$G = 1 + \frac{49.4\,\text{k}\Omega}{R_G}$$

The common-mode output voltage is set by the following equation:

$$V_{CM\_OUT} = (V_{OUT+} - V_{OUT-})/2 = V_{BIAS}$$

The advantage of this circuit is that the dc differential accuracy depends on the AD8426 and not on the op amp or the resistors. This circuit takes advantage of the precise control of the AD8426 over its output voltage relative to the reference voltage. Op amp dc performance and resistor matching do affect the dc common-mode output accuracy. However, because common-mode errors are likely to be rejected by the next device in the signal chain, these errors typically have little effect on overall system accuracy.

For best ac performance, an op amp with gain bandwidth of at least 2 MHz and a slew rate of at least 1 V/µs is recommended. Good choices for op amps are the AD8642 and the AD822.

Tips for Best Differential Output Performance

Keep trace lengths from resistors to the inverting terminal of the op amp as short as possible. Excessive capacitance at this node can cause the circuit to be unstable. If capacitance cannot be avoided, use lower value resistors.

For best linearity and ac performance, a minimum positive supply voltage ($+V_S$) is required. Table 13 shows the minimum supply voltage required for optimum performance, where V_{CM_MAX} indicates the maximum common-mode voltage expected at the input of the AD8426.

Table 13. Minimum Positive Supply Voltage

Temperature	Equation
Less than −10°C	$+V_S > (V_{CM\_MAX} + V_{BIAS})/2 + 1.4$ V
−10°C to +25°C	$+V_S > (V_{CM\_MAX} + V_{BIAS})/2 + 1.25$ V
More than +25°C	$+V_S > (V_{CM\_MAX} + V_{BIAS})/2 + 1.1$ V

DRIVING A CABLE

All cables have a certain capacitance per unit length, which varies widely with cable type. The capacitive load from the cable may cause peaking in the output response of the AD8426. To reduce the peaking, use a resistor between the AD8426 outputs and the cable (see Figure 71). Because cable capacitance and desired output response vary widely, this resistor is best determined empirically. A good starting point is 50 Ω.

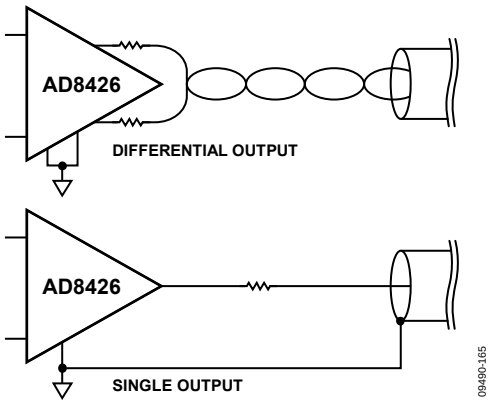


Figure 71. Driving a Cable

The AD8426 operates at such a relatively low frequency that transmission line effects are rarely an issue; therefore, the resistor need not match the characteristic impedance of the cable.

DRIVING AN ADC

Figure 72 shows several different methods of driving an ADC. The ADC in the ADuC7026 microcontroller was chosen for this example because it has an unbuffered, charge sampling architecture that is typical of most modern ADCs. This type of architecture typically requires an RC buffer stage between the ADC and the amplifier to work correctly.

Option 1 shows the minimum configuration required to drive a charge sampling ADC. The capacitor provides charge to the ADC sampling capacitor, and the resistor shields the AD8426 from the capacitance. To keep the AD8426 stable, the RC time constant of the resistor and capacitor needs to stay above 5 µs. This circuit is mainly useful for lower frequency signals.

Option 2 shows a circuit for driving higher frequency signals. It uses a precision op amp (AD8616) with relatively high bandwidth and output drive. This amplifier can drive a resistor and capacitor with a much higher time constant and is, therefore, suited for higher frequency applications.

Option 3 is useful for applications where the AD8426 must operate from a large voltage supply but drives a single-supply ADC. In normal operation, the AD8426 output signal stays within the ADC range, and the AD8616 simply buffers the signal. However, in a fault condition, the output of the AD8426 may go outside the supply range of both the AD8616 and the ADC. This is not a problem in this circuit, because the 10 kΩ resistor between the two amplifiers limits the current into the AD8616 to a safe level.

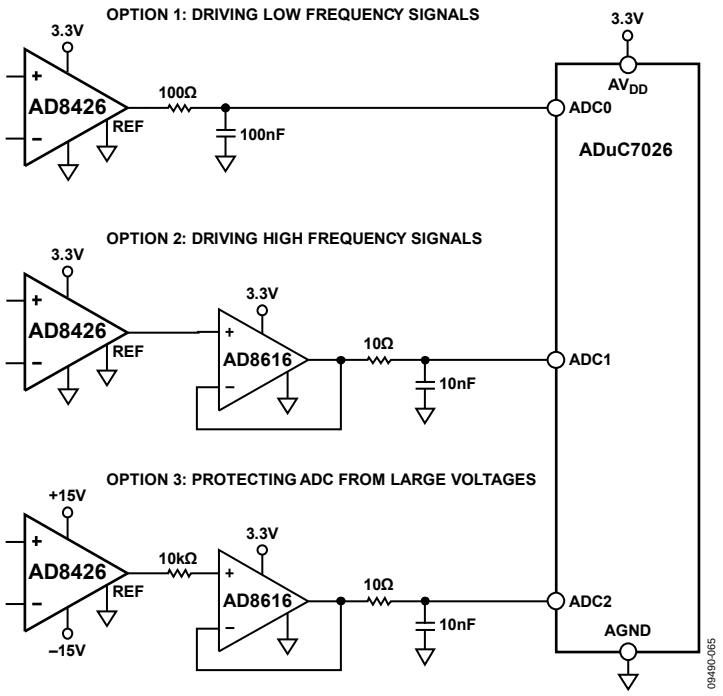
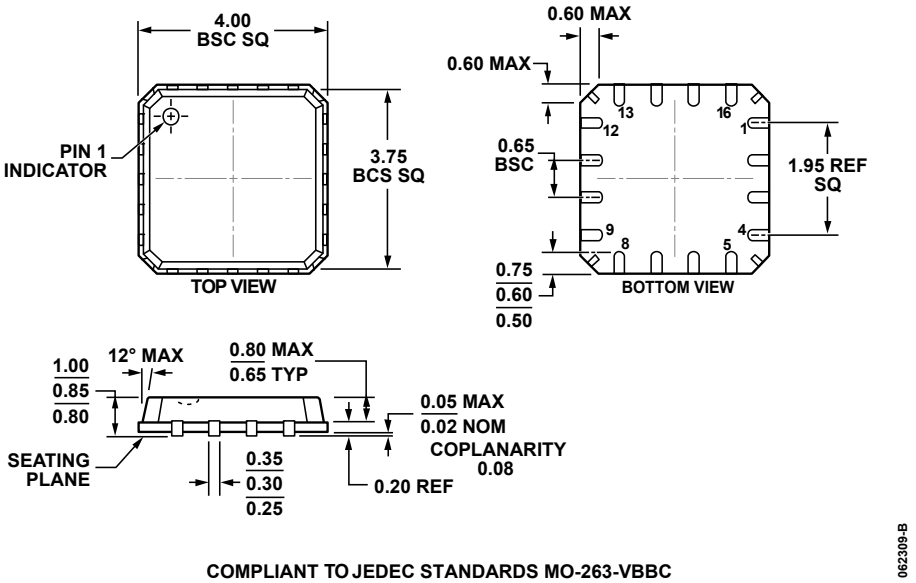


Figure 72. Driving an ADC

OUTLINE DIMENSIONS



COMPLIANT TO JEDEC STANDARDS MO-263-VBBC

Figure 73. 16-Lead Lead Frame Chip Scale Package [LFCSP_VQ]
4 mm × 4 mm Body, Very Thin Quad, with Hidden Paddle
(CP-16-19)
Dimensions shown in millimeters

ORDERING GUIDE

Model[1]	Temperature Range	Package Description	Package Option
AD8426ACPZ-R7	−40°C to +125°C	16-Lead Lead Frame Chip Scale Package [LFCSP_VQ]	CP-16-19
AD8426ACPZ-WP	−40°C to +125°C	16-Lead Lead Frame Chip Scale Package [LFCSP_VQ]	CP-16-19
AD8426BCPZ-R7	−40°C to +125°C	16-Lead Lead Frame Chip Scale Package [LFCSP_VQ]	CP-16-19
AD8426BCPZ-WP	−40°C to +125°C	16-Lead Lead Frame Chip Scale Package [LFCSP_VQ]	CP-16-19

[1] Z = RoHS Compliant Part.