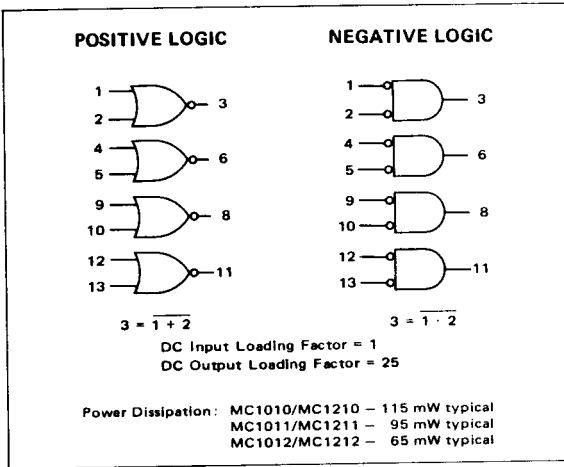


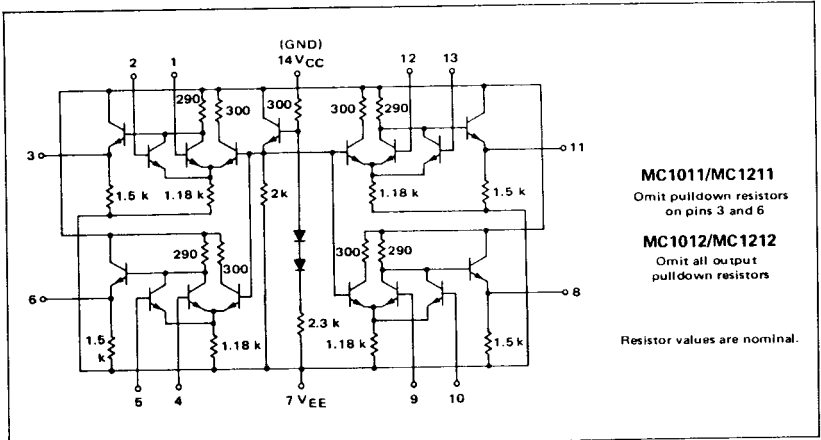
**MC1010 thru MC1012
MC1210 thru MC1212**

Provide the NOR output function. These devices contain an internal bias reference insuring that the threshold point is always in the center of the transition region over the temperature range.

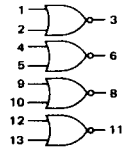
Emitter follower output configurations differ for these three circuits as shown in the circuit schematic.



MC1010/MC1210 CIRCUIT SCHEMATIC



MC1010 thru MC1012, MC1210 thru MC1212 (continued)



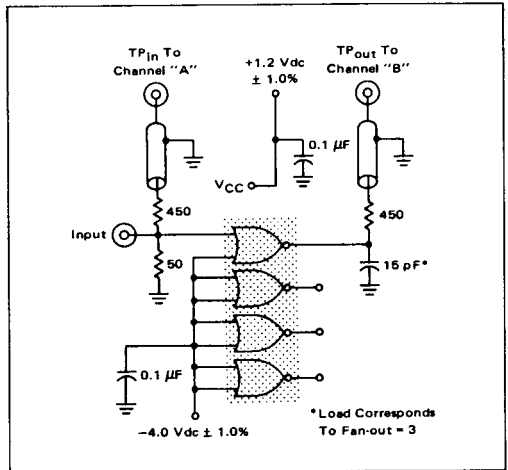
ELECTRICAL CHARACTERISTICS

Test procedures are shown for only one gate. The other gates are tested in the same manner. Outputs without pull-down resistors are tested with a 1.5 kΩ resistor to VEE.

Characteristic	Symbol	Pin Under Test	MC1210-1212 Test Limits						MC1010-1012 Test Limits								
			-55°C		+25°C		+125°C		0°C		+25°C		+75°C		Unit		
			Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max			
Power Supply Drain Current MC1210, MC1010 MC1211, MC1011 MC1212, MC1012	I_E	7	-	-	-	32	-	-	-	-	-	-	-	32	-	-	mAdc
Input Current	I_{in}	1 2	-	-	-	100	-	-	-	-	-	-	-	100	-	-	μAdc
Input Leakage Current	I_R	Inputs*	-	-	-	0.2	-	1.0	μAdc	-	-	-	0.2	-	1.0	μAdc	
"NOR" Logical "1" Output Voltage	V_{OH1}	3	-0.990	-0.825	-0.850	-0.700	-0.700	-0.530	Vdc	-0.895	-0.740	-0.850	-0.700	-0.775	-0.615	Vdc	
"NOR" Logical "0" Output Voltage	V_{OL}	3	-1.890	-1.580	-1.800	-1.500	-1.720	-1.380	Vdc	-1.830	-1.525	-1.800	-1.500	-1.760	-1.435	Vdc	
Switching Times Propagation Delay (Fan-Out = 3)	t_{1-3+}	3	Typ	Max	Typ	Max	Typ	Max	ns	Typ	Max	Typ	Max	Typ	Max	ns	
			4.0	7.5	4.5	7.5	6.0	9.0		4.0	7.5	4.5	7.5	5.5	8.5		
			5.0	7.0	5.0	7.0	6.0	9.0		5.0	7.0	5.0	7.0	5.5	8.0		
			18	-	18	-	22	-		18	-	18	-	20	-		
Rise Time (Fan-Out = 3)	t_{3+}	3	4.0	7.5	4.0	7.0	5.0	8.0	4.0	7.0	4.0	7.0	4.5	7.5			
			6.0	-	6.0	-	9.0	-	6.0	-	6.0	-	7.0	-			
Fall Time (Fan-Out = 3)	t_{3-}	3	6.0	8.5	6.0	8.0	7.0	10	6.0	8.0	6.0	8.0	6.5	9.0			

* Individually test each input using the pin connections shown.
 V_{OH} limits apply from no load (0 mA) to full load (-2.5 mA).

SWITCHING TIME TEST CIRCUIT @ 25°C



@ Test Temperature

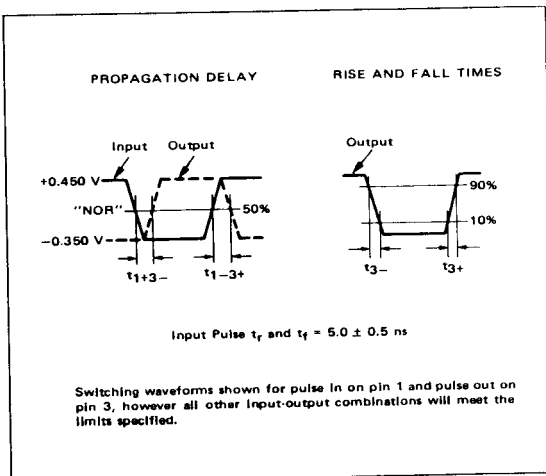
MC1210-1212

MC1010-1012

TEST VOLTAGE/CURRENT VALUES					
Vdc ± 1.0%					mAdc
V _{IL min} to V _{IL max}	V _{IH min} to V _{IH max}	V _{IH max}	V _{EE}	I _L	
-5.2 to -1.405	-1.165 to -0.825	-	-5.2	-	-2.5
-5.2 to -1.325	-1.025 to -0.700	-0.700	-5.2	-	-2.5
-5.2 to -1.205	-0.875 to -0.530	-	-5.2	-	-2.5
-5.2 to -1.350	-1.070 to -0.740	-	-5.2	-	-2.5
-5.2 to -1.325	-1.025 to -0.700	-0.700	-5.2	-	-2.5
-5.2 to -1.260	-0.950 to -0.615	-	-5.2	-	-2.5

TEST VOLTAGE/CURRENT APPLIED TO PINS LISTED BELOW:					
V _{IL min} to V _{IL max}	V _{IH min} to V _{IH max}	V _{IH max}	V _{EE}	I _L	V _{CC} (Gnd)
-	-	-	1, 2, 4, 5, 7, 9, 10, 12, 13	-	14
-	-	1	2, 4, 5, 7, 9, 10, 12, 13	-	14
-	-	2	1, 4, 5, 7, 9, 10, 12, 13	-	14
-	-	-	1, 2, 4, 5, 7, 9, 10, 12, 13	-	14
1	-	-	2, 4, 5, 7, 9, 10, 12, 13	3	14
2	-	-	1, 4, 5, 7, 9, 10, 12, 13	3	14
-	1	-	2, 4, 5, 7, 9, 10, 12, 13	-	14
-	2	-	1, 4, 5, 7, 9, 10, 12, 13	-	14
Pulse In		Pulse Out		V _{EE} = -4.0 Vdc (+1.2V)	
1	3	-	2, 4, 5, 7, 9, 10, 12, 13	-	14

Characteristic	Symbol	Pin Under Test
Power Supply Drain Current MC1210/MC1010 MC1211/MC1011 MC1212/MC1012	I _E	7
Input Current	I _{in}	1, 2
Input Leakage Current	I _R	Inputs*
"NOR" Logical "1" Output Voltage	V _{OH}	3
"NOR" Logical "0" Output Voltage	V _{OL}	3
Switching Times Propagation Delay (Fan-Out = 3)	t _{1+3- t₁₋₃₊}	3
(Fan-Out = 15)	t _{1+3- t₁₋₃₊}	
Rise Time (Fan-Out = 3)	t ₃₊	
Fall Time (Fan-Out = 3)	t ₃₋	



SWITCHING TIME WAVEFORMS

APPLICATIONS INFORMATION

The MC1010-1012/MC1210-1212 quad 2-input NOR gates are very useful in building more complex functions. For example, two R-S flip-flops may be obtained by cross-coupling gates, or a single gated R-S flip-flop may be obtained (see diagram below).

Dual clocked R-S flip-flops are available in MECL II (see flip-flop section). The quad 2-input gate may also be used as a dual exclusive OR or NOR by ORing the outputs as shown below.

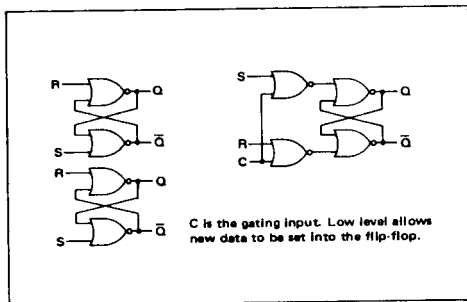
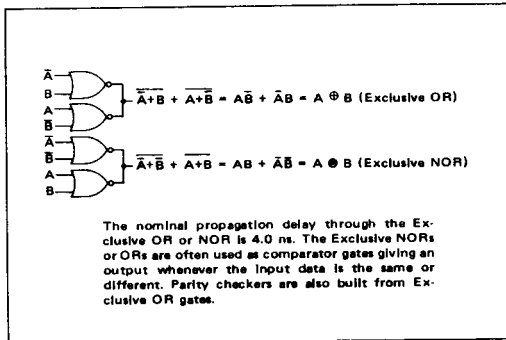


FIGURE 1 - FLIP-FLOPS OBTAINED BY USING MC1010-1012/MC1210-1212 GATES

FIGURE 2 - DUAL EXCLUSIVE "OR" or "NOR" GATES



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