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National Semiconductor

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# LP3982
# Micropower, Ultra Low-Dropout, Low-Noise, 300mA CMOS Regulator

## General Description

The LP3982 low-dropout (LDO) CMOS linear regulator is available in 1.8V, 2.5V, 2.77V, 2.82V, 3.0V, 3.3V, and adjustable versions. They deliver 300mA of output current. Packaged in an 8-Pin MSOP, the LP3982 is pin and package compatible with Maxim's MAX8860. The LM3982 is also available in the small footprint LLP package.

The LP3982 suits battery powered applications because of its shutdown mode (1nA typ), low quiescent current (90µA typ), and LDO voltage (120mV typ). The low dropout voltage allows for more utilization of a battery's available energy by operating closer to its end-of-life voltage. The LP3982's PMOS output transistor consumes relatively no drive current compared to PNP LDO regulators.

This PMOS regulator is stable with small ceramic capacitive loads (2.2µF typ).

These devices also include regulation fault detection, a bandgap voltage reference, constant current limiting and thermal overload protection.

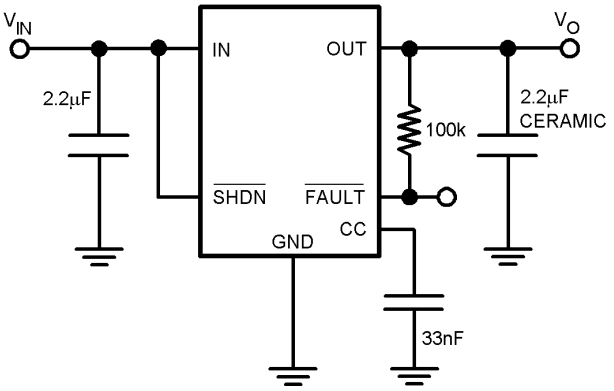
## Features

- MAX8860 pin, package and spec. compatible
- LLP space saving package
- 300mA guaranteed output current
- 120mV typical dropout @ 300mA
- 90µA typical quiescent current
- 1nA typical shutdown mode
- 60dB typical PSRR
- 2.5V to 6V input range
- 120µs typical turn-on time
- Stable with small ceramic output capacitors
- 37µV RMS output voltage noise (10Hz to 100kHz)
- Over temperature/over current protection
- ±2% output voltage tolerance

## Applications

- Wireless handsets
- DSP core power
- Battery powered electronics
- Portable information appliances

## Application Circuit

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## Absolute Maximum Ratings (Notes 1, 2)

**If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/ Distributors for availability and specifications.**

| | |
|---|---|
| $V_{IN}$, $V_{OUT}$, $V_{\overline{SHDN}}$, $V_{SET}$, $V_{CC}$, $V_{\overline{FAULT}}$ | −0.3V to 6.5V |
| Fault Sink Current | 20mA |
| Power Dissipation | (Note 3) |
| Storage Temperature Range | −65˚C to 160˚C |
| Junction Temperature ($T_J$) | 150˚C |
| Lead Temperature (10 sec.) | 260˚C |
| ESD Rating | |
| Human Body Model (Note 6) | 2kV |
| Machine Model | 200V |
| Thermal Resistance ($\theta_{JA}$) | |
| 8-Pin MSOP | 223˚C/W |
| 8-Pin LLP | (Note 3) |

## Operating Ratings (Note 1), (Note 2)

| | |
|---|---|
| Temperature Range | −40˚C to 85˚C |
| Supply Voltage | 2.5V to 6.0V |

## Electrical Characteristics

Unless otherwise specified, all limits guaranteed for $V_{IN} = V_O$ +0.5V (Note 7), $V_{\overline{SHDN}} = V_{IN}$, $C_{IN} = C_{OUT} = 2.2\mu F$, $C_{CC} = 33nF$, $T_J = 25˚C$. **Boldface** limits apply for the operating temperature extremes: −40˚C and 85˚C.

| Symbol | Parameter | Conditions | Min (Note 5) | Typ (Note 4) | Max (Note 5) | Units |
|---|---|---|---|---|---|---|
| $V_{IN}$ | Input Voltage | | **2.5** | | **6.0** | V |
| $\Delta V_O$ | Output Voltage Tolerance | 100µA ≤ $I_{OUT}$ ≤ 300mA<br>$V_{IN} = V_O$ +0.5V, (Note 7)<br>SET = OUT for the Adjust Versions | −2 | | +2 | % of $V_{OUT (NOM)}$ |
| | | | **−3** | | **+3** | |
| $V_O$ | Output Adjust Range | Adjust Version Only | **1.25** | | **6** | V |
| $I_O$ | Maximum Output Current | Average DC Current Rating | **300** | | | mA |
| $I_{LIMIT}$ | Output Current Limit | | **330** | 770 | | mA |
| $I_Q$ | Supply Current | $I_{OUT}$ = 0mA | | 90 | **270** | µA |
| | | $I_{OUT}$ = 300mA | | 225 | | |
| | Shutdown Supply Current | $V_O$ = 0V, $\overline{SHDN}$ = GND | | 0.001 | 1 | µA |
| $V_{DO}$ | Dropout Voltage (Note 7), (Note 8) | $I_{OUT}$ = 1mA | | 0.4 | | mV |
| | | $I_{OUT}$ = 200mA | | 80 | **220** | |
| | | $I_{OUT}$ = 300mA | | 120 | | |
| $\Delta V_O$ | Line Regulation | $I_{OUT}$ = 1mA, ($V_O$ + 0.5V) ≤ $V_I$ ≤ 6V (Note 7) | **−0.1** | 0.01 | **0.1** | %/V |
| | Load Regulation | 100µA ≤ $I_{OUT}$ ≤ 300mA | | 0.002 | | %/mA |
| $e_n$ | Output Voltage Noise | $I_{OUT}$ = 10mA, 10Hz ≤ f ≤ 100kHz | | 37 | | $\mu V_{RMS}$ |
| | Output Voltage Noise Density | 10Hz ≤ f ≤ 100kHz, $C_{OUT}$ = 10µF | | 190 | | nV/$\sqrt{Hz}$ |
| $V_{\overline{SHDN}}$ | $\overline{SHDN}$ Input Threshold | $V_{IH}$, ($V_O$ + 0.5V) ≤ $V_I$ ≤ 6V (Note 7) | **2** | | | V |
| | | $V_{IL}$, ($V_O$ + 0.5V) ≤ $V_I$ ≤ 6V (Note 7) | | | **0.4** | |
| $I_{\overline{SHDN}}$ | $\overline{SHDN}$ Input Bias Current | $\overline{SHDN}$ = GND or IN | | 0.1 | 100 | nA |
| $I_{SET}$ | SET Input Leakage | SET = 1.3V, Adjust Version Only (Note 9) | | 0.1 | 2.5 | nA |
| $V_{\overline{FAULT}}$ | $\overline{FAULT}$Detection Voltage | $V_O \geq$ 2.5V, $I_{OUT}$ = 200mA (Note 10) | | 120 | **280** | mV |
| | $\overline{FAULT}$ Output Low Voltage | $I_{SINK}$ = 2mA | | 0.115 | **0.25** | V |
| $I_{\overline{FAULT}}$ | $\overline{FAULT}$ Off-Leakage Current | $\overline{FAULT}$ = 3.6V, $\overline{SHDN}$ = 0V | | 0.1 | 100 | nA |
| $T_{SD}$ | Thermal Shutdown Temperature | | | 160 | | ˚C |
| | Thermal Shutdown Hysteresis | | | 10 | | |
| $T_{ON}$ | Start-Up Time | $C_{OUT}$ = 10µF, $V_O$ at 90% of Final Value | | 120 | | µs |

**Note 1:** Absolute Maximum ratings indicate limits beyond which damage may occur. Electrical specifications do not apply when operating the device outside of its rated operating conditions.

## Electrical Characteristics (Continued)

**Note 2:** All voltages are with respect to the potential at the ground pin.

**Note 3:** Maximum Power dissipation for the device is calculated using the following equations:

$$P_D = \frac{T_{J(MAX)} - T_A}{\theta_{JA}}$$

where $T_{J(MAX)}$ is the maximum junction temperature, $T_A$ is the ambient temperature, and $\theta_{JA}$ is the junction-to-ambient thermal resistance. E.g. for the MSOP-8 package $\theta_{JA}$ = 223˚C/W, $T_{J(MAX)}$ = 150˚C and using $T_A$ = 25˚C, the maximum power dissipation is found to be 561mW. The derating factor ($-1/\theta_{JA}$) = −4.5mW/˚C, thus below 25˚C the power dissipation figure can be increased by 4.5mW per degree, and similarity decreased by this factor for temperatures above 25˚C. The value of the $\theta_{JA}$ for the LLP package is specifically dependent on the PCB trace area, trace material, and the number of layers and thermal vias. For improved thermal resistance and power dissipation for the LLP package, refer to Application Note AN-1187.

**Note 4:** Typical Values represent the most likely parametric norm.

**Note 5:** All limits are guaranteed by testing or statistical analysis.

**Note 6:** Human body model: 1.5kΩ in series with 100pF.

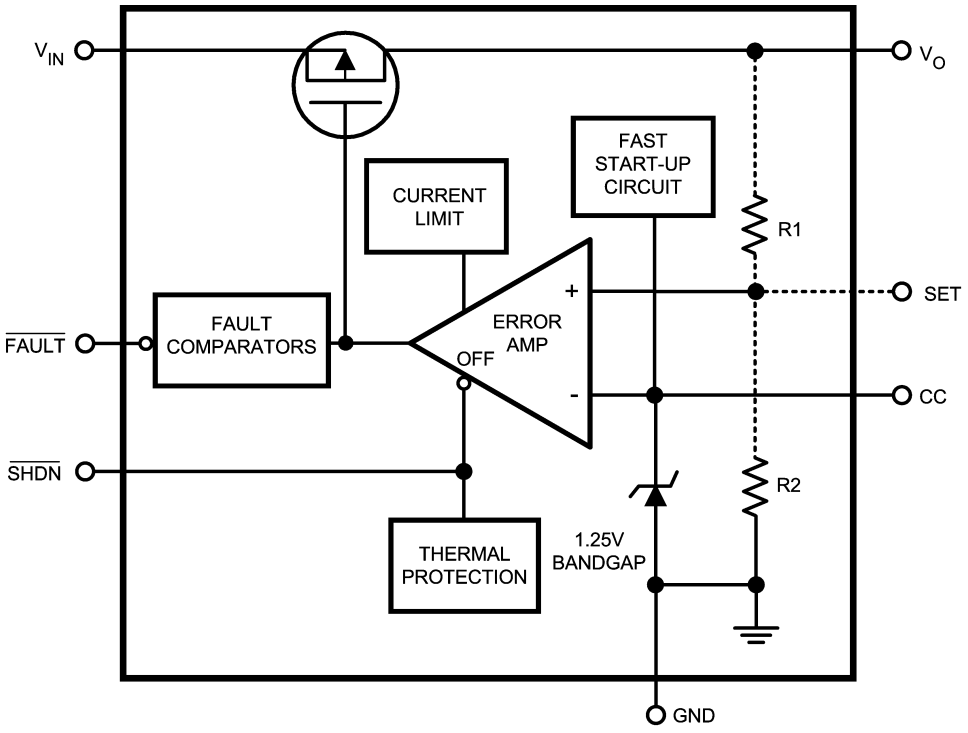
**Note 7:** Condition does not apply to input voltages below 2.5V since this is the minimum input operating voltage.

**Note 8:** Dropout voltage is measured by reducing $V_{IN}$ until $V_O$ drops 100mV from its nominal value at $V_{IN}$ -$V_O$ = 0.5V. Dropout Voltage does not apply to the 1.8 version.

**Note 9:** The SET pin is not externally connected for the fixed versions.

**Note 10:** The $\overline{\text{FAULT}}$ detection voltage is specified for the input to output voltage differential at which the $\overline{\text{FAULT}}$ pin goes active low.

## Functional Block Diagram

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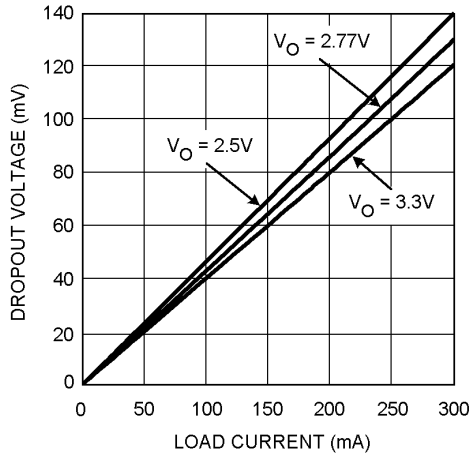
## Typical Performance Characteristics

Unless otherwise specified, $V_{IN} = V_O + 0.5V$, $C_{IN} = C_{OUT} = 2.2\mu F$, $C_{CC} = 33nF$, $T_J = 25^\circ C$, $V_{\overline{SHDN}} = V_{IN}$.

**Dropout Voltage vs. Load Current (For Different Output Voltages)**

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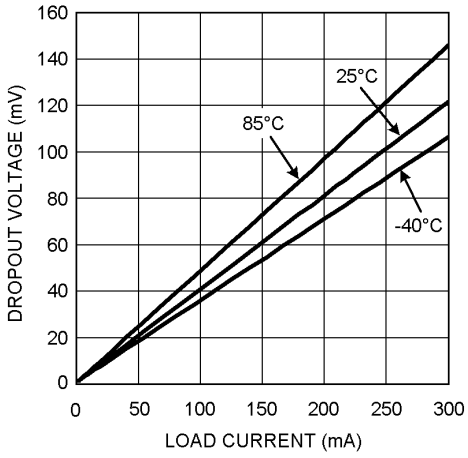
**Dropout Voltage vs. Load Current (For Different Output Temperatures)**

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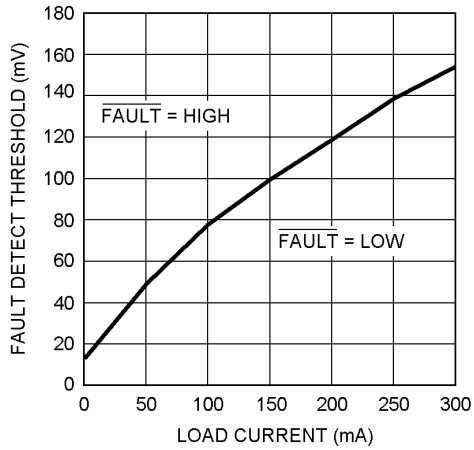
**$\overline{FAULT}$ Detect Threshold vs. Load Current**

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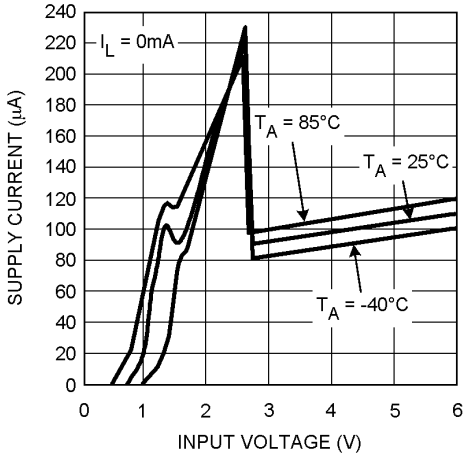
**Supply Current vs. Input Voltage**

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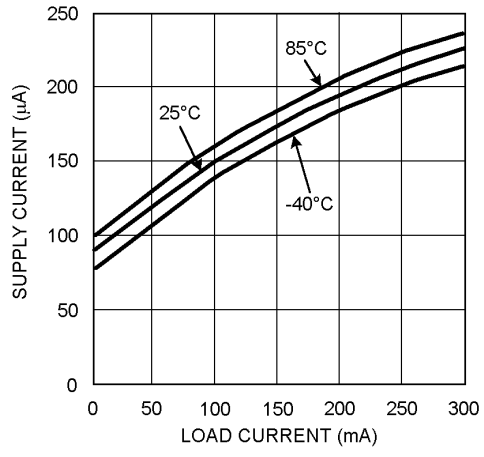
**Supply Current vs. Load Current**

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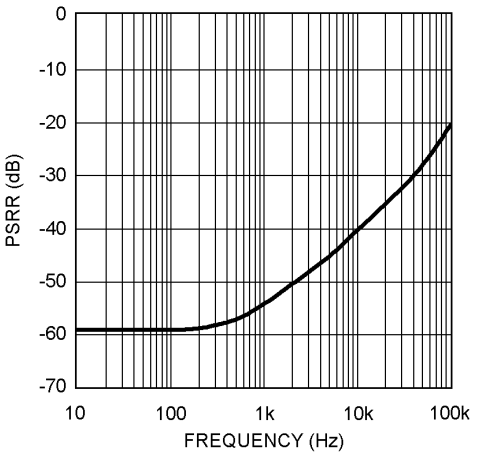
**Power Supply Rejection Ratio vs. Frequency**

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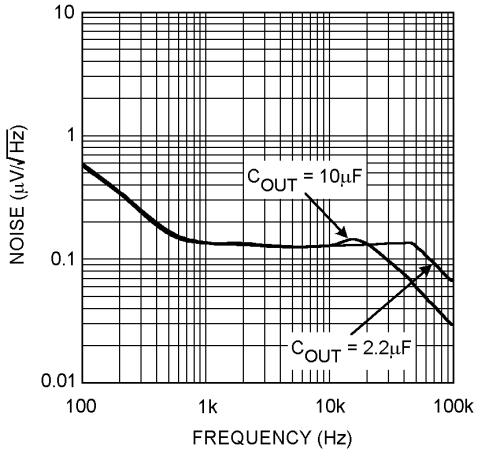
## Typical Performance Characteristics

Unless otherwise specified, $V_{IN} = V_O + 0.5V$, $C_{IN} = C_{OUT} = 2.2\mu F$, $C_{CC} = 33nF$, $T_J = 25^\circ C$, $V_{\overline{SHDN}} = V_{IN}$. (Continued)

**Output Noise Spectral Density**

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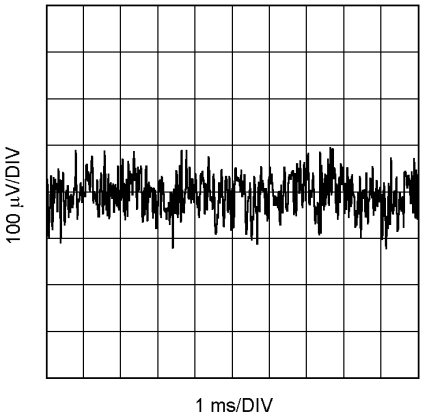
**Output Noise (10Hz to 100kHz)**

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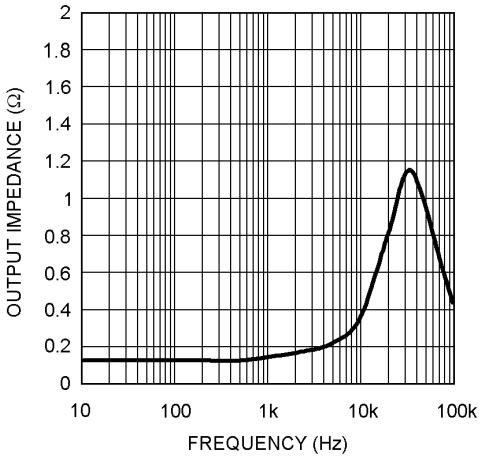
**Output Impedance vs. Frequency**

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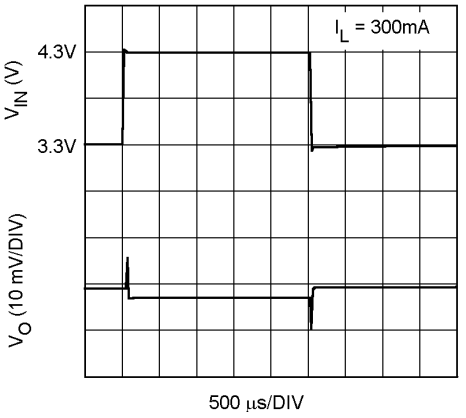
**Line Transient Response**

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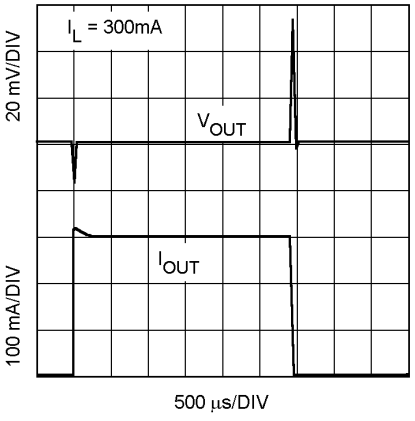
**Load Transient**

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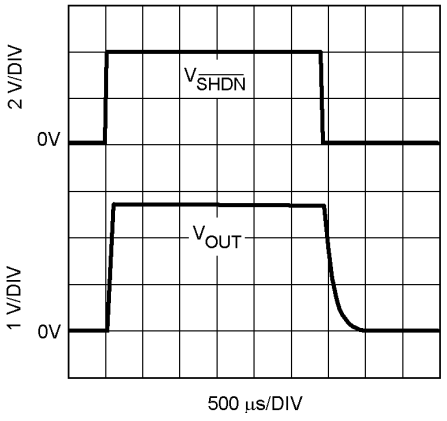
**Shutdown Response**

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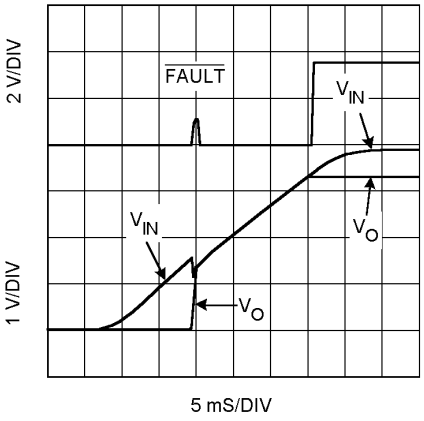
## Typical Performance Characteristics

Unless otherwise specified, $V_{IN} = V_O + 0.5V$, $C_{IN} = C_{OUT} = 2.2\mu F$, $C_{CC} = 33nF$, $T_J = 25^\circ C$, $V_{\overline{SHDN}} = V_{IN}$. (Continued)

**Power-Up Response**

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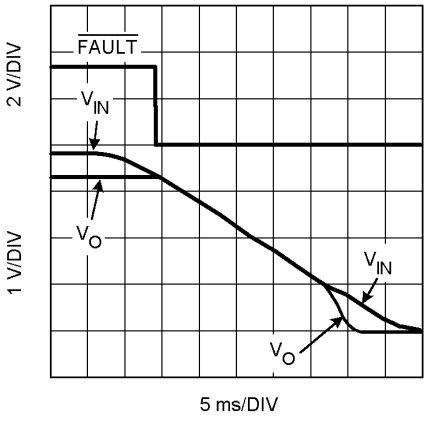
**Power-Down Response**

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## Application Information

### GENERAL INFORMATION

LP3982 is package, pin and performance compatible with Maxim's MAX8860 excluding reverse battery protection and Dual Mode™ function (fixed and adjustable combined).

*Figure 1* shows the functional block diagram for the LP3982. A 1.25V bandgap reference, an error amplifier and a PMOS pass transistor perform voltage regulation while being supported by shutdown, fault, and the usual Temperature and current protection circuitry

The regulator's topology is the classic type with negative feedback from the output to one of the inputs of the error amplifier. Feedback resistors $R_1$ and $R_2$ are either internal or external to the IC, depending on whether it is the fixed voltage version or the adjustable version. The negative feedback and high open loop gain of the error amplifier cause the two inputs of the error amplifier to be virtually equal in voltage. If the output voltage changes due to load changes, the error amplifier provides the appropriate drive to the pass transistor to maintain the error amplifier's inputs as virtually equal. In short, the error amplifier keeps the output voltage constant in order to keep its inputs equal.

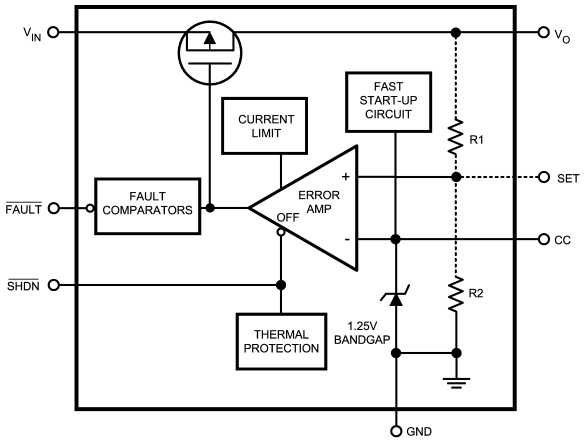


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**FIGURE 1. Functional Block Diagram for the LP3982**

### OUTPUT VOLTAGE SETTING (ADJ VERSION ONLY)

The output voltage is set according to the amount of negative feedback (Note that the pass transistor inverts the feedback signal.) *Figure 2* simplifies the topology of the LP3982. This type of regulator can be represented as an op amp configured as non-inverting amplifier and a fixed DC Voltage ($V_{REF}$) for its input signal. The special characteristic of this op amp is its extra-large output transistor that only sources current. In terms of its non-inverting configuration, the output voltage equals $V_{REF}$ times the closed loop gain:

$$V_O = V_{REF}\left[\frac{R_1}{R_2} + 1\right]$$

Utilize the following equation for adjusting the output to a particular voltage:

$$R_1 = R_2\left[\frac{V_O}{1.25V} - 1\right]$$

Choose $R_2$ = 100k to optimize accuracy, power supply rejection, noise and power consumption.

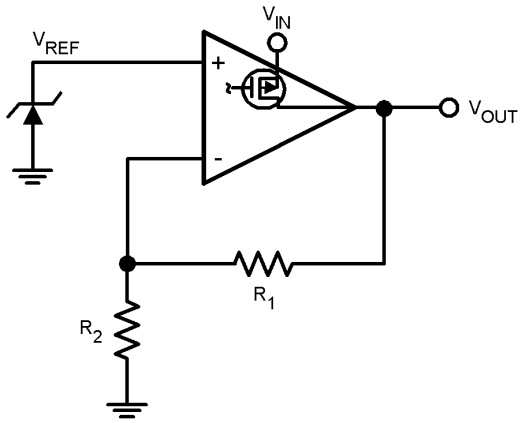


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**FIGURE 2. Regulator Topology Simplified**

## Application Information (Continued)

Similarity in the output capabilities exists between op amps and linear regulators. Just as rail-to-rail output op amps allow their output voltage to approach the supply voltage, low dropout regulators (LDOs) allow their output voltage to operate close to the input voltage. Both achieve this by the configuration of their output transistors. Standard op amps and regulator outputs are at the source (or emitter) of the output transistor. Rail-to-rail op amp and LDO regulator outputs are at the drain (or collector) of the output transistor. This replaces the threshold (or diode drop) limitations on the output with the less restrictive source-to-drain (or $V_{SAT}$) limitations. There is a trade-off, of course. The output impedance become significantly higher, thus providing a critically lower pole when combined with the capacitive load. That's why rail-to-rail op amps are usually poor at driving capacitive loads and recommend a series output resistor when doing so. LDOs require the same series resistance except that the internal resistance of the output capacitor will usually suffice. Refer to the output capacitance section for more information.

### OUTPUT CAPACITANCE

The LP3982 is specifically designed to employ ceramic output capacitors as low as 2.2µF. Ceramic capacitors below 10µF offer significant cost and space savings, along with high frequency noise filtering. Higher values and other types and of capacitor may be used, but their equivalent series resistance (ESR) should be maintained below 0.5Ω

Ceramic capacitor of the value required by the LP3982 are available in the following dielectric types: Z5U, Y5V, X5R and X7R. The Z5U and Y5V types exhibit a 50% or more drop in capacitance value as their temperature increases from 25˚C, an important consideration. The X5R generally maintain their capacitance value within ±20%. The X7R type are desirable for their tighter tolerance of 10% over temperature.

Ceramic capacitors pose a challenge because of their relatively low ESR. Like most other LDOs, the LP3982 relies on a zero in the frequency response to compensate against excessive phase shift in the regulator's feedback loop. If the phase shift reaches 360˚ (i.e.; becomes positive), the regulator will oscillate. This compensation usually resides in the zero generated by the combination of the output capacitor with its equivalent series resistance (ESR). The zero is intended to cancel the effects of the pole generated by the load capacitance ($C_L$) combined with the parallel combination of the load resistance ($R_L$) and the output resistance ($R_O$) of the regulator. The challenge posed by low ESR capacitors is that the zero it generates can be too high in frequency for the pole that it's intended to compensate. The LP3982 overcomes this challenge by internally generating a strategically placed zero.

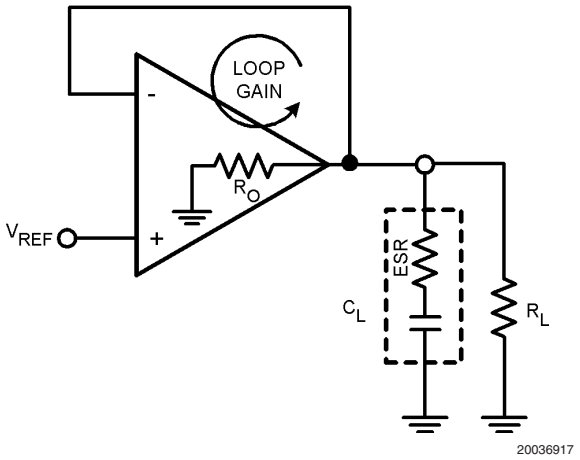



**FIGURE 3. Simplified Model of Regulator Loop Gain Components**

*Figure 3* shows a basic model for the linear regulator that helps describe what happens to the output signal as it is processed through its feedback loop; that is, describe its loop gain (LG). The LG includes two main transfer functions: the error amplifier and the load. The error amplifier provides voltage gain and a dominant pole, while the load provides a zero and a pole. The LG of the model in *Figure 3* is described by the following equation:

$$LG\ (j\omega) = \frac{A_O}{1 + j\left[\frac{\omega}{\omega_{POLE}}\right]} * \frac{1 + j\omega\ (ESR \times C_L)}{1 + j\omega\ ((ESR + R_O\ //\ R_L)\ C_L)}$$

The first term of the above equation expresses the voltage gain (numerator) and a single pole role-off (denominator) of the error amplifier. The second term expresses the zero (numerator) and pole (denominator) of the load in combination with the $R_O$ of the regulator.

*Figure 4* shows a Bode plot that represents a case where the zero contributed by the load is too high to cancel the effect of the pole contributed by the load and $R_O$. The solid line illustrates the loop gain while the dashed line illustrates the corresponding phase shift. Notice that the phase shift at unity gain is a total 360˚ -the criteria for oscillation.

## Application Information (Continued)

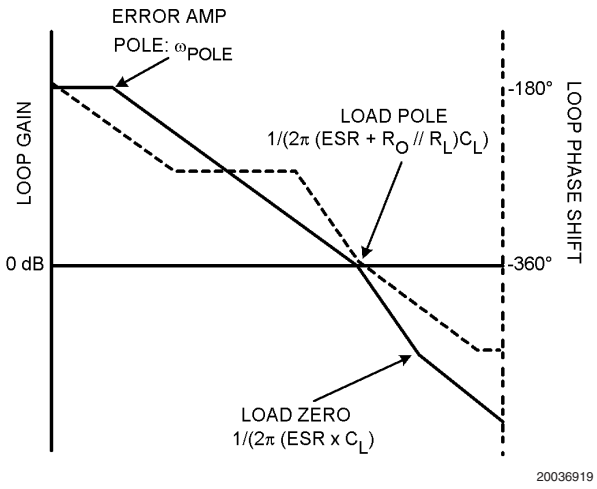



**FIGURE 4. Loop Gain Bode Plot Illustrating Inadequately High Zero for Stability Compensation**

The LP3982 generates an internal zero that makes up for the inadequately high zero of the low ESR ceramic output capacitor. This internally generated zero is strategically placed to provide positive phase shift near unity gain, thus providing a stable phase margin.

### NO-LOAD STABILITY

The LP3982 remains stable during no-load conditions, a necessary feature for CMOS RAM keep-alive applications.

### INPUT CAPACITOR

The LP3982 requires a minimum input capacitance of about 1µF. The value may be increased indefinitely. The type is not critical to stability. However, instability may occur with bench set-ups where long supply leads are used, particularly at near dropout and high current conditions. This is attributed to the lead inductance coupling to the output through the gate oxide of the pass transistor; thus, forming a pseudo LCR network within the Loop-gain. A 10µF tantalum input capacitor remedies this non-situ condition; its larger ESR acts to dampen the pseudo LCR network. This may only be necessary for some bench setups. 1µF ceramic input capacitor are fine for most end-use applications.

If a tantalum input capacitor is intended for the final application, it is important to consider their tendency to fail in short circuit mode, thus potentially damaging the part.

### NOISE BYPASS CAPACITOR

The noise bypass capacitor (CC) significantly reduces output noise of the LP3982. It connects between pin 6 and ground. The optimum value for CC is 33nF.

Pin 6 directly connects to the high impedance output of the bandgap. The DC leakage of the CC capacitor should be considered; loading down the reference will reduce the output voltage. NPO and COG ceramic capacitors typically offer very low leakage. Polypropylene and polycarbonate film carbonate capacitor offer even lower leakage currents.

CC does not affect the transient response; however, it does affect turn-on time. The smaller the CC value, the quicker the turn-on time.

### POWER DISSIPATION

Power dissipation refers to the part's ability to radiate heat away from the silicon, with packaging being a key factor. A reasonable analogy is the packaging a human being might wear, a jacket for example. A jacket keeps a person comfortable on a cold day, but not so comfortable on a hot day. It would be even worse if the person was exerting power (exercising). This is because the jacket has resistance to heat flow to the outside ambient air, like the IC package has a thermal resistance from its junctions to the ambient ($\theta_{JA}$).

$\theta_{JA}$ has a unit of temperature per power and can be used to calculate the IC's junction temperature as follows:

$$T_J = \theta_{JA} (PD) + T_A$$

$T_J$ is the junction temperature of the IC. $\theta_{JA}$ is the thermal resistance from the junction to the ambient air outside the package. PD is the power exerted by the IC, and $T_A$ is the ambient temperature.

PD is calculated as follows:

$$PD = I_{OUT} (V_{IN} - V_O)$$

$\theta_{JA}$ for the LP3982 package (MSOP-8) is 223˚C/W with no forced air flow, 182˚C/W with 225 linear feet per minute (LFPM) of air flow, 163˚C/W with 500 LFPM of air flow, and 149˚C/W with 900 LFPM of air flow.

$\theta_{JA}$ can also be decreased (improved) by considering the layout of the PC board: heavy traces (particularly at $V_{IN}$ and the two $V_{OUT}$ pins), large planes, through-holes, etc.

Improvements and absolute measurements of the $\theta_{JA}$ can be estimated by utilizing the thermal shutdown circuitry that is internal to the IC. The thermal shutdown turns off the pass transistor of the device when its junction temperature reaches 160˚C (Typical). The pass transistor doesn't turn on again until the junction temperature drops about 10˚C (hysteresis).

Using the thermal shutdown circuit to estimate , $\theta_{JA}$ can be done as follows: With a low input to output voltage differential, set the load current to 300mA. Increase the input voltage until the thermal shutdown begins to cycle on and off. Then slowly decrease $V_{IN}$ (100mV increments) until the part stays on. Record the resulting voltage differential ($V_D$) and use it in the following equation:

$$\theta_{JA} = \frac{(160 - T_A)}{(0.300 \times V_D)}$$

### FAULT DETECTION

The LP3982 provides a $\overline{\text{FAULT}}$ pin that goes low during out of regulation conditions like current limit and thermal shutdown, or when it approaches dropout. The latter monitors the input-to-output voltage differential and compares it against a threshold that is slightly above the dropout voltage. This threshold also tracks the dropout voltage as it varies with load current. Refer to Fault Detect vs. Load Current curve in the typical characteristics section.

The $\overline{\text{FAULT}}$ pin requires a pull-up resistor since it is an open-drain output. This resistor should be large in value to reduce energy drain. A 100kΩ pull-up resistor works well for most applications.

*Figure 5* shows the LP3985 with delay added to the $\overline{\text{FAULT}}$ pin for the reset pin of a microprocessor. The output of the comparator stays low for a preset amount of time after the regulator comes out of a fault condition.

## Application Information (Continued)

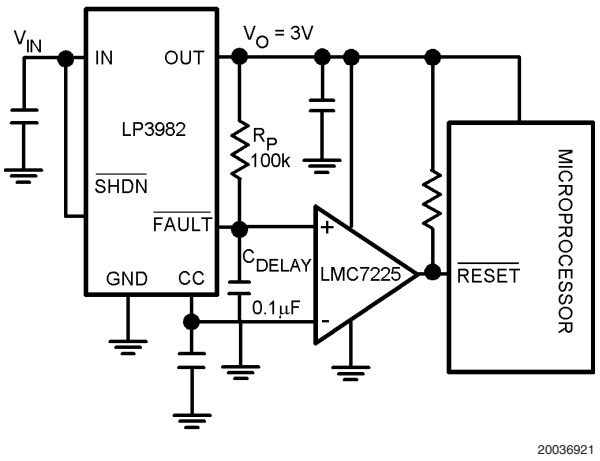



**FIGURE 5. Power on Delayed Reset Application**

The delay time for the application of *Figure 5* is set as follows:

$$C_{DELAY} = \frac{-t}{R_P \ln\left[1 - \frac{V_{REF}}{V_O}\right]}$$

The application is set for a reset delay time of 8.8ms. Note that the comparator should have high impedance inputs so as to not load down the $V_{REF}$ at the CC pin of the LP3982.

### SHUTDOWN

The LP3982 goes into sleep mode when the $\overline{SHDN}$ pin is in a logic low condition. During this condition, the pass transistor, error amplifier, and bandgap are turned off, reducing the supply current to 1nA typical. The maximum guaranteed voltage for a logic low at the $\overline{SHDN}$ pin is 0.4V. A minimum guaranteed voltage of 2V at the $\overline{SHDN}$ pin will turn the LP3982 back on. The $\overline{SHDN}$ pin may be directly tied to $V_{IN}$ to keep the part on. The $\overline{SHDN}$ pin may exceed $V_{IN}$ but not the ABS MAX of 6.5V.

*Figure 6* shows an application that uses the $\overline{SHDN}$ pin. It detects when the battery is too low and disconnects the load by turning off the regulator. A micropower comparator (LMC7215) and reference (LM385) are combined with resistors to set the minimum battery voltage. At the minimum battery voltage, the comparator output goes low and tuns off the LP3982 and corresponding load. Hysteresis is added to the minimum battery threshold to prevent the battery's recovery voltage from falsely indicating an above minimum condition. When the load is disconnected from the battery, it automatically increases in terminal voltage because of the reduced IR drop across its internal resistance. The Minimum battery detector of figure 6 has a low detection threshold ($V_{LT}$) of 3.6V that corresponds to the minimum battery voltage. The upper threshold ($V_{UT}$) is set for 4.6V in order to exceed the recovery voltage of the battery.

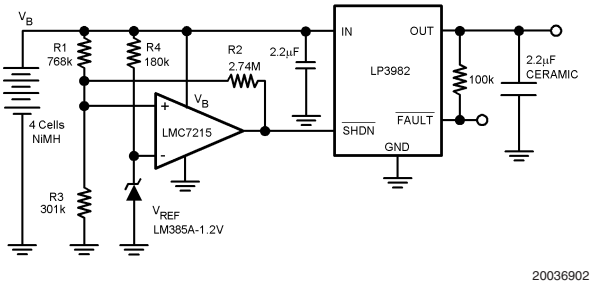



**FIGURE 6. Minimum Battery Detector that Disconnects the Load Via the $\overline{SHDN}$ Pin of the LP3982**

Resistor value for $V_{UT}$ and $V_{LT}$ are determined as follows:

$$G_T = \frac{1}{R_1} + \frac{1}{R_2} + \frac{1}{R_3}$$

$$V_{UT} = R_1 (V_{REF})\, G_T$$

$$V_{LT} = R_1 \,//\, R_2 (V_{REF})\, G_T$$

(The application of figure 6 used a $G_T$ of 5µ mho)

$$R_1 = \frac{V_{UT1}}{V_{REF}(G_T)}$$

$$R_2 = \frac{1}{\frac{V_{REF}(G_T)}{V_{LT}} - \frac{1}{R_1}}$$

$$R_3 = \frac{1}{G_T - \left[\frac{1}{R_1} + \frac{1}{R_2}\right]}$$

The above procedure assumes a rail-to-rail output comparator. Essentially, $R_2$ is in parallel with $R_1$ prior to reaching the lower threshold, then $R_2$ becomes parallel with $R_3$ for the upper threshold. Note that the application requires rail-to-rail input as well.

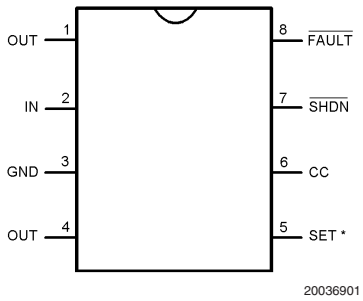
The resistor values shown in *Figure 6* are the closest practical to calculated values.

### FAST START-UP

The LP3982 provides fast start-up time for better system efficiency. The start-up speed is maintained when using the optional noise bypass capacitor. An internal 500µA current source charges the capacitor until it reaches about 90% of its final value.

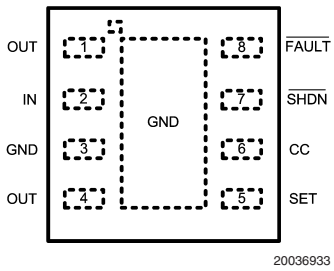
## Connection Diagrams

**8-Pin MSOP**




**Top View**

**8-Pin LLP Surface Mount**



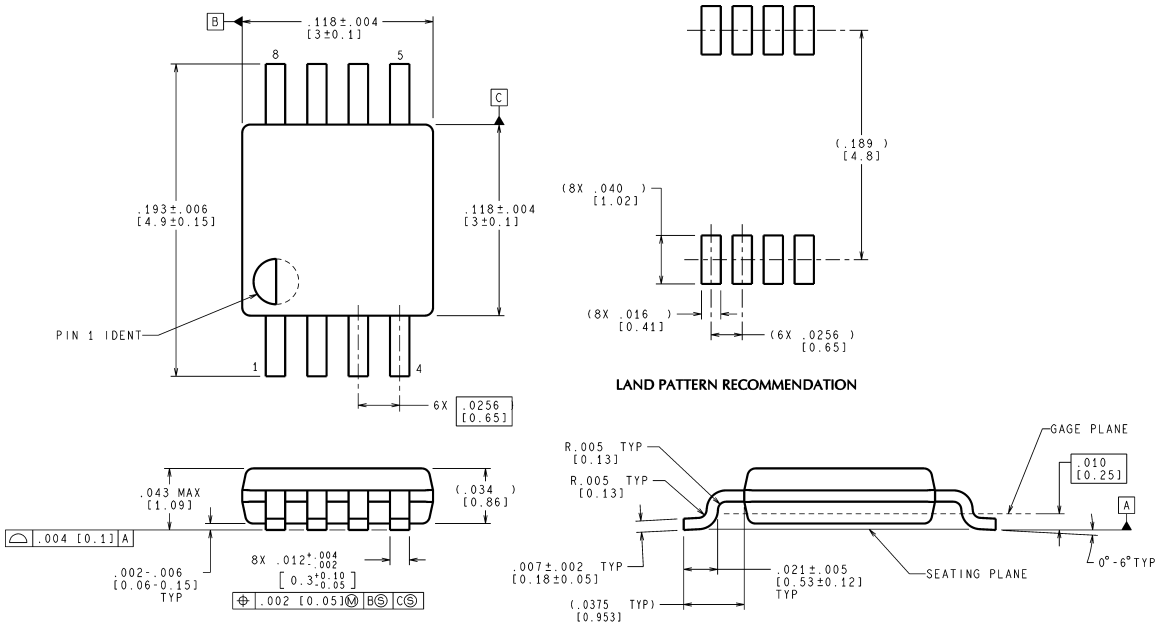

**Top View**

**Note:** The SET pin is internally disconnected for the fixed versions.

## Ordering Information

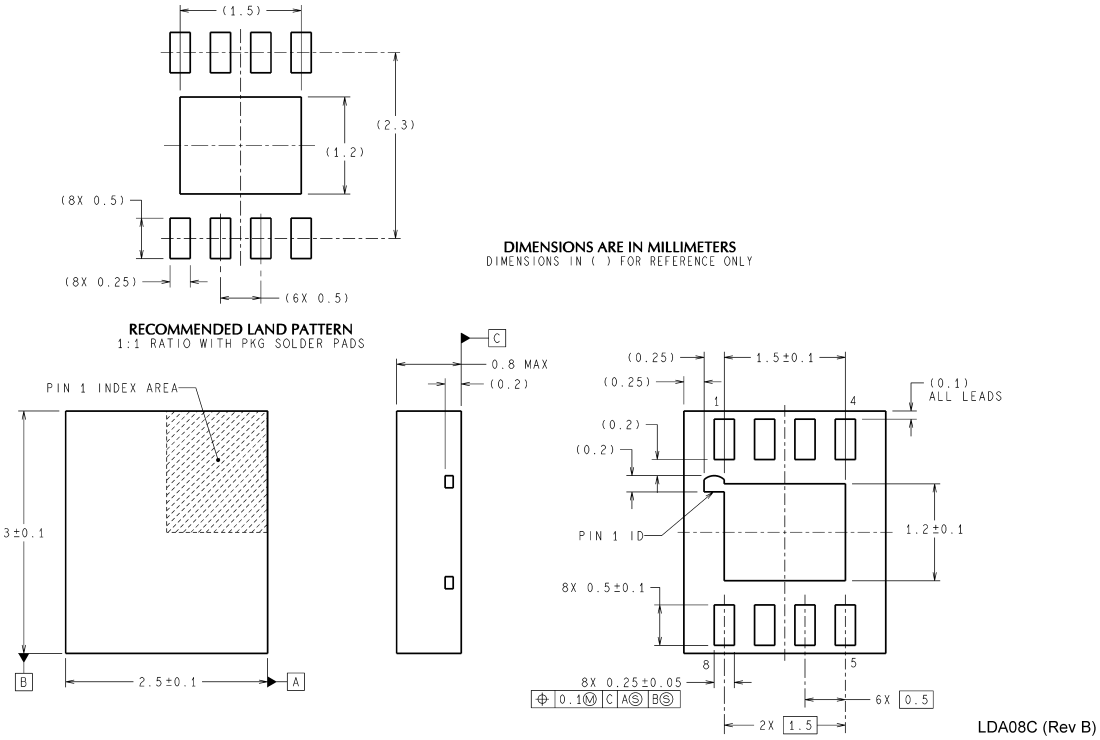
| Package | Part Number | Package Marking | Transport Media | NSC Drawing |
|---|---|---|---|---|
| 8-Pin MSOP | LP3982IMM-ADJ | LEVB | 1k Units Tape and Reel | MUA08A |
| | LP3982IMMX-ADJ | | 3.5k Units Tape and Reel | |
| | LP3982IMM-1.8 | LENB | 1k Units Tape and Reel | |
| | LP3982IMMX-1.8 | | 3.5k Units Tape and Reel | |
| | LP3982IMM-2.5 | LEPB | 1k Units Tape and Reel | |
| | LP3982IMMX-2.5 | | 3.5k Units Tape and Reel | |
| | LP3982IMM-2.77 | LERB | 1k Units Tape and Reel | |
| | LP3982IMMX-2.77 | | 3.5k Units Tape and Reel | |
| | LP3982IMM-2.82 | LESB | 1k Units Tape and Reel | |
| | LP3982IMMX-2.82 | | 3.5k Units Tape and Reel | |
| | LP3982IMM-3.0 | LETB | 1k Units Tape and Reel | |
| | LP3982IMMX-3.0 | | 3.5k Units Tape and Reel | |
| | LP3982IMM-3.3 | LEUB | 1k Units Tape and Reel | |
| | LP3982IMMX-3.3 | | 3.5k Units Tape and Reel | |
| 8-Pin LLP | LP3982ILD-1.8 | LNB | 1k Units Tape and Reel | LDA08C |
| | LP3982ILDX-1.8 | | 4.5k Units Tape and Reel | |
| | LP3982ILD-2.5 | LPB | 1k Units Tape and Reel | |
| | LP3982ILDX-2.5 | | 4.5k Units Tape and Reel | |
| | LP3982ILD-2.77 | LRB | 1k Units Tape and Reel | |
| | LP3982ILDX-2.77 | | 4.5k Units Tape and Reel | |
| | LP3982ILD-2.82 | LSB | 1k Units Tape and Reel | |
| | LP3982ILDX-2.82 | | 4.5k Units Tape and Reel | |
| | LP3982ILD-3.0 | LTB | 1k Units Tape and Reel | |
| | LP3982ILDX-3.0 | | 4.5k Units Tape and Reel | |
| | LP3982ILD-3.3 | LUB | 1k Units Tape and Reel | |
| | LP3982ILDX-3.3 | | 4.5k Units Tape and Reel | |
| | LP3982ILD-ADJ | LVB | 1k Units Tape and Reel | |
| | LP3982ILDX-ADJ | | 4.5k Units Tape and Reel | |

## Physical Dimensions inches (millimeters) unless otherwise noted




MUA08A (Rev E)

**8-Pin MSOP**
**NS Package Number MUA08A**




LDA08C (Rev B)

**8-Lead LLP Surface Mount**
**NS Package Number LDA08C**

## Notes



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