# **USER GUIDE**



# ML4066 CMIS Analyzer User Guide

CMIS Analyzer Board and CMIS Analysis and Compliance Software| Step-by-Step Guide

User Guide Revision 1.8, July 2021

# multiLane

Table of Contents

Revision Control	3
Overview	4
Analyzer Features	5
SFF Analyzer features	5
CMIS features	5
SFF Analyzer GUI	6
VCC tab	6
I2C Configuration Tab	7
I2C tab	7
Packet Descriptions	9
Functional Tests Tab	9
I2C Read/Write:	. 10
Memory Map Tab	. 11
CNTRL/ALRM Signals tab	. 12
Application Notes	13
I2C Tab	. 13
Functional Tests Tab	. 14
Cntrl/Alrm Tab	. 16
CMIS State Machine Test	19
Paged Memory Modules	19
Flat Memory Modules	20
Appendix I: Analyzer Card Diagram	21



# **Revision Control**

Revision number	Description	Release Date
1.0	Preliminary revision	11/27/2017
1.1	<ul> <li>Updated parag 3.2 to match version 1.0 of the GUI</li> </ul>	12/13/2017
1.2	<ul> <li>Adding period selection</li> </ul>	1/4/2018
1.3	<ul> <li>Adding Resistor pullup and Refresh button in cntrl Tab</li> </ul>	4/26/2018
1.4	<ul> <li>Adding application notes</li> </ul>	3/5/2018
1.5	<ul> <li>Update parag 3.3.1</li> </ul>	6/4/2018
1.6	<ul> <li>Add Appendix</li> </ul>	9/4/2019
1.7	<ul> <li>Add CMIS 4.0 State Machine Test</li> </ul>	3/2/2020
1.8	Format Updates	7/27/2021



# Overview

The ML4066 is an adapter with diagnostic interface for the power, I2C and management interface control and alarm signals. The ML4066-ANA analyzer board is connected to the ML4066 to enable live diagnosis for the transceiver and host, ensuring that the entire data was delivered.

The ML4066 also makes use of the Common Management Interface Specification (CMIS) allows host and module software implementers to utilize a common code base across a variety of form factors. CMIS is a robust and increasingly crucial element of data center interconnects, and critical for transceiver stability.



# Analyzer Features

# SFF Analyzer features

- USB Interface
- Windows based GUI and API Library
- Detection and measurement of host pull up + pull down resistors on low-speed signals
- Host VCC rails sampling measurement
- VCC spectral noise analysis
- I2C Analyzer
  - o Bus Speed
  - ACK/ NACK Detection
  - o Clock Stretching Analysis
  - $\circ$  Time Event Logging
- Functional tests
  - o Control signals
  - o Configuration registers
  - $\circ$   $% \left( Ability to emulate optical module by loading identification registers with custom data <math display="inline">% \left( Ability,Abilit$
  - $\circ$  ~ I2C Terminated by microcontroller, I2C slave compliant with MSA
  - $\circ$   $\;$  Implements MSA Memory map and programmable new pages  $\;$
  - $\circ$  Memory map can be loaded to replicate optical module's identification registers
  - o Ability to control/monitor all low-speed signals
  - $\circ \quad \text{Hot pluggable}$
- Alarm generation
- State Machine Emulator (CMIS)

## **CMIS features**

- Communicate with, operate and control various MCBs boards.
- Utilize a common software across a variety of form factors.
- Communicate on multiple host simultaneously, by assigning different USB instance to each host.
- In master mode, the analyzer acts as a host module DUT
  - $\circ$   $\,$  Load or save MSA files
  - o Read/Write individual module registers
  - o Stretch I2C rate
  - Drive control signals
  - $\circ$   $\;$  State machine sequencing test with transition timing and test report generation
- In slave mode, the analyzer acts as a module for a host DUT
  - Emulate a pluggable full register mapping
  - o Load any MSA file onto analyzer
  - Clock Stretching during I2C transactions



- Monitor host control signals and raise alarms
- In bypass mode, the analyzer monitors exchange between host and module
  - Analyze and log I2C packet exchange between module and host
    - o Observe control and alarm signal transactions
    - o Monitor VCC levels in real time

## **SFF Analyzer GUI**

#### VCC tab

The VCC tab allows the measurement of the VCCTX, RX and VCC1. Select the number of samples that will be multiplied by the sampling period selected from the Combo box. The default value of this period is  $0.55 \ \mu$ s.

You can add two markers to the graph by right-clicking with the mouse. Make sure to clear all markers to add new ones.



The values of the markers and their difference are displayed under the graph.

Figure 1: VCC tab



# I2C Configuration Tab

This tab allows the user to manually configure the I2C bus direction, speed, and clock stretching.

MLAnal	/zer Kit				-		×
Help	il ano						
		ML4066-Analyzer	Analyzer Type	QDD Analyzer	Disconne	ct	
CC rails	Select I2C Bus Direction:						Â
I2C Configuration	Internal Slave	و الا Master Configuration ــــــــــــــــــــــــــــــــــــ					
IZC		12C Speed(10~400/KHz) 100 Max 12C Clock Stretching(0~3000us) 1000					
Functional Tests		Get Apply Configuration					
dem A		r I2C Stave Configuration					
Memor		Enable Clock Stretching					
Critrl/Alrm signals		Get Apply Configuration					
: Machine Test (CMIS)							↓

Figure 2: I2C Capture tab

When choosing **Internal Slave**, you can Read/Write the Data of the Analyzer's EEPROM. **Internal Master** allows User to read/write on the Module\*.

Bypass mode makes the communication direct between the module and the host.

For the I2C Master configuration, use the Get button to retrieve the configuration. To change it, write the desired configuration then click "Apply Configuration". The max clock stretching corresponds to the maximum time that the Master waits for the Slave's response. To set the max clock stretching the "Enable Clock Stretching" checkbox must be checked.

For I2C slave configuration, user can choose to enable/disable clock stretching, and can also set the clock stretching time that will be forced on SCL during I2C transactions.

#### Disclaimer:

\*MultiLane supports the replacement of this terminology with more inclusive language. These terms will be retired in the updated CMIS 5.0 specification.

## I2C tab

This tab analyzes the I2C packets. The graph displays the clock (SCL) and the data (SDA). The SCL rising edges are detected and the SDA values are displayed at each rising edge (cf. image below).



A vertical line is drawn at each rising edge and the SDA binary values are displayed under the yellow SDA curve.



Figure 3: I2C Capture tab

The image above refers to the I2C read command. The data packets are displayed in a list under the graph.

Select the packet that you want to visualize on the graph to see the range of that packet.

Each packet is delimited on the graph by the Start (marked in green) and Stop (marked in red) conditions (cf. image above).

Note that you can show/hide any of the lines by clicking on the corresponding checkbox at the top of the graph.

You can also change the sampling period using the combo box. This period will be multiplied by the number of samples chosen. Its default value is 0.963µs.

To view the reading process, select a higher number of samples so the whole packet can be captured.



h	alyzer Kit																										9 <u>-</u>	
ıl	tiLane									ML	4066	-An	alyz	er					Anal	yzer T	ype					Disco	nnect	
	Number of Samples	; (1-120000)	120000		Free R	un	Sampling	) Period(u	s) = 0	.963			Period	set	0.963	<u> </u>			Captu	re I2C P	ackets		12C + Cla	oc <mark>k</mark> Stret	ching		Save to Fi	ile
						<b>V</b>		Edges	<b>-</b>	_	Start	⊻ -		Stop	<b>-</b>		SCL	<u>-</u>	- sc	A								
							0				1			1			0			•		0	0 0		0	0		-
	1000		1040		060	1080		100	1120		1140	Tim	1160 ne (us)				1200				40	1260		1280	130			
	Captured I2C Pace 1. A0 0 7F 0 00 0 2. A0 0 00 0 A1 0 1	ckets 8 0 20 <mark>0 02 0</mark>	0 02 0 FF 0 00	0 0 00 0 0	0 0 A 0 0	80 0 00 0	00 0 00 0	00 0 1C 0	75 0 78	8 0 83 (	0 00 0 00	0 00 0	00 0 00	0 00 0	00 0 00	0 1E (	0 0 0 0A	0 0 00 0	78 0 OF	1				~	Stre	tching	Duration	<u>(us)</u>

#### Figure 4: I2C Write

## Packet Descriptions

Each packet begins with the slave address A0 followed by the acknowledgment 0. The data afterword is the Data Word (7F is the page selection and 00 is the MemPage needed to write on). The second packet presents the writing process on the address 00(hex).

The free run checkbox is used to monitor the I2C bus. When checked, the monitoring function will start sampling directly after the I2C button is clicked.

When unchecked, the monitoring function will automatically detect I2C start frame.

#### Functional Tests Tab

The functional tests tab gives access to the memory pages. You can read/write on registers via I2C using this tab. To read/write from the module, select the "Internal Master" bus direction from the I2C configuration tab, or the "Internal Slave" to read/write from the EEPROM.



MLAnalyzer Kit				- 🗆 X
Help				
multiL <u>ane</u>	ML	4066-Analyzer	Analyzer Type QDD Analyzer	✓ Disconnect
C rails	I2C Read / Write			^
×	Memory Location	Upper Page 02 Upper Page 03		
ration				
Configu	None of the above	Set		
1200	Single Byte			
X	Address(decimal) Memory Co	ntent(Hex) Memory Content(binary)		
3	0 18	00011000		
ional Te	Read	Write		
Funct	- Multi Puta Pasel			
- g		Addrose Lloy Pin		
nory n				
M	Startung Address (Dec)	000 18 00011000 001 40 01000000	o	
	8	002 00 0000000		
lan (jan (jan (jan (jan (jan (jan (jan (j	David Courses file	003 07 00000111		
5 U	Read Save to file	005 00 0000000		
ltrl/A		006 00 0000000		
5		007 00 0000000		
		009 00 0000000		
		010 00 00000000		
AIIS)		011 00 0000000	~	
й С <u></u>		<	>	v

Figure 5: Functional Tests tab

For the SFP-Analyzer, the functional tests tab adds the slave addresses corresponding to the SFP standards.

MLAnalyzer Kit					- 🗆 X
Help					
multiLane		ML4066-Analyzer		Analyzer Type	Disconnect
Functional Teds IDC Deformation VCC mits	D2C Read / Write Slave Address O A0h A2h Other A0 h Set Single Byte Address(decimal) O Read	Memory Location Upper Page 00 Up Upper Page 03 None of the above Proceed Memory Content(Hoc) 03 Write	per Page 01 Uppe nter page number Memory Content(Dinary) 00000011	r Page 02 Set	
Memory map	Starting Address (Dec) End /	Address (Dec) Addre	ss Hex B 03 00000011 04 00000100 00 0000000	inary	
Critr/Alm signals	Read S	Save to file 003 004 005 006 007 007 007	11         00010001           00         00000000           00         00000000           00         00000000           00         00000000           00         00000000           04         00000100		
State Machine Test		009 010 011 <	00 0000000 00 0000000 00 0000000		

Figure 6: Functional Tests Tab for SFP-Analyzer

#### I2C Read/Write:

- 1. First, select which page you need to perform a read or write operation on in the Memory Location.
- 2. Then, use the "Single Byte" window to read/write one byte from the memory.
  - a. Address: The address to read/write from.



- b. Memory Content: The data value to be read/written to the selected address (In Hex or in Binary).
- 3. Alternatively, use the "Multi-byte Read" to read/write multiple bytes between a specified Starting Address and an End Address.

#### Memory Map Tab

This tab gives access to the memory map of the module. It can be loaded to replicate optical module's identification registers.

MLAnalyzer Kit						-	×
Help							
multiLane			<b>ML</b> 40	66-Analy	zer Analyzer Type	Disconnect	
VCC raits	Refresh	Load MS	6A from file	Save	MSA to file Write MSA to HW		^
	Address	Data(Hex)	Data(Dec.)	Data(Ascii)	MSA Description		
ti i	LowMem 0(00h)	18	24	٥	Identifier		
	LowMem 1(01h)	40	64	Ø	Version Id		
Cont	LowMem 2(02h)	00	0		CLEI code present		
	LowMem 3(03h)	07	7	0	Module State		
	LowMem 4(04h)	00	0		Bank 0		
_ <sup>™</sup>	LowMem 5(05h)	00	0		Bank 1		
	LowMem 6(06h)	00	0		Bank 2		
	LowMem 7(07h)	00	0		Bank 3		
lional	LowMem 8(08h)	00	0		Module State changed flag		
-	LowMem 9(09h)	00	0		Latched VCC3.3/Temp Alarm and Warning		
	LowMem 10(0Ah)	00	0		Latched AUX1/2 Alarm and Warning		
de -	LowMem 11(0Bh)	00	0		Latched Vendor Defined Alarm and Warning		
ory n	LowMem 12(0Ch)	00	0		Reserved		
Yem	LowMem 13(0Dh)	00	0		Custom		
	LowMem 14(0Eh)	1C	28		Internally measured Temperature 1 MSB		
( se	LowMem 15(0Fh)	00	0		Internally measured Temperature 1 LSB		
- sign	LowMem 16(10h)	7F	127	1	Internally measured Supply 3.3v MSB		
- All	LowMem 17(11h)	OB	11	٥	Internally measured Supply 3.3v LSB		
, the second sec	LowMem 18(12h)	00	0		Internally measured AUX1 MSB		
	LowMem 19(13h)	00	0		Internally measured AUX1 LSB		
lest	LowMem 20(14h)	00	0		Internally measured AUX2 MSB		
. s) sine	LowMem 21(15h)	00	0		Internally measured AUX2 LSB		
Mact	LowMem 22(16h)	7F	127	1	Internally measured AUX3 MSB		
	Lauddam (22(17b)	rr.	220	12	Informative managed AUV2 LCD		- T

Figure 7: Memory Map tab

This screen allows you to Load or Save your custom MSA configuration.

Data is displayed according to the selected I2C Bus Direction in a grid showing: register address,

hex value, Decimal Values, ASCII value, MSA description.

- **Refresh** button: Read MSA Registers, and refresh values.
- Write MSA to HW button: Write the current MSA configuration to OSFP module.
- Save MSA to file button: Saves the current MSA memory to a file using Comma separated values (CSV) format.
- Load MSA from file button: Loads MSA values from file and map it to MSA memory.

When choosing **Internal Slave**, you can Read/Write the Data of the Analyzer's EEPROM. **Internal Master** allows you to read/write on the Module. **Bypass mode** makes the communication direct between the module and the host.



For the SFP-Analyzer, choose your desired slave address and page to read it.

MLAna	ılyzer Kit								-	×
Help										
mult	tiLane			ML406	6-Analyzo	er Analyzer T	ype	✓ Di	isconnect	
VCC rails	Choose addresses to display Slave address A0	Refresh	Load MSA	from file	Save	MSA to file Write MSA to HW				
		Address	Data(Hex)	Data(Dec.)	Data(Ascii)	MSA Description				1
ration		5.A. A0 Byte 0 (00h)	0	0	0	Identifier	1.8			
ligu		S.A. A0 Byte 1 (01h)	0	0	0	Ext. Identifier				
Con		S.A. A0 Byte 2 (02h)	0	0	0	Connector	1.8			
L ≊		5.A. A0 Byte 3 (03h)	0	0	0	Transceiver				1
		S.A. A0 Byte 4 (04h)	0	0	0	Transceiver	1.8			
<u> </u>		S.A. A0 Byte 5 (05h)	0	0	0	Transceiver				
<b>2</b>		S.A. A0 Byte 6 (06h)	0	0	0	Transceiver				
E E		S.A. A0 Byte 7 (07h)	0	0	0	Transceiver	1.8			1
tions		S.A. A0 Byte 8 (08h)	0	0	0	Transceiver				
Func		S.A. A0 Byte 9 (09h)	0	0	0	Transceiver	1.8			
		S.A. A0 Byte 10 (0Ah)	0	0	0	Transceiver	1.8			
8		S.A. A0 Byte 11 (0Bh)	0	0	0	Encoding	1.8			
E b		5.A. A0 Byte 12 (0Ch)	0	0	0	BR, Nominal	1.8			
emo		S.A. A0 Byte 13 (0Dh)	0	0	0	Rate Identifier	1.8			
Σ		S.A. A0 Byte 14 (0Eh)	0	0	0	Length(SMF,km)	1.8			
		S.A. A0 Byte 15 (0Fh)	0	0	0	Length(SMF)	1.8			
l se		S.A. A0 Byte 16 (10h)	0	0	0	Length				
n sign		S.A. A0 Byte 17 (11h)	0	0	0	Length				
Alm /		S.A. A0 Byte 18 (12h)	0	0	0	Length	1.8			
l Tr		S.A. A0 Byte 19 (13h)	0	0	0	Length				
		S.A. A0 Byte 20 (14h)	0	0	0	Vendor Name	1.1			
ž		S.A. A0 Byte 21 (15h)	0	0	0	Vendor Name				
i i i		S.A. A0 Byte 22 (16h)	0	0	0	Vendor Name				
CMIS		S.A. A0 Byte 23 (17h)	0	0	0	Vendor Name	-			
State										

Figure 8: Memory Map tab in SFP analyzer

#### CNTRL/ALRM Signals tab

This tab allows detection and measurement of host pull up resistors on low speed signals and the detection of their state (either digital or analog). You can also drive these signals using the corresponding checkboxes.

- Pull-Up Resistors window: The analyzer detects if the pull-up resistor of each signal is missing or not and it calculates its value. The range between 1.3 KΩ and 10 KΩ is acceptable indicating that a pull-up resistor is present. Below 1.3 KΩ the resistor value is too low and you a short circuit. Above 10 KΩ you risk an open circuit. The marge of accuracy for the resistor's value is about 1 KΩ.
- For each signal the desired mode "Drive", "Bypass" or "Analog Sampler" is chosen. The Analog Monitor button displays the voltage of the desired signal. To manually assert/deassert the signals, the "Drive" option must be chosen to be able to toggle the signal's checkbox. Finally, if "Bypass" mode is selected, you can control the module externally and check its status by pressing the "Get" button.
- The Refresh button resets the signals in "Drive" mode to their initial states.



MLAnalyzer Kit		- 🗆 ×
Help		
multiLane	ML4066-Analyzer Analyzer Type	Disconnect
cails	Analog Monitor:	^
ACC	ResetL	4
		3.5
te stand te Unite Y stand te Unite		3
		2.5
I. LPMode     InitMode digital		2 ¥
Refresh		1.5
		1
ResetL		
Mode: Bypass V Mode: Analog Sampler V		0.5
2 1. ModSell 1. T ResetL		800
2. ModSelL digital 2. ResetL digital	Time (us)	
	Pull-Up Resistors	
	Refresh VCC VCC VCC	vcc
S Mode: Uppuss + Mode: Uppuss +	: Resistor value too low	
1. Intl. 1. ModPrst	4.244 K 4.273 K 1.766 K	1./66 K
2. ModersLaightai	ModPrsL IntL 12C SCL	I2C SDA

Figure 9: Cntrl/Alrm signals tab 1 in QDD analyzer

The pin pull-up resistors will differ depending on the form factor of the adaptor and module.



The SFP has different low speed control signals as seen in the figure below.

Figure 10: SFP-Analyzer Control signals

# **Application Notes**

## I2C Tab

1. Select "Bypass" mode from the "I2C Configuration" tab.



- 2. In the I2C tab, select the number of samples for the I2C capture, for the I2C read it should be the maximum.
- 3. Without selecting the "free run" checkbox, click the I2C button to start monitoring, then using your host send an I2C command (read or write) and wait for the I2C Frame Capture.
- 4. If the "free run" checkbox is selected, the capturing will start immediately after the I2C button is clicked.



Figure 11: I2C Read

## Functional Tests Tab

1. Select "Bypass" mode in the I2C configuration tab, using your host try to read/write a value from the module. In the Analyzer GUI, the read/write won't work in this mode because the Host and module communicate directly without the interference of the Analyzer.



MLAnalyzer Kit				- 🗆 X
Help				
multiLane	N	IL4066-Analyzer	Analyzer Type SFP Analyzer	✓ Disconnect
functional Tank IK RC configuration VCC with	I2C Read / Write Slave Address O Anh A2h Other A0 h Set Single Byte Address(decimal) Net 0 Read	Nory Location Upper Page 01 Upper Page 03 Nore of the above nory Context(tex) Write	Upper Page 02 Set ((hinary)	
Let Mactine Test Cut/Man signals Memory map	Starting Address (Dec) End Address 0 100 Read Save to	(Ovc) Address Hex 000 03 001 04 002 00 003 11 004 00 005 00 005 00 005 00 006 04 009 00 010 00 011 00 € ■	Binary 0000011 0 0000000 0 0000000 0 0000000 0 000000	

Figure 12: Functional Tab in Master Mode

 Select "Internal Master" mode in the I2C configuration tab, read address 0 using the Analyzer GUI. This value refers to the one written on the module. The connection between the Host and the Analyzer is cut and using the Host to read will give you FF values.

MLAnalyzer Kit				- 🗆 X
Help				
multilane	ML4	1066-Analyzer	Analyzer Type QDD Analyzer	✓ Disconnect
aire .	I2C Read / Write			^
ACC	Memory Location	Upper Page 02 Upper Page 03		
ation				
Configu	None of the above	Set		
	single Byte			
Z	Address(decimal) Memory Cont	tent(Hex) Memory Content(binary)		
	0 18	00011000		
Tional T	Read	Write		
Func	r Mutti-Byte Read			
de		Address Hex Bir	ary	
temory	Starting Address (Dec) End Address (Dec)	000 18 00011000	^	
	0 100	001 40 0100000 002 00 0000000	©	
akungis i	Read Save to file	003 07 00000111 004 00 0000000		
iri/Alim		005 00 0000000 006 00 0000000		
5		007 00 0000000 008 00 0000000		
- Test		009 00 0000000		
MIS)		011 00 0000000	~	

Figure 13: Functional Tab in Slave Mode

3. Select "Internal Slave" mode in the I2C configuration tab, the reading/writing command from the Analyzer or your Host will give the same value written in the EEPROM.



MLAnalyzer Kit				– 🗆 ×
Help				
multiLane		ML4066-Analyzer	Analyzer Type SFP Analyzer	✓ Disconnect
As DC Configuration VC clib	IZC Read / Write Slave Address O A0h A2h Other A0 h Set - Single Byte - Address(decimal) 0	Memory Location Upper Page 00 Upper Page 01 Upper Page 03 None of the above Please enter page number Memory Content[Hex] 03 00000011	Upper Page 02 Set	
Functional Tes	Read	Write		
Memory map	Starting Address (Dec) End A	Address (Dec) Address Hex 000 03 000 001 04 000 002 00 000	Binary 000011 ^ 000000 □	
Get(//km signals	Read Sa	avec to file         003         11         000           004         00         000         000           005         00         000         000           006         00         000         000           007         00         000         000           008         0.44         000         000           009         00         000         000	110001 □ 1000000 □ 1000000 □ 1000000 □ 1000000 □ 1000100	
State Machine Teat (CMMS)		000 000 000 011 00 000 <		

Figure 14: Reading Specific Registers from Functional Tests Tab

When clicking "Refresh" in the "Memory Map" tab, the grid displays all data written in the registers and follows the rules above.

MLAnalyzer Kit								×
Help								
multiLane			ML40	66-Analyz	zer Analyzer Typ	e QDD Analyzer 🗸 🗸	Disconnect	
ie is in the second	Refresh Load MSA from file Sav		MSA to file Write MSA to HW					
	Address	Data(Hex)	Data(Dec.)	Data(Ascii)	MSA Description			
ation at a second se	LowMem 0(00h)	18	24	٥	Identifier			
l and i di la companya di la company	LowMem 1(01h)	40	64	0	Version Id			
-	LowMem 2(02h)	00	0		CLEI code present			
	LowMem 3(03h)	07	7	0	Module State			
-	LowMem 4(04h)	00	0		Bank 0			
	LowMem 5(05h)	00	0		Bank 1			
( #	LowMem 6(06h)	00	0		Bank 2			
	LowMem 7(07h)	00	0		Bank 3			
	LowMem 8(USh)	00	0		Module State changed flag			
	LowMem 10(04h)	00	0		Latened VCCS.5/Temp Alarm and Warning			
-	LowMem 11(0Rb)	00	0		Latched Vender Defined Alarm and Warning			
de -	LowMem 12(0(b)	00	0		Perspect			
	LowMem 13(0Db)	00	0		Custom			
-	LowMem 14(0Eb)	10	28		Internally measured Temperature 1 MSB			
	LowMem 15(0Fh)	00	0		Internally measured Temperature 1 LSB			
	LowMem 16(10h)	7F	127	1	Internally measured Supply 3.3v MSB			
	LowMem 17(11h)	OB	11	0	Internally measured Supply 3.3v LSB			
tri/A	LowMem 18(12h)	00	0		Internally measured AUX1 MSB			
5	LowMem 19(13h)	00	0		Internally measured AUX1 LSB			
1	LowMem 20(14h)	00	0		Internally measured AUX2 MSB			
a a a a a a a a a a a a a a a a a a a	LowMem 21(15h)	00	0		Internally measured AUX2 LSB			
MIS)	LowMem 22(16h)	7F	127	1	Internally measured AUX3 MSB			
20	Laureldon (22/17b)	rr.	220	2	Informative management AUX21CD			$\sim$

Figure 15: Internal Master

## Cntrl/Alrm Tab

1. The refresh button gets the Status of the signals at the "Drive" mode and the checkboxes reflect its condition.



Figure 16: Cntrl/Alarm Tab

- 2. Select "Drive" mode for ResetL and toggle the checkbox, the ResetL signal of the module will be activated or deactivated.
- 3. Select "Bypass" mode, from Host try to trigger the ResetL signal. Check the analyzer GUI's status by clicking on "Get" button.
- 4. Select "Analog Monitor" mode and click on the "Analog Monitor" button of ResetL. The graph displays its DC voltage level from the Host side.



Figure 17: Reading ResetL from the Analog Monitor Window

multiLane



5. In the "Pull-Up Resistors" Groupbox, click the "Refresh" button, the values displayed are the values of the pullup resistors at the Host.



Figure 18: Pull-Up Resistor Values



# CMIS State Machine Test

This analyzer test works for all QSFP and QDD modules that are both CMIS 3.0 and CMIS 4.0 compliant. In CMIS 3.0, the test skips the low power if the configuration is set to high when transitioning from state to state. In CMIS 4.0, the transition passes through the low power configuration to get to high power.

The Module State Machine is engaged after module insertion and power on, and thus the test can be started. During the test, different state transitions can be shown and tested by toggling the desired destination state. The Module State Machine is different for devices implementing a paged memory map and those implementing a flat (non-paged) memory map.

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Figure 19: Landing Page for State Machine Test

Upon test initialization, the CMIS compliance version is verified and module type is detected. If the latter is not feasible the test will not start.

# **Paged Memory Modules**

If the detected module implements a paged memory map, the diagram below appears and displays the current state of the module and the transition signals.

Toggle another steady state (Reset, ModuleLowPwr, ModuleReady) to switch to it. State and transition signal changes will appear and events will be logged in the logging box. Logged events can be saved to a text file possessing the module serial number and the time the test was done.

If an error occurs while transitioning, the module will be thrown into a "Fault" state. This state can be exited only by resetting the module.





Figure 20: State Machine Test for Paged Memory Modules

## **Flat Memory Modules**

If the detected module implements a flat (non-paged) memory map, the diagram below appears, displaying the current state of the module and the transition signal.

Toggle any of the steady states (Reset or ModuleReady) to switch between them. State and transition signal changes will appear and events will be logged in the logging box. Logged events can be saved to a text file possessing the module serial number and the time the test was done.

If an error occurs while transitioning, the module will be stuck in the transition state until resetting the module or re-initializing the test.



Figure 21: State Machine Test for Flat Memory Modules



# Appendix I: Analyzer Card Diagram







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