FAIRCHILD SEMICONDUCTOR™

March 1998

100307
Low Power Quint Exclusive OR/NOR Gate

General Description

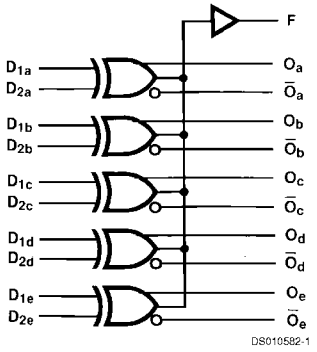
The 100307 is monolithic quint exclusive-OR/NOR gate. The Function output is the wire-OR of all five exclusive-OR outputs. All inputs have 50 kΩ pull-down resistors.

Features

- Low Power Operation
- 2000V ESD protection
- Pin/function compatible with 100107
- Voltage compensated operating range = −4.2V to −5.7V
- Available to industrial grade temperature range
- Available to MIL-STD-883

Ordering Code:

Logic Symbol



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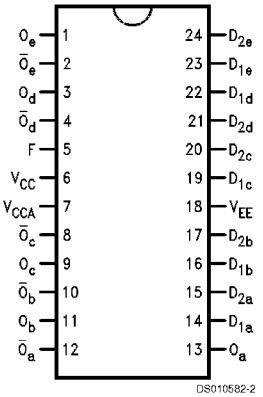
Logic Equation

$F = (D_{1a} \oplus D_{2a}) + (D_{1b} \oplus D_{2b}) + (D_{1c} \oplus D_{2c}) + (D_{1d} \oplus D_{2d}) + (D_{1e} \oplus D_{2e})$.

Pin Names	Description
D_{na}–D_{ne}	Data Inputs
F	Function Output
O_a–O_e	Data Outputs
$\overline{O}_a$–$\overline{O}_e$	Complementary Data Outputs

Connection Diagrams

24-Pin DIP/SOIC



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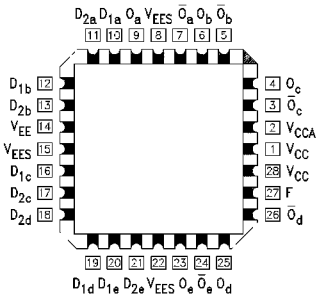
Connection Diagrams (Continued)

28-Pin PCC



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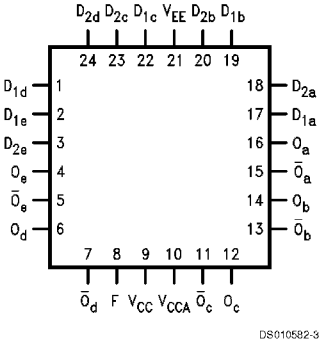
24-Pin Quad Cerpak



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Absolute Maximum Ratings (Note 1)

Above which the useful life may be impaired.

Storage Temperature (T_{STG})	−65°C to +150°C
Maximum Junction Temperature (T_J)	
Ceramic	+175°C
Plastic	+150°C
V_{EE} Pin Potential to Ground Pin	−7.0V to +0.5V
Input Voltage (DC)	V_{EE} to +0.5V
Output Current (DC Output HIGH)	−50 mA
ESD (Note 2)	≥2000V

Recommended Operating Conditions

Case Temperature (T_C)	
Commercial	0°C to +85°C
Industrial	−40°C to +85°C
Military	−55°C to +125°C
Supply Voltage (V_{EE})	−5.7V to −4.2V

Note 1: Absolute maximum ratings are those values beyond which the device may be damaged or have its useful life impaired. Functional operation under these conditions is not implied.

Note 2: ESD testing conforms to MIL-STD-883, Method 3015.

Commercial Version DC Electrical Characteristics

V_{EE} = −4.2V to −5.7V, V_{CC} = V_{CCA} = GND, T_C = 0°C to +85°C (Note 3)

Symbol	Parameter	Min	Typ	Max	Units	Conditions	
V_{OH}	Output HIGH Voltage	−1025	−955	−870	mV	V_{IN} =$V_{IH\ (Max)}$	Loading with
V_{OL}	Output LOW Voltage	−1830	−1705	−1620	mV	or $V_{IL\ (Min)}$	50Ω to −2.0V
V_{OHC}	Output HIGH Voltage	−1035			mV	V_{IN} = $V_{IH\ (Min)}$	Loading with
V_{OLC}	Output LOW Voltage			−1610	mV	or $V_{IL\ (Max)}$	50Ω to −2.0V
V_{IH}	Input HIGH Voltage	−1165		−870	mV	Guaranteed HIGH Signal for All Inputs	
V_{IL}	Input LOW Voltage	−1830		−1475	mV	Guaranteed LOW Signal for All Inputs	
I_{IL}	Input LOW Current	0.50			µA	V_{IN} = $V_{IL\ (Min)}$	
I_{IH}	Input HIGH Current						
	D_{2a}–D_{2e}			250	µA	V_{IN} = V_{IH} (Max)	
	D_{1a}–D_{1e}			350			
I_{EE}	Power Supply Current	−69	−43	−30	mA	Inputs Open	

Note 3: The specified limits represent the "worst case" value for the parameter. Since these values normally occur at the temperature extremes, additional noise immunity and guardbanding can be achieved by decreasing the allowable system operating ranges. Conditions for testing shown in the tables are chosen to guarantee operation under "worst case" conditions.

DIP AC Electrical Characteristics

V_{EE} = −4.2V to −5.7V, V_{CC} = V_{CCA} = GND

Symbol	Parameter	T_C = 0°C		T_C = +25°C		T_C = +85°C		Units	Conditions
		Min	Max	Min	Max	Min	Max		
t_{PLH} t_{PHL}	Propagation Delay D_{2a}–D_{2e} to O, $\overline{O}$	0.55	1.90	0.55	1.80	0.55	1.90	ns	
t_{PLH} t_{PHL}	Propagation Delay D_{1a}–D_{1e} to O, $\overline{O}$	0.55	1.70	0.55	1.60	0.55	1.70	ns	*Figures 1, 2*
t_{PLH} t_{PHL}	Propagation Delay Data to F	1.15	2.75	1.15	2.75	1.15	3.00	ns	
t_{TLH} t_{THL}	Transition Time 20% to 80%, 80% to 20%	0.35	1.20	0.35	1.20	0.35	1.20	ns	

SOIC, PCC and Cerpak AC Electrical Characteristics

V_{EE} = −4.2V to −5.7V, V_{CC} = V_{CCA} = GND

Symbol	Parameter	T_C = 0°C		T_C = +25°C		T_C = +85°C		Units	Conditions
		Min	Max	Min	Max	Min	Max		
t_{PLH} t_{PHL}	Propagation Delay D_{2a}–D_{2e} to O, $\overline{O}$	0.55	1.70	0.55	1.60	0.55	1.70	ns	*Figures 1, 2*
t_{PLH} t_{PHL}	Propagation Delay D_{1a}–D_{1e} to O, $\overline{O}$	0.55	1.50	0.55	1.40	0.55	1.50	ns	
t_{PLH} t_{PHL}	Propagation Delay Data to F	1.15	2.55	1.15	2.55	1.15	2.80	ns	
t_{TLH} t_{THL}	Transition Time 20% to 80%, 80% to 20%	0.35	1.10	0.35	1.10	0.35	1.10	ns	

Industrial Version
PCC DC Electrical Characteristics

V_{EE} = −4.2V to −5.7V, V_{CC} = V_{CCA} = GND, T_C = −40°C to +85°C (Note 4)

Symbol	Parameter	T_C = −40°C		T_C = 0°C to +85°C		Units	Conditions	
		Min	Max	Min	Max			
V_{OH}	Output HIGH Voltage	−1085	−870	−1025	−870	mV	V_{IN} = $V_{IH(Max)}$	Loading with
V_{OL}	Output LOW Voltage	−1830	−1575	−1830	−1620	mV	or $V_{IL(Min)}$	50Ω to −2.0V
V_{OHC}	Output HIGH Voltage	−1095		−1035		mV	V_{IN} = $V_{IH(Min)}$	Loading with
V_{OLC}	Output LOW Voltage		−1565		−1610	mV	or $V_{IL(Max)}$	50Ω to −2.0V
V_{IH}	Input HIGH Voltage	−1170	−870	−1165	−870	mV	Guaranteed HIGH Signal for All Inputs	
V_{IL}	Input LOW Voltage	−1830	−1480	−1830	−1475	mV	Guaranteed LOW Signal for All Inputs	
I_{IL}	Input LOW Current	0.50		0.50		µA	V_{IN} = $V_{IL(Min)}$	
I_{IH}	Input HIGH Current							
	D_{2a}–D_{2e}		250		250	µA	V_{IN} = V_{IH}(Max)	
	D_{1a}–D_{1e}		350		350			
I_{EE}	Power Supply Current	−69	−30	−69	−30	mA	Inputs Open	

Note 4: The specified limits represent the "worst case" value for the parameter. Since these values normally occur at the temperature extremes, additional noise immunity and guardbanding can be achieved by decreasing the allowable system operating ranges. Conditions for testing shown in the tables are chosen to guarantee operation under "worst case" conditions.

PCC AC Electrical Characteristics

V_{EE} = −4.2V to −5.7V, V_{CC} = V_{CCA} = GND

Symbol	Parameter	T_C = −40°C		T_C = +25°C		T_C = +85°C		Units	Conditions
		Min	Max	Min	Max	Min	Max		
t_{PLH} t_{PHL}	Propagation Delay D_{2a}–D_{2e} to O, $\overline{O}$	0.45	1.70	0.55	1.60	0.55	1.70	ns	*Figures 1, 2*
t_{PLH} t_{PHL}	Propagation Delay D_{1a}–D_{1e} to O, $\overline{O}$	0.45	1.50	0.55	1.40	0.55	1.50	ns	
t_{PLH} t_{PHL}	Propagation Delay Data to F	1.05	2.55	1.15	2.55	1.15	2.80	ns	
t_{TLH} t_{THL}	Transition Time 20% to 80%, 80% to 20%	0.35	1.10	0.35	1.10	0.35	1.10	ns	

Military Version
DC Electrical Characteristics

V_{EE} = −4.2V to −5.7V, V_{CC} = V_{CCA} = GND, T_C = −55°C to +125°C

Symbol	Parameter	Min	Max	Units	T_C	Conditions		Notes
V_{OH}	Output HIGH Voltage	−1025	−870	mV	0°C to +125°C	V_{IN} = V_{IH} (Max) or V_{IL} (Min)	Loading with 50Ω to −2.0V	1, 2, 3
		−1085	−870	mV	−55°C			
V_{OL}	Output LOW Voltage	−1830	−1620	mV	0°C to +125°C			
		−1830	−1555	mV	−55°C			
V_{OHC}	Output HIGH Voltage	−1035		mV	0°C to +125°C	V_{IN} = V_{IH} (Min) or V_{IL} (Max)	Loading with 50Ω0 to −2.0V	1, 2, 3
		−1085		mV	−55°C			
V_{OLC}	Output LOW Voltage		−1610	mV	0°C to +125°C			
			−1555	mV	−55°C			
V_{IH}	Input HIGH Voltage	−1165	−870	mV	−55°C +125°C	Guaranteed HIGH Signal for All Inputs		1, 2, 3, 4
V_{IL}	Input LOW Voltage	−1830	−1475	mV	−55°C to +125°C	Guaranteed LOW Signal for All Inputs		1, 2, 3,4
I_{IL}	Input LOW Current	0.50		µA	−55°C to +125°C	V_{EE} = −4.2V V_{IN} = V_{IL} (Min)		1, 2, 3
I_{IH}	Input High Current							
	D_{2a}–D_{2e}		250	µA	0°C to			
	D_{1a}–D_{1e}		350		+125°C	V_{EE} = −5.7V		1, 2, 3
	D_{2a}–D_{2e}		350	µA	−55°C	V_{IN} = V_{IH} (Max)		
	D_{1a}–D_{1e}		500					
I_{EE}	Power Supply Current	−75	−25	mA	−55°C to +125°C	Inputs Open		1, 2, 3

Note 5: F100K 300 Series cold temperature testing is performed by temperature soaking (to guarantee junction temperature equals −55°C), then testing immediately without allowing for the junction temperature to stabilize due to heat dissipation after power-up. This provides "cold start" specs which can be considered a worst case condition at cold temperatures.

Note 6: Screen tested 100% on each device at −55°C, +25°C, and +125°C, Subgroups 1, 2 3, 7, and 8.

Note 7: Sample tested (Method 5005, Table I) on each manufactured lot at −55°C, +25°C, and +125°C, Subgroups A1, 2, 3, 7, and 8.

Note 8: Guaranteed by applying specified input condition and testing V_{OH}/V_{OL}.

AC Electrical Characteristics

V_{EE} = −4.2V to −5.7V, V_{CC} = V_{CCA} = GND

Symbol	Parameter	T_C = −55°C		T_C = +25°C		T_C = +125°C		Units	Conditions	Notes
		Min	Max	Min	Max	Min	Max			
t_{PLH} t_{PHL}	Propagation Delay D_{2a}–D_{2e} to O, $\overline{O}$	0.30	2.10	0.40	1.90	0.40	2.40	ns	*Figures 1, 2*	1, 2, 3
t_{PLH} t_{PHL}	Propagation Delay D_{1a}–D_{1e} to O, $\overline{O}$	0.30	1.90	0.40	1.80	0.40	2.20	ns		
t_{PLH} t_{PHL}	Propagation Delay Data to F	0.80	2.90	0.90	2.80	0.90	3.40	ns		
t_{TLH} t_{THL}	Transition Time 20% to 80%, 80% to 20%	0.20	1.70	0.30	1.60	0.20	1.70	ns		4

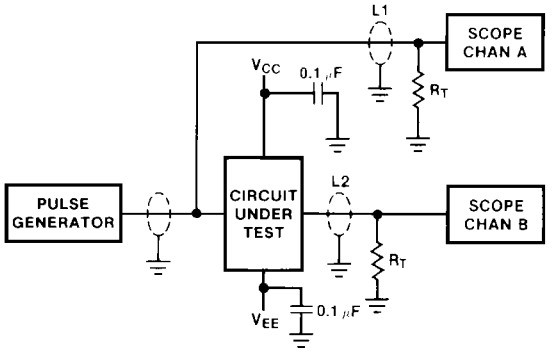
Note 9: F100K 300 Series cold temperature testing is performed by temperature soaking (to guarantee junction temperature equals −55°C), then testing immediately after power-up. This provides "cold start" specs which can be considered a worst case condition at cold temperatures.

Note 10: Screen tested 100% on each device at +25°C temperature only, Subgroup A9.

Note 11: Sample tested (Method 5005, Table I) on each mfg. lot at +25°C, Subgroup A9, and at +125°C and −55°C temperatures, Subgroups A10 and A11.

Note 12: Not tested at +25°C, +125°C, and −55°C temperature (design characterization data).

Test Circuitry



Notes:
V_{CC}, V_{CCA} = +2V, V_{EE} = −2.5V
L1 and L2 = equal length 50Ω impedance lines
R_T = 50Ω terminator internal to scope
Decoupling 0.1 μF from GND to V_{CC} and V_{EE}
All unused outputs are loaded with 50Ω to GND
C_L = Fixture and stray capacitance ≤ 3 pF

FIGURE 1. AC Test Circuit

Switching Waveforms

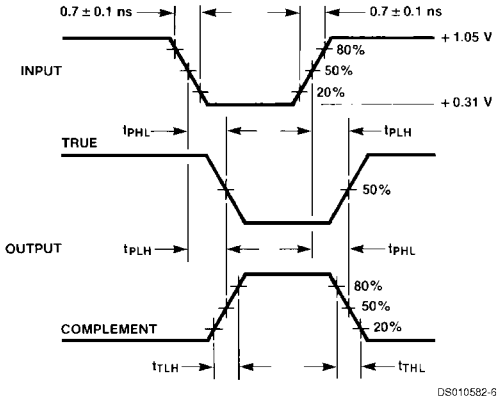
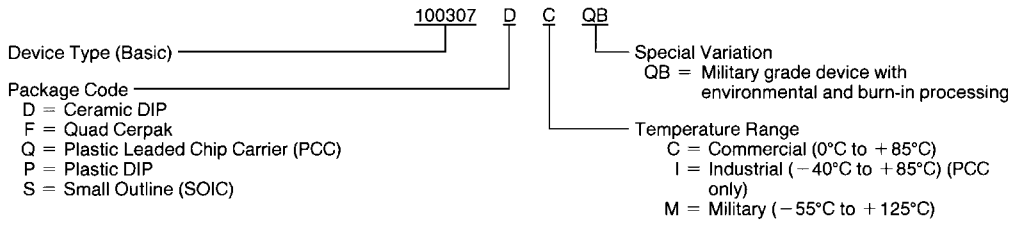


FIGURE 2. Propagation Delay and Transition Times

Ordering Information

The device number is used to form part of a simplified purchasing code where a package type and temperature range are defined as follows:



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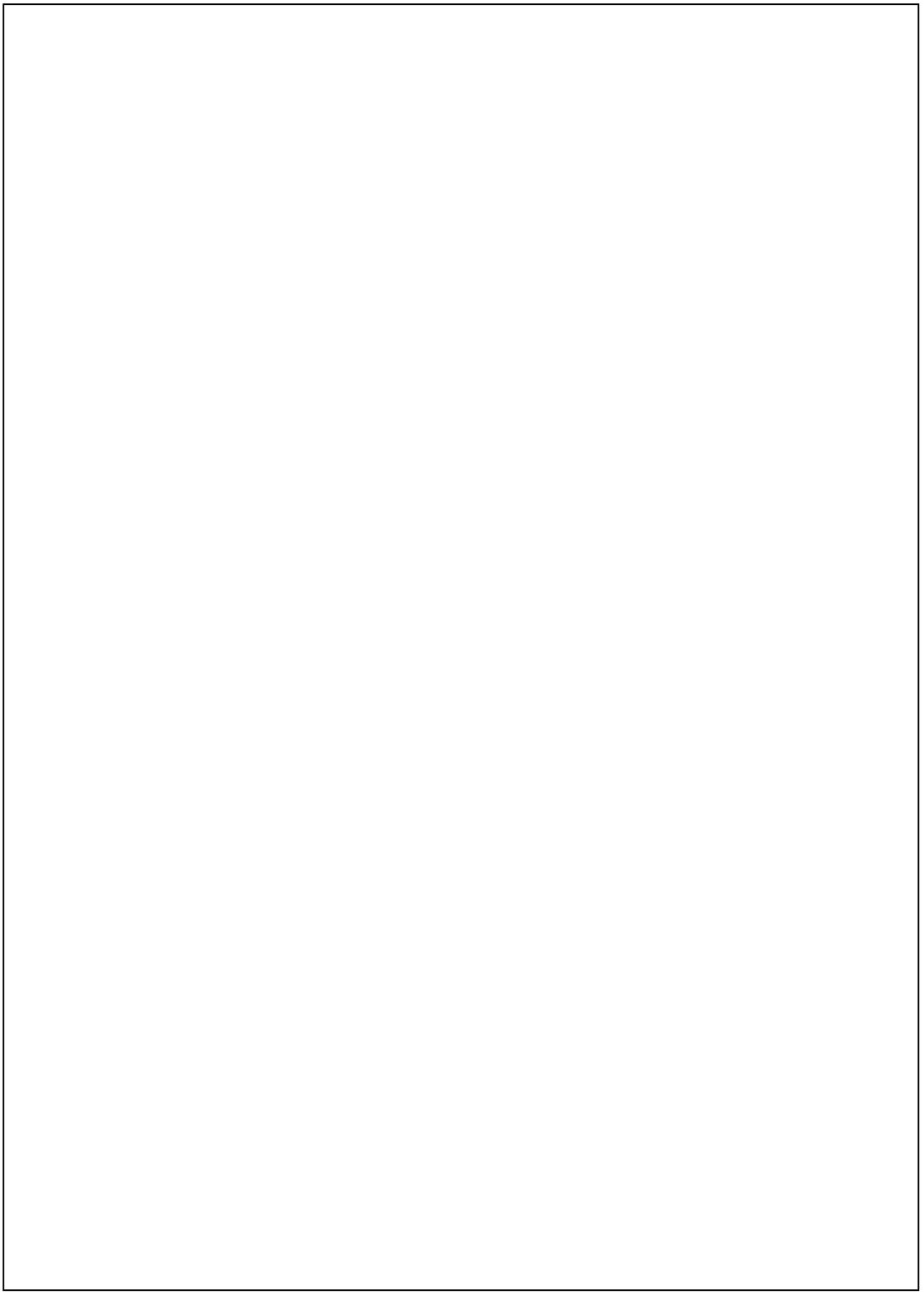
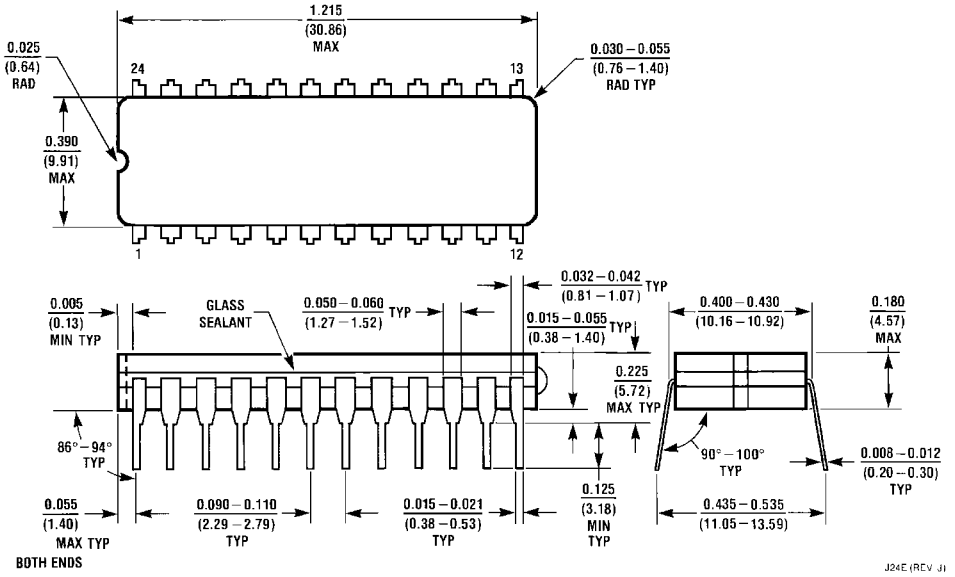
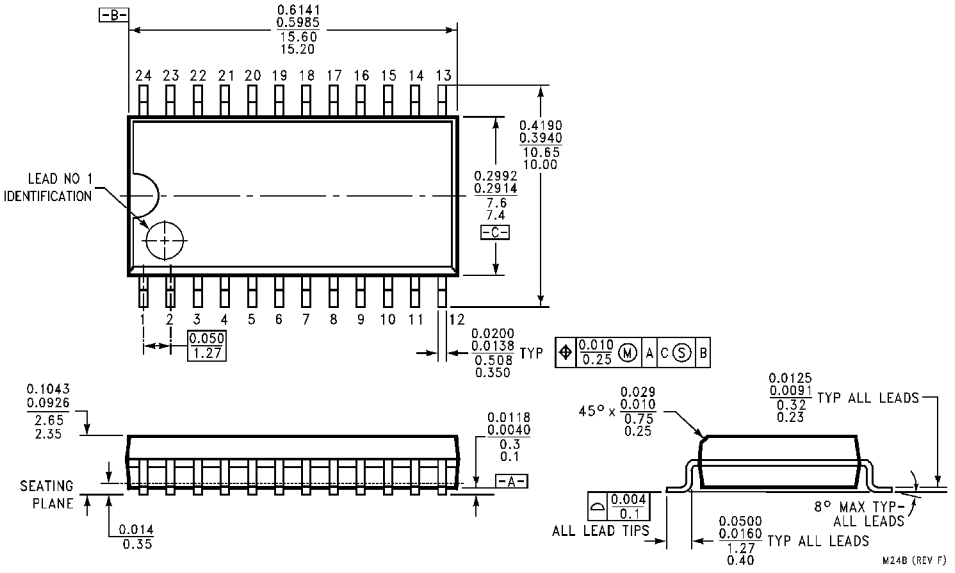


Physical Dimensions inches (millimeters) unless otherwise noted

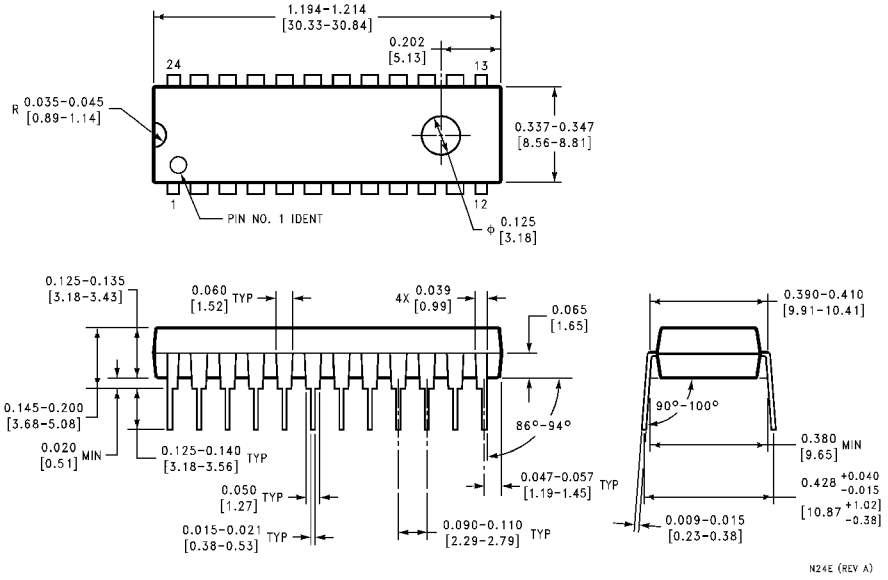


24-Pin Ceramic Dual-In-Line Package (D)
Package Number J24E



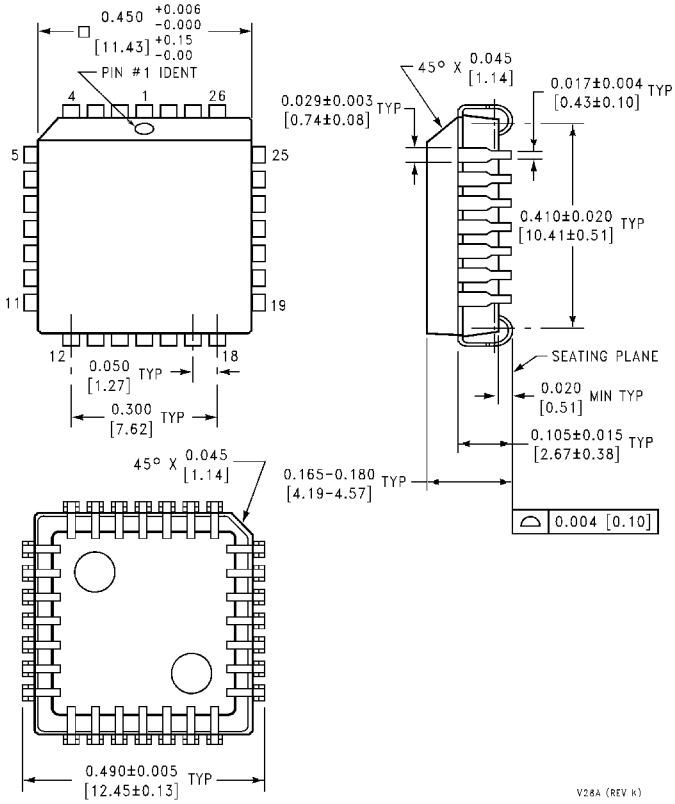
24-Lead Molded Package (0.300" Wide) (S)
Package Number M24B

Physical Dimensions inches (millimeters) unless otherwise noted (Continued)



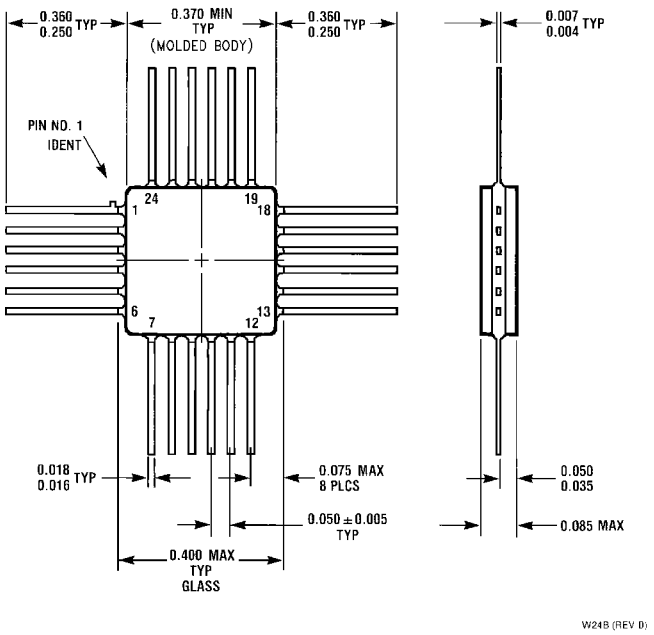
24-Lead Plastic Dual-In-Line Package (P)
Package Number N24E

Physical Dimensions inches (millimeters) unless otherwise noted (Continued)



28-Lead Plastic Leaded Chip Carrier (Q)
Package Number V28A

Physical Dimensions inches (millimeters) unless otherwise noted (Continued)



24-Pin Quad Cerpak (F)
Package Number W24B

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2. A critical component in any component of a life support device or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.

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