

# 74HC4067; 74HCT4067

16-channel analog multiplexer/demultiplexer

Rev. 6 — 22 May 2015

Product data sheet

## 1. General description

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The 74HC4067; 74HCT4067 is a single-pole 16-throw analog switch (SP16T) suitable for use in analog or digital 16:1 multiplexer/demultiplexer applications. The switch features four digital select inputs (S0, S1, S2 and S3), sixteen independent inputs/outputs (Yn), a common input/output (Z) and a digital enable input ( $\bar{E}$ ). When  $\bar{E}$  is HIGH, the switches are turned off. Inputs include clamp diodes. This enables the use of current limiting resistors to interface inputs to voltages in excess of  $V_{CC}$ .

## 2. Features and benefits

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- Input levels S0, S1, S2, S3 and  $\bar{E}$  inputs:
  - ◆ For 74HC4067: CMOS level
  - ◆ For 74HCT4067: TTL level
- Low ON resistance:
  - ◆ 80  $\Omega$  (typical) at  $V_{CC} = 4.5$  V
  - ◆ 70  $\Omega$  (typical) at  $V_{CC} = 6.0$  V
  - ◆ 60  $\Omega$  (typical) at  $V_{CC} = 9.0$  V
- Specified in compliance with JEDEC standard no. 7A
- ESD protection:
  - ◆ HBM JESD22-A114F exceeds 2000 V
  - ◆ MM JESD22-A115-A exceeds 200 V
  - ◆ CDM JESD22-C101E exceeds 1000 V
- Multiple package options
- Specified from  $-40$  °C to  $+85$  °C and  $-40$  °C to  $+125$  °C
- Typical 'break before make' built-in

## 3. Applications

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- Analog multiplexing and demultiplexing
- Digital multiplexing and demultiplexing
- Signal gating

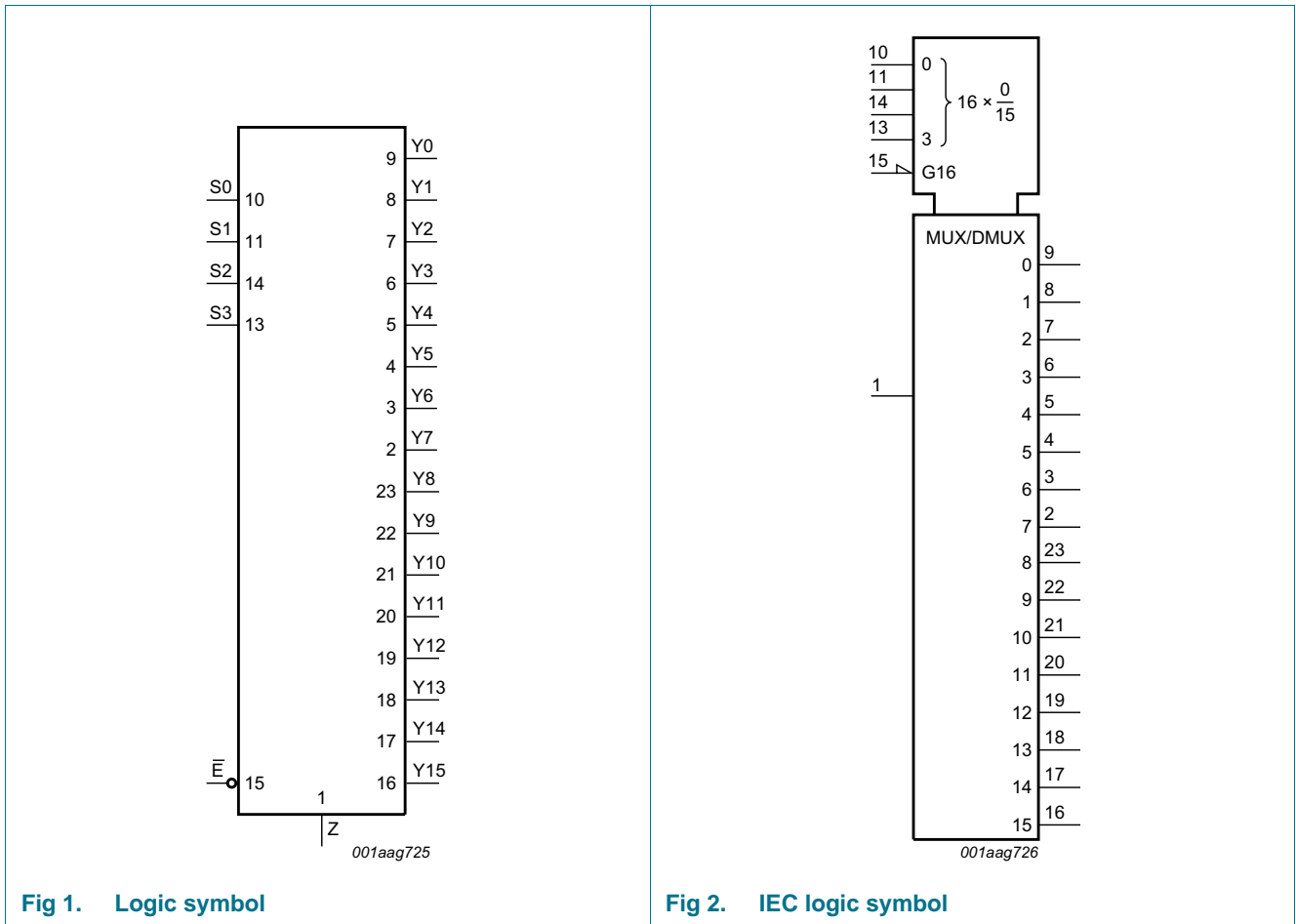


### 4. Ordering information

Table 1. Ordering information

Type number	Package			Version
	Temperature range	Name	Description	
74HC4067D	-40 °C to +125 °C	SO24	plastic small outline package; 24 leads; body width 7.5 mm	SOT137-1
74HCT4067D				
74HC4067DB	-40 °C to +125 °C	SSOP24	plastic shrink small outline package; 24 leads; body width 5.3 mm	SOT340-1
74HCT4067DB				
74HC4067PW	-40 °C to +125 °C	TSSOP24	plastic thin shrink small outline package; 24 leads; body width 4.4 mm	SOT355-1
74HCT4067PW				
74HC4067BQ	-40 °C to +125 °C	DHVQFN24	plastic dual in-line compatible thermal enhanced very thin quad flat package; no leads; 24 terminals; body 3.5 × 5.5 × 0.85 mm	SOT815-1
74HCT4067BQ				

### 5. Functional diagram



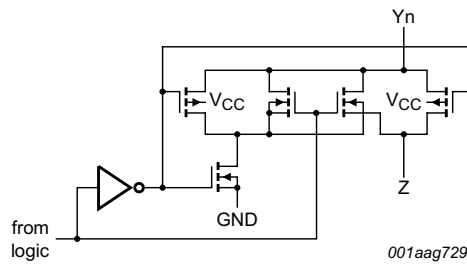


Fig 3. Schematic diagram (one switch)

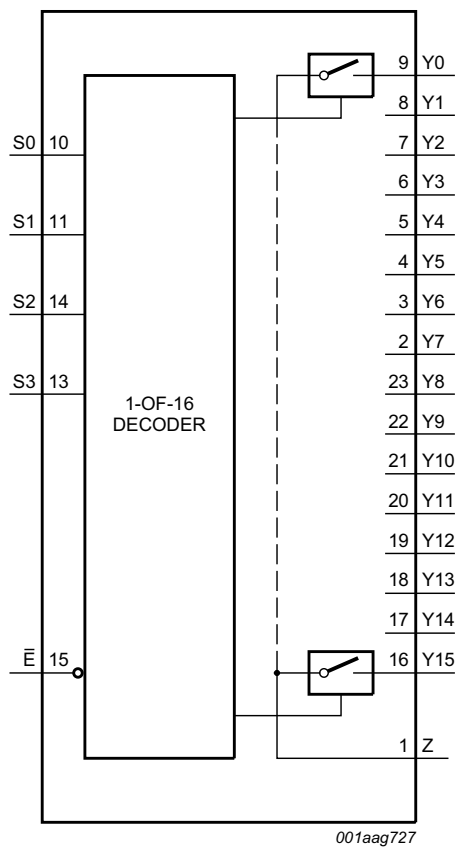


Fig 4. Functional diagram

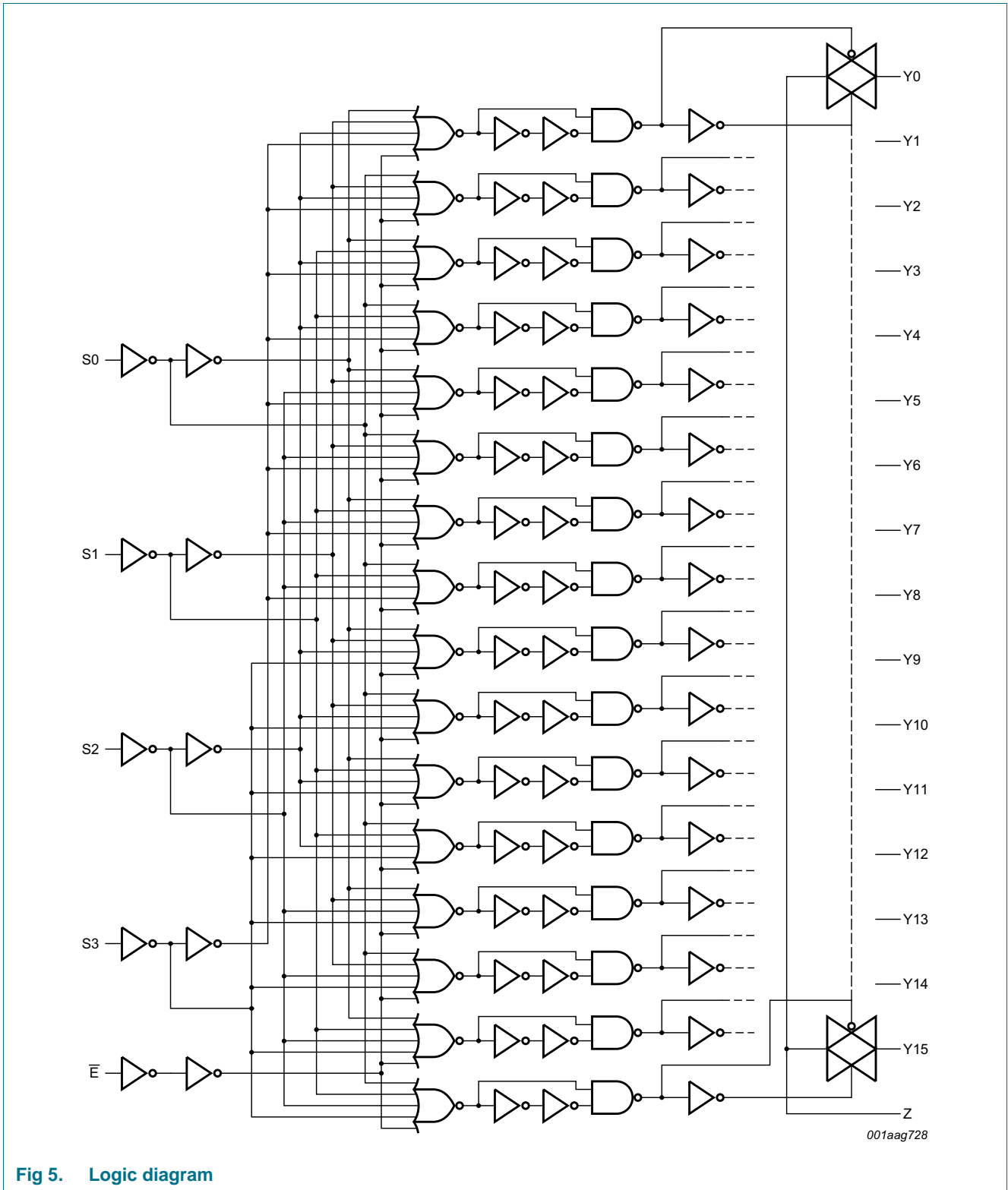
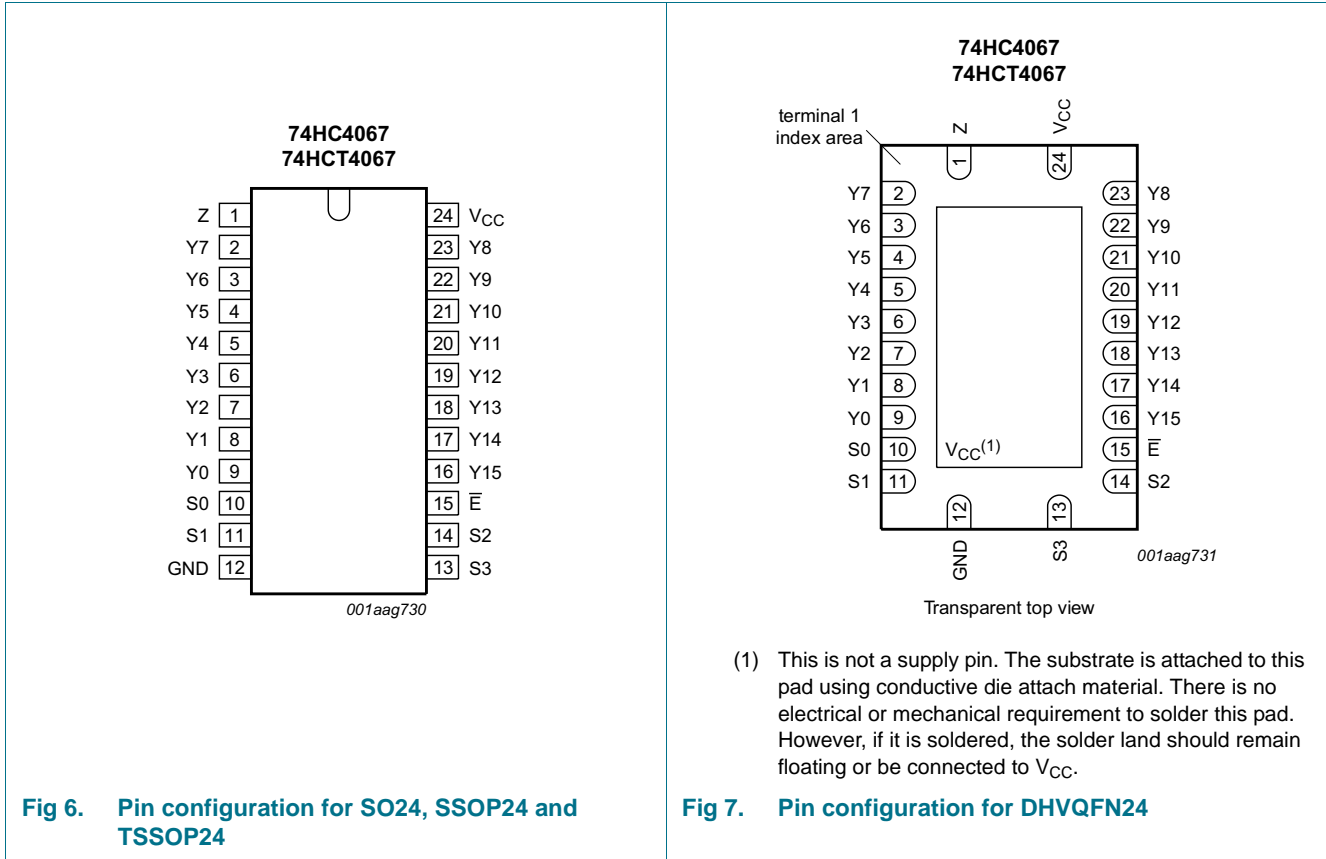


Fig 5. Logic diagram

6. Pinning information

6.1 Pinning



6.2 Pin description

Table 2. Pin description

Symbol	Pin	Description
Z	1	common input or output
Y7, Y6, Y5, Y4, Y3, Y2, Y1, Y0, Y15, Y14, Y13, Y12, Y11, Y10, Y9, Y8	2, 3, 4, 5, 6, 7, 8, 9, 16, 17, 18, 19, 20, 21, 22, 23	independent input or output
S0, S1, S3, S2	10, 11, 13, 14	address input 0
GND	12	ground (0 V)
$\bar{E}$	15	enable input (active LOW)
V <sub>CC</sub>	24	supply voltage

## 7. Functional description

Table 3. Function table<sup>[1]</sup>

Inputs					Channel ON
$\bar{E}$	S3	S2	S1	S0	
L	L	L	L	L	Y0 to Z
L	L	L	L	H	Y1 to Z
L	L	L	H	L	Y2 to Z
L	L	L	H	H	Y3 to Z
L	L	H	L	L	Y4 to Z
L	L	H	L	H	Y5 to Z
L	L	H	H	L	Y6 to Z
L	L	H	H	H	Y7 to Z
L	H	L	L	L	Y8 to Z
L	H	L	L	H	Y9 to Z
L	H	L	H	L	Y10 to Z
L	H	L	H	H	Y11 to Z
L	H	H	L	L	Y12 to Z
L	H	H	L	H	Y13 to Z
L	H	H	H	L	Y14 to Z
L	H	H	H	H	Y15 to Z
H	X	X	X	X	-

- [1] H = HIGH voltage level;  
L = LOW voltage level;  
X = don't care.

## 8. Limiting values

Table 4. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134). Voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	Min	Max	Unit
$V_{CC}$	supply voltage	[1]	-0.5	+11.0	V
$I_{IK}$	input clamping current	$V_I < -0.5\text{ V}$ or $V_I > V_{CC} + 0.5\text{ V}$	-	$\pm 20$	mA
$I_{SK}$	switch clamping current	$V_{SW} < -0.5\text{ V}$ or $V_{SW} > V_{CC} + 0.5\text{ V}$	-	$\pm 20$	mA
$I_{SW}$	switch current	$V_{SW} = -0.5\text{ V}$ to $V_{CC} + 0.5\text{ V}$	-	$\pm 25$	mA
$I_{CC}$	supply current		-	+50	mA
$I_{GND}$	ground current		-50	-	mA
$T_{stg}$	storage temperature		-65	+150	°C

**Table 4. Limiting values ...continued**

In accordance with the Absolute Maximum Rating System (IEC 60134). Voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	Min	Max	Unit
P <sub>tot</sub>	total power dissipation	T <sub>amb</sub> = -40 °C to +125 °C			
		SO24 package <a href="#">[2]</a>	-	500	mW
		SSOP24 package <a href="#">[3]</a>	-	500	mW
		TSSOP24 package <a href="#">[3]</a>	-	500	mW
		DHVQFN24 package <a href="#">[4]</a>	-	500	mW
P	power dissipation	per switch	-	100	mW

- [1] To avoid drawing V<sub>CC</sub> current out of terminal Z, when switch current flows in terminals Y<sub>n</sub>, the voltage drop across the bidirectional switch must not exceed 0.4 V. If the switch current flows into terminal Z, no V<sub>CC</sub> current will flow out of terminals Y<sub>n</sub>. In this case there is no limit for the voltage drop across the switch, but the voltages at Y<sub>n</sub> and Z may not exceed V<sub>CC</sub> or GND.
- [2] For SO24 package: P<sub>tot</sub> derates linearly with 8 mW/K above 70 °C.
- [3] For SSOP24 and TSSOP24 packages: P<sub>tot</sub> derates linearly with 5.5 mW/K above 60 °C.
- [4] For DHVQFN24 package: P<sub>tot</sub> derates linearly with 4.5 mW/K above 60 °C.

## 9. Recommended operating conditions

**Table 5. Recommended operating conditions**

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
<b>74HC4067</b>						
V <sub>CC</sub>	supply voltage		2.0	5.0	10.0	V
V <sub>I</sub>	input voltage		GND	-	V <sub>CC</sub>	V
V <sub>SW</sub>	switch voltage		GND	-	V <sub>CC</sub>	V
Δt/ΔV	input transition rise and fall rate	V <sub>CC</sub> = 2.0 V	-	-	625	ns
		V <sub>CC</sub> = 4.5 V	-	1.67	139	ns
		V <sub>CC</sub> = 6.0 V	-	-	83	ns
		V <sub>CC</sub> = 10.0 V	-	-	31	ns
T <sub>amb</sub>	ambient temperature		-40	+25	+125	°C
<b>74HCT4067</b>						
V <sub>CC</sub>	supply voltage		4.5	5.0	5.5	V
V <sub>I</sub>	input voltage		GND	-	V <sub>CC</sub>	V
V <sub>SW</sub>	switch voltage		GND	-	V <sub>CC</sub>	V
Δt/ΔV	input transition rise and fall rate	V <sub>CC</sub> = 4.5 V	-	1.67	139	ns
T <sub>amb</sub>	ambient temperature		-40	+25	+125	°C

## 10. Static characteristics

**Table 6.**  $R_{ON}$  resistance per switch for types 74HC4067 and 74HCT4067

$V_I = V_{IH}$  or  $V_{IL}$ ; for test circuit see [Figure 8](#).

$V_{is}$  is the input voltage at a Yn or Z terminal, whichever is assigned as an input.

$V_{os}$  is the output voltage at a Yn or Z terminal, whichever is assigned as an output.

For 74HC4067:  $V_{CC} - GND = 2.0\text{ V}, 4.5\text{ V}, 6.0\text{ V}$  and  $9.0\text{ V}$ .

For 74HCT4067:  $V_{CC} - GND = 4.5\text{ V}$ .

Symbol	Parameter	Conditions	25 °C		-40 °C to +125 °C		Unit
			Typ	Max	Max (85 °C)	Max (125 °C)	
$R_{ON(peak)}$	ON resistance (peak)	$V_{is} = V_{CC}$ to GND					
		$V_{CC} = 2.0\text{ V}; I_{SW} = 100\ \mu\text{A}$ <a href="#">[1]</a>	-	-	-	-	$\Omega$
		$V_{CC} = 4.5\text{ V}; I_{SW} = 1000\ \mu\text{A}$	110	180	225	270	$\Omega$
		$V_{CC} = 6.0\text{ V}; I_{SW} = 1000\ \mu\text{A}$	95	160	200	240	$\Omega$
		$V_{CC} = 9.0\text{ V}; I_{SW} = 1000\ \mu\text{A}$	75	130	165	195	$\Omega$
$R_{ON(rail)}$	ON resistance (rail)	$V_{is} = GND$ or $V_{CC}$					
		$V_{CC} = 2.0\text{ V}; I_{SW} = 100\ \mu\text{A}$ <a href="#">[1]</a>	150	-	-	-	
		$V_{CC} = 4.5\text{ V}; I_{SW} = 1000\ \mu\text{A}$	90	160	200	240	$\Omega$
		$V_{CC} = 6.0\text{ V}; I_{SW} = 1000\ \mu\text{A}$	80	140	175	210	$\Omega$
		$V_{CC} = 9.0\text{ V}; I_{SW} = 1000\ \mu\text{A}$	70	120	150	180	$\Omega$
$\Delta R_{ON}$	ON resistance mismatch between channels	$V_{is} = V_{CC}$ to GND					
		$V_{CC} = 2.0\text{ V}$ <a href="#">[1]</a>	-	-	-	-	$\Omega$
		$V_{CC} = 4.5\text{ V}$	9	-	-	-	$\Omega$
		$V_{CC} = 6.0\text{ V}$	8	-	-	-	$\Omega$
		$V_{CC} = 9.0\text{ V}$	6	-	-	-	$\Omega$

[1] At supply voltages ( $V_{CC} - GND$ ) approaching 2 V, the analog switch ON resistance becomes extremely non-linear. Therefore it is recommended that these devices be used to transmit digital signals only, when using these supply voltages.



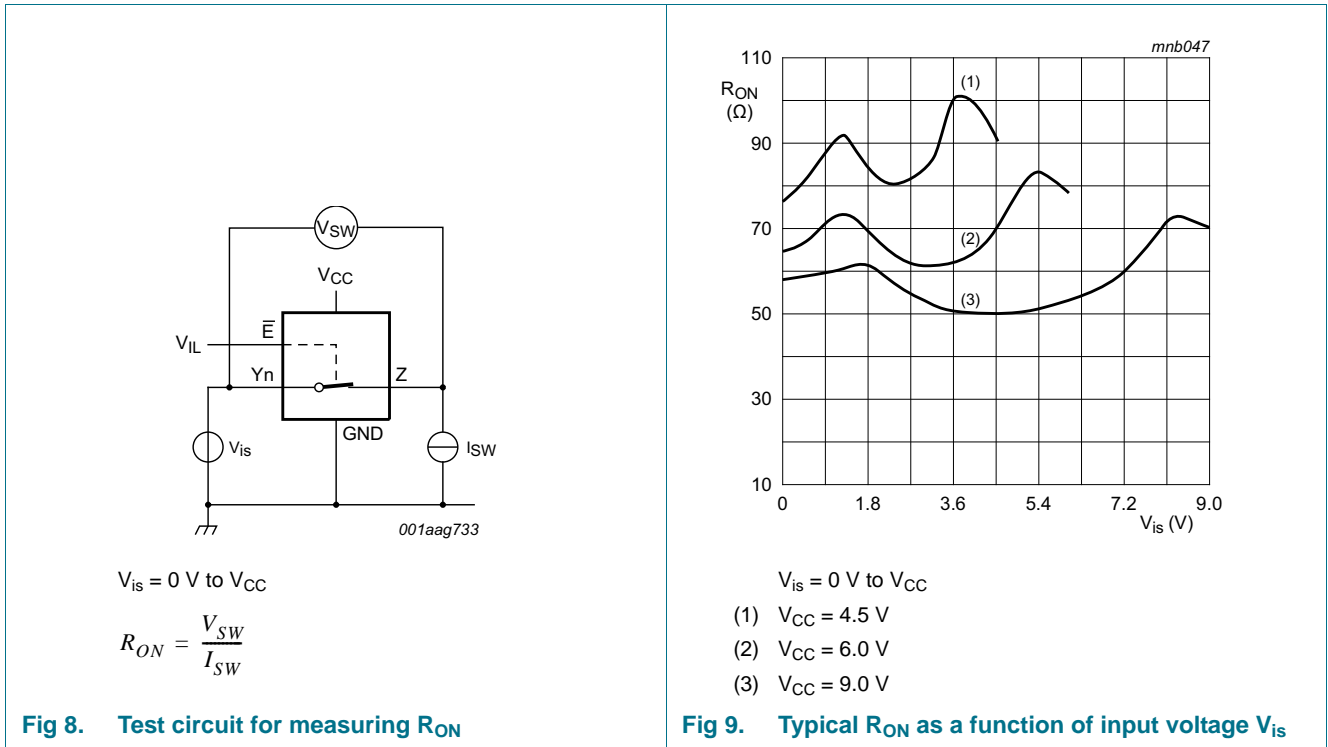


Table 7. Static characteristics 74HC4067

At recommended operating conditions; voltages are referenced to GND (ground = 0 V).  
 Vis is the input voltage at a Yn or Z terminal, whichever is assigned as an input.  
 Vos is the output voltage at a Yn or Z terminal, whichever is assigned as an output.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
<b>T<sub>amb</sub> = 25 °C</b>						
VIH	HIGH-level input voltage	VCC = 2.0 V	1.5	1.2	-	V
		VCC = 4.5 V	3.15	2.4	-	V
		VCC = 6.0 V	4.2	3.2	-	V
		VCC = 9.0 V	6.3	4.7	-	V
VIL	LOW-level input voltage	VCC = 2.0 V	-	0.8	0.5	V
		VCC = 4.5 V	-	2.1	1.35	V
		VCC = 6.0 V	-	2.8	1.80	V
		VCC = 9.0 V	-	4.3	2.70	V
II	input leakage current	VI = VCC or GND				
		VCC = 6.0 V	-	-	±0.1	μA
		VCC = 10.0 V	-	-	±0.2	μA
IS(OFF)	OFF-state leakage current	VCC = 10.0 V; VI = VIH or VIL;  Vsw  = VCC - GND; see <a href="#">Figure 10</a>				
		per channel	-	-	±0.1	μA
		all channels	-	-	±0.8	μA
IS(ON)	ON-state leakage current	VCC = 10.0 V; VI = VIH or VIL;  Vsw  = VCC - GND; see <a href="#">Figure 11</a>	-	-	±0.8	μA

**Table 7. Static characteristics 74HC4067 ...continued**

At recommended operating conditions; voltages are referenced to GND (ground = 0 V).

$V_{is}$  is the input voltage at a Yn or Z terminal, whichever is assigned as an input.

$V_{os}$  is the output voltage at a Yn or Z terminal, whichever is assigned as an output.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$I_{CC}$	supply current	$V_I = V_{CC}$ or GND; $V_{is} =$ GND or $V_{CC}$ ; $V_{os} = V_{CC}$ or GND				
		$V_{CC} = 6.0$ V	-	-	8.0	$\mu$ A
		$V_{CC} = 10.0$ V	-	-	16.0	$\mu$ A
$C_I$	input capacitance		-	3.5	-	pF
<b><math>T_{amb} = -40</math> °C to <math>+85</math> °C</b>						
$V_{IH}$	HIGH-level input voltage	$V_{CC} = 2.0$ V	1.5	-	-	V
		$V_{CC} = 4.5$ V	3.15	-	-	V
		$V_{CC} = 6.0$ V	4.2	-	-	V
		$V_{CC} = 9.0$ V	6.3	-	-	V
$V_{IL}$	LOW-level input voltage	$V_{CC} = 2.0$ V	-	-	0.50	V
		$V_{CC} = 4.5$ V	-	-	1.35	V
		$V_{CC} = 6.0$ V	-	-	1.80	V
		$V_{CC} = 9.0$ V	-	-	2.70	V
$I_I$	input leakage current	$V_I = V_{CC}$ or GND				
		$V_{CC} = 6.0$ V	-	-	$\pm 1.0$	$\mu$ A
		$V_{CC} = 10.0$ V	-	-	$\pm 2.0$	$\mu$ A
$I_{S(OFF)}$	OFF-state leakage current	$V_{CC} = 10.0$ V; $V_I = V_{IH}$ or $V_{IL}$ ; $ V_{SW}  = V_{CC} - \text{GND}$ ; see <a href="#">Figure 10</a>				
		per channel	-	-	$\pm 1.0$	$\mu$ A
		all channels	-	-	$\pm 8.0$	$\mu$ A
$I_{S(ON)}$	ON-state leakage current	$V_{CC} = 10.0$ V; $V_I = V_{IH}$ or $V_{IL}$ ; $ V_{SW}  = V_{CC} - \text{GND}$ ; see <a href="#">Figure 11</a>	-	-	$\pm 8.0$	$\mu$ A
$I_{CC}$	supply current	$V_I = V_{CC}$ or GND; $V_{is} =$ GND or $V_{CC}$ ; $V_{os} = V_{CC}$ or GND				
		$V_{CC} = 6.0$ V	-	-	80.0	$\mu$ A
		$V_{CC} = 10.0$ V	-	-	160	$\mu$ A
<b><math>T_{amb} = -40</math> °C to <math>+125</math> °C</b>						
$V_{IH}$	HIGH-level input voltage	$V_{CC} = 2.0$ V	1.5	-	-	V
		$V_{CC} = 4.5$ V	3.15	-	-	V
		$V_{CC} = 6.0$ V	4.2	-	-	V
		$V_{CC} = 9.0$ V	6.3	-	-	V
$V_{IL}$	LOW-level input voltage	$V_{CC} = 2.0$ V	-	-	0.50	V
		$V_{CC} = 4.5$ V	-	-	1.35	V
		$V_{CC} = 6.0$ V	-	-	1.80	V
		$V_{CC} = 9.0$ V	-	-	2.70	V
$I_I$	input leakage current	$V_I = V_{CC}$ or GND				
		$V_{CC} = 6.0$ V	-	-	$\pm 1.0$	$\mu$ A
		$V_{CC} = 10.0$ V	-	-	$\pm 2.0$	$\mu$ A

**Table 7. Static characteristics 74HC4067 ...continued**

At recommended operating conditions; voltages are referenced to GND (ground = 0 V).

$V_{is}$  is the input voltage at a Yn or Z terminal, whichever is assigned as an input.

$V_{os}$  is the output voltage at a Yn or Z terminal, whichever is assigned as an output.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$I_{S(OFF)}$	OFF-state leakage current	$V_{CC} = 10.0\text{ V}$ ; $V_I = V_{IH}$ or $V_{IL}$ ; $ V_{SW}  = V_{CC} - \text{GND}$ ; see <a href="#">Figure 10</a>				
		per channel	-	-	$\pm 1.0$	$\mu\text{A}$
		all channels	-	-	$\pm 8.0$	$\mu\text{A}$
$I_{S(ON)}$	ON-state leakage current	$V_{CC} = 10.0\text{ V}$ ; $V_I = V_{IH}$ or $V_{IL}$ ; $ V_{SW}  = V_{CC} - \text{GND}$ ; see <a href="#">Figure 11</a>	-	-	$\pm 8.0$	$\mu\text{A}$
$I_{CC}$	supply current	$V_I = V_{CC}$ or GND; $V_{is} = \text{GND}$ or $V_{CC}$ ; $V_{os} = V_{CC}$ or GND				
		$V_{CC} = 6.0\text{ V}$	-	-	160	$\mu\text{A}$
		$V_{CC} = 10.0\text{ V}$	-	-	320	$\mu\text{A}$

**Table 8. Static characteristics 74HCT4067**

At recommended operating conditions; voltages are referenced to GND (ground = 0 V).

$V_{is}$  is the input voltage at a Yn or Z terminal, whichever is assigned as an input.

$V_{os}$  is the output voltage at a Yn or Z terminal, whichever is assigned as an output.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
<b><math>T_{amb} = 25\text{ }^\circ\text{C}</math></b>						
$V_{IH}$	HIGH-level input voltage	$V_{CC} = 4.5\text{ V to }5.5\text{ V}$	2.0	1.6	-	V
$V_{IL}$	LOW-level input voltage	$V_{CC} = 4.5\text{ V to }5.5\text{ V}$	-	1.2	0.8	V
$I_I$	input leakage current	$V_I = V_{CC}$ or GND; $V_{CC} = 5.5\text{ V}$	-	-	$\pm 0.1$	$\mu\text{A}$
$I_{S(OFF)}$	OFF-state leakage current	$V_{CC} = 5.5\text{ V}$ ; $V_I = V_{IH}$ or $V_{IL}$ ; $ V_{SW}  = V_{CC} - \text{GND}$ ; see <a href="#">Figure 10</a>				
		per channel	-	-	$\pm 0.1$	$\mu\text{A}$
		all channels	-	-	$\pm 0.8$	$\mu\text{A}$
$I_{S(ON)}$	ON-state leakage current	$V_{CC} = 5.5\text{ V}$ ; $V_I = V_{IH}$ or $V_{IL}$ ; $ V_{SW}  = V_{CC} - \text{GND}$ ; see <a href="#">Figure 11</a>	-	-	$\pm 0.8$	$\mu\text{A}$
$I_{CC}$	supply current	$V_I = V_{CC}$ or GND; $V_{is} = \text{GND}$ or $V_{CC}$ ; $V_{os} = V_{CC}$ or GND; $V_{CC} = 4.5\text{ V to }5.5\text{ V}$	-	-	8.0	$\mu\text{A}$
$\Delta I_{CC}$	additional supply current	per input pin; $V_I = V_{CC} - 2.1\text{ V}$ ; other inputs at $V_{CC}$ or GND; $V_{CC} = 4.5\text{ V to }5.5\text{ V}$				
		pin $\bar{E}$	-	60	216	$\mu\text{A}$
		pin Sn	-	50	180	$\mu\text{A}$
$C_I$	input capacitance		-	3.5	-	pF
<b><math>T_{amb} = -40\text{ }^\circ\text{C to }+85\text{ }^\circ\text{C}</math></b>						
$V_{IH}$	HIGH-level input voltage	$V_{CC} = 4.5\text{ V to }5.5\text{ V}$	2.0	-	-	V
$V_{IL}$	LOW-level input voltage	$V_{CC} = 4.5\text{ V to }5.5\text{ V}$	-	-	0.8	V
$I_I$	input leakage current	$V_I = V_{CC}$ or GND; $V_{CC} = 5.5\text{ V}$	-	-	$\pm 1.0$	$\mu\text{A}$
$I_{S(OFF)}$	OFF-state leakage current	$V_{CC} = 5.5\text{ V}$ ; $V_I = V_{IH}$ or $V_{IL}$ ; $ V_{SW}  = V_{CC} - \text{GND}$ ; see <a href="#">Figure 10</a>				
		per channel	-	-	$\pm 1.0$	$\mu\text{A}$
		all channels	-	-	$\pm 8.0$	$\mu\text{A}$

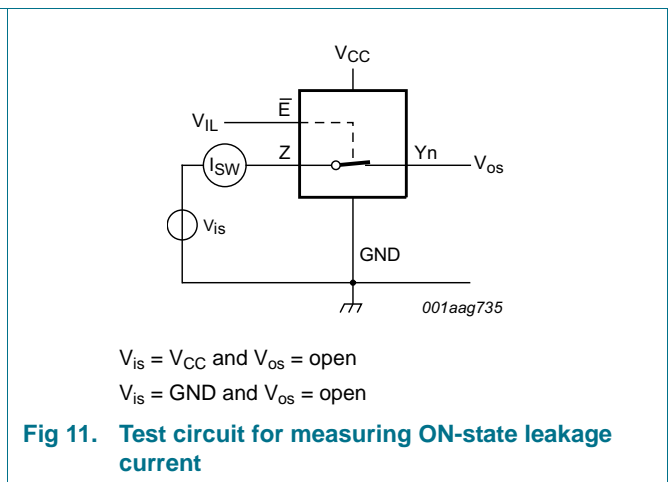
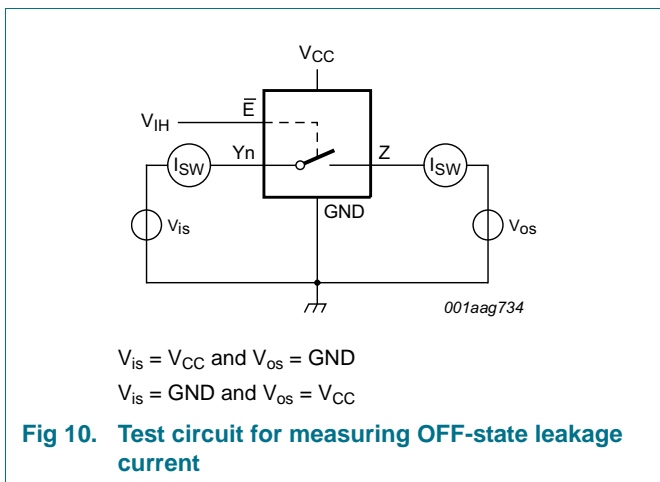
**Table 8. Static characteristics 74HCT4067 ...continued**

At recommended operating conditions; voltages are referenced to GND (ground = 0 V).

$V_{is}$  is the input voltage at a  $Y_n$  or  $Z$  terminal, whichever is assigned as an input.

$V_{os}$  is the output voltage at a  $Y_n$  or  $Z$  terminal, whichever is assigned as an output.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$I_{S(ON)}$	ON-state leakage current	$V_{CC} = 5.5\text{ V}$ ; $V_I = V_{IH}$ or $V_{IL}$ ; $ V_{SW}  = V_{CC} - \text{GND}$ ; see <a href="#">Figure 11</a>	-	-	$\pm 8.0$	$\mu\text{A}$
$I_{CC}$	supply current	$V_I = V_{CC}$ or $\text{GND}$ ; $V_{is} = \text{GND}$ or $V_{CC}$ ; $V_{os} = V_{CC}$ or $\text{GND}$ ; $V_{CC} = 4.5\text{ V}$ to $5.5\text{ V}$	-	-	80.0	$\mu\text{A}$
$\Delta I_{CC}$	additional supply current	per input pin; $V_I = V_{CC} - 2.1\text{ V}$ ; other inputs at $V_{CC}$ or $\text{GND}$ ; $V_{CC} = 4.5\text{ V}$ to $5.5\text{ V}$				
		pin $\bar{E}$	-	-	270	$\mu\text{A}$
		pin Sn	-	-	225	$\mu\text{A}$
<b><math>T_{amb} = -40\text{ }^\circ\text{C}</math> to <math>+125\text{ }^\circ\text{C}</math></b>						
$V_{IH}$	HIGH-level input voltage	$V_{CC} = 4.5\text{ V}$ to $5.5\text{ V}$	2.0	-	-	V
$V_{IL}$	LOW-level input voltage	$V_{CC} = 4.5\text{ V}$ to $5.5\text{ V}$	-	-	0.8	V
$I_I$	input leakage current	$V_I = V_{CC}$ or $\text{GND}$ ; $V_{CC} = 5.5\text{ V}$	-	-	$\pm 1.0$	$\mu\text{A}$
$I_{S(OFF)}$	OFF-state leakage current	$V_{CC} = 5.5\text{ V}$ ; $V_I = V_{IH}$ or $V_{IL}$ ; $ V_{SW}  = V_{CC} - \text{GND}$ ; see <a href="#">Figure 10</a>				
		per channel	-	-	$\pm 1.0$	$\mu\text{A}$
		all channels	-	-	$\pm 8.0$	$\mu\text{A}$
$I_{S(ON)}$	ON-state leakage current	$V_{CC} = 5.5\text{ V}$ ; $V_I = V_{IH}$ or $V_{IL}$ ; $ V_{SW}  = V_{CC} - \text{GND}$ ; see <a href="#">Figure 11</a>	-	-	$\pm 8.0$	$\mu\text{A}$
$I_{CC}$	supply current	$V_I = V_{CC}$ or $\text{GND}$ ; $V_{is} = \text{GND}$ or $V_{CC}$ ; $V_{os} = V_{CC}$ or $\text{GND}$ ; $V_{CC} = 4.5\text{ V}$ to $5.5\text{ V}$	-	-	160	$\mu\text{A}$
$\Delta I_{CC}$	additional supply current	per input pin; $V_I = V_{CC} - 2.1\text{ V}$ ; other inputs at $V_{CC}$ or $\text{GND}$ ; $V_{CC} = 4.5\text{ V}$ to $5.5\text{ V}$				
		pin $\bar{E}$	-	-	294	$\mu\text{A}$
		pin Sn	-	-	245	$\mu\text{A}$



## 11. Dynamic characteristics

**Table 9. Dynamic characteristics 74HC4067**

$GND = 0\text{ V}$ ;  $t_r = t_f = 6\text{ ns}$ ;  $C_L = 50\text{ pF}$  unless specified otherwise; for test circuit see [Figure 14](#).

$V_{is}$  is the input voltage at a  $Y_n$  or  $Z$  terminal, whichever is assigned as an input.

$V_{os}$  is the output voltage at a  $Y_n$  or  $Z$  terminal, whichever is assigned as an output.

Symbol	Parameter	Conditions	25 °C		-40 °C to +125 °C		Unit
			Typ	Max	Max (85 °C)	Max (125 °C)	
$t_{pd}$	propagation delay	$Y_n$ to $Z$ ; see <a href="#">Figure 12</a> <span style="float:right">[1][2]</span>					
		$V_{CC} = 2.0\text{ V}$	25	75	95	110	ns
		$V_{CC} = 4.5\text{ V}$	9	15	19	22	ns
		$V_{CC} = 6.0\text{ V}$	7	13	16	19	ns
		$V_{CC} = 9.0\text{ V}$	5	9	11	14	ns
		$Z$ to $Y_n$					
		$V_{CC} = 2.0\text{ V}$	18	60	75	90	ns
		$V_{CC} = 4.5\text{ V}$	6	12	15	18	ns
		$V_{CC} = 6.0\text{ V}$	5	10	13	15	ns
		$V_{CC} = 9.0\text{ V}$	4	8	10	12	ns
$t_{off}$	turn-off time	$\bar{E}$ to $Y_n$ ; see <a href="#">Figure 13</a> <span style="float:right">[3]</span>					
		$V_{CC} = 2.0\text{ V}$	74	250	315	375	ns
		$V_{CC} = 4.5\text{ V}$	27	50	63	75	ns
		$V_{CC} = 5.0\text{ V}$ ; $C_L = 15\text{ pF}$	27	-	-	-	ns
		$V_{CC} = 6.0\text{ V}$	22	43	54	64	ns
		$V_{CC} = 9.0\text{ V}$	20	38	48	57	ns
		$S_n$ to $Y_n$					
		$V_{CC} = 2.0\text{ V}$	83	250	315	375	ns
		$V_{CC} = 4.5\text{ V}$	30	50	63	75	ns
		$V_{CC} = 5.0\text{ V}$ ; $C_L = 15\text{ pF}$	29	-	-	-	ns
		$V_{CC} = 6.0\text{ V}$	24	43	54	64	ns
		$V_{CC} = 9.0\text{ V}$	21	38	48	57	ns
		$\bar{E}$ to $Z$					
		$V_{CC} = 2.0\text{ V}$	85	275	345	415	ns
		$V_{CC} = 4.5\text{ V}$	31	55	69	83	ns
		$V_{CC} = 6.0\text{ V}$	25	47	59	71	ns
		$V_{CC} = 9.0\text{ V}$	24	42	53	63	ns
		$S_n$ to $Z$					
		$V_{CC} = 2.0\text{ V}$	94	290	365	435	ns
		$V_{CC} = 4.5\text{ V}$	34	58	73	87	ns
$V_{CC} = 6.0\text{ V}$	27	47	62	74	ns		
$V_{CC} = 9.0\text{ V}$	25	45	56	68	ns		

**Table 9. Dynamic characteristics 74HC4067 ...continued**

$GND = 0\text{ V}$ ;  $t_r = t_f = 6\text{ ns}$ ;  $C_L = 50\text{ pF}$  unless specified otherwise; for test circuit see [Figure 14](#).

$V_{is}$  is the input voltage at a Yn or Z terminal, whichever is assigned as an input.

$V_{os}$  is the output voltage at a Yn or Z terminal, whichever is assigned as an output.

Symbol	Parameter	Conditions	25 °C		-40 °C to +125 °C		Unit
			Typ	Max	Max (85 °C)	Max (125 °C)	
$t_{on}$	turn-on time	$\bar{E}$ to Yn; see <a href="#">Figure 13</a> [4]					
		$V_{CC} = 2.0\text{ V}$	80	275	345	415	ns
		$V_{CC} = 4.5\text{ V}$	29	55	69	83	ns
		$V_{CC} = 5.0\text{ V}$ ; $C_L = 15\text{ pF}$	26	-	-	-	ns
		$V_{CC} = 6.0\text{ V}$	23	47	59	71	ns
		$V_{CC} = 9.0\text{ V}$	17	42	53	63	ns
		Sn to Yn					
		$V_{CC} = 2.0\text{ V}$	88	300	375	450	ns
		$V_{CC} = 4.5\text{ V}$	32	60	75	90	ns
		$V_{CC} = 5.0\text{ V}$ ; $C_L = 15\text{ pF}$	29	-	-	-	ns
		$V_{CC} = 6.0\text{ V}$	26	51	64	77	ns
		$V_{CC} = 9.0\text{ V}$	18	45	56	68	ns
		$\bar{E}$ to Z					
		$V_{CC} = 2.0\text{ V}$	85	275	345	415	ns
		$V_{CC} = 4.5\text{ V}$	31	55	69	83	ns
		$V_{CC} = 6.0\text{ V}$	25	47	59	71	ns
		$V_{CC} = 9.0\text{ V}$	18	42	53	63	ns
		Sn to Z					
		$V_{CC} = 2.0\text{ V}$	94	300	375	450	ns
		$V_{CC} = 4.5\text{ V}$	34	60	75	90	ns
$V_{CC} = 6.0\text{ V}$	27	51	64	77	ns		
$V_{CC} = 9.0\text{ V}$	19	45	56	68	ns		
$C_{PD}$	power dissipation capacitance	per switch; $V_I = GND$ to $V_{CC}$ [5]	29	-	-	-	pF

[1]  $t_{pd}$  is the same as  $t_{PHL}$  and  $t_{PLH}$ .

[2] Due to higher Z terminal capacitance (16 switches versus 1) the delay figures to the Z terminal are higher than those to the Y terminal.

[3]  $t_{on}$  is the same as  $t_{PHZ}$  and  $t_{PLZ}$ .

[4]  $t_{off}$  is the same as  $t_{PZH}$  and  $t_{PZL}$ .

[5]  $C_{PD}$  is used to determine the dynamic power dissipation ( $P_D$  in  $\mu\text{W}$ ).

$$P_D = C_{PD} \times V_{CC}^2 \times f_i + \sum\{(C_L + C_{sw}) \times V_{CC}^2 \times f_o\}$$
 where:

$f_i$  = input frequency in MHz;

$f_o$  = output frequency in MHz;

$\sum\{(C_L + C_{sw}) \times V_{CC}^2 \times f_o\}$  = sum of outputs;

$C_L$  = output load capacitance in pF;

$C_{sw}$  = switch capacitance in pF;

$V_{CC}$  = supply voltage in V.

**Table 10. Dynamic characteristics 74HCT4067**

$GND = 0\text{ V}$ ;  $t_r = t_f = 6\text{ ns}$ ;  $C_L = 50\text{ pF}$  unless specified otherwise; for test circuit see [Figure 14](#).

$V_{is}$  is the input voltage at a Yn or Z terminal, whichever is assigned as an input.

$V_{os}$  is the output voltage at a Yn or Z terminal, whichever is assigned as an output.

Symbol	Parameter	Conditions	25 °C		-40 °C to +125 °C		Unit
			Typ	Max	Max (85 °C)	Max (125 °C)	
$t_{pd}$	propagation delay	Yn to Z; see <a href="#">Figure 12</a> <a href="#">[1][2]</a>					
		$V_{CC} = 4.5\text{ V}$	9	15	19	22	ns
		Z to Yn					
		$V_{CC} = 4.5\text{ V}$	6	12	15	18	ns
$t_{off}$	turn-off time	$\bar{E}$ to Yn; see <a href="#">Figure 13</a> <a href="#">[3]</a>					
		$V_{CC} = 4.5\text{ V}$	26	55	69	83	ns
		$V_{CC} = 5.0\text{ V}$ ; $C_L = 15\text{ pF}$	26	-	-	-	ns
		Sn to Yn					
		$V_{CC} = 4.5\text{ V}$	31	55	69	83	ns
		$V_{CC} = 5.0\text{ V}$ ; $C_L = 15\text{ pF}$	30	-	-	-	ns
		$\bar{E}$ to Z					
		$V_{CC} = 4.5\text{ V}$	30	60	75	90	ns
		Sn to Z					
		$V_{CC} = 4.5\text{ V}$	35	60	75	90	ns
$t_{on}$	turn-on time	$\bar{E}$ to Yn; see <a href="#">Figure 13</a> <a href="#">[4]</a>					
		$V_{CC} = 4.5\text{ V}$	32	60	75	90	ns
		$V_{CC} = 5.0\text{ V}$ ; $C_L = 15\text{ pF}$	32	-	-	-	ns
		Sn to Yn					
		$V_{CC} = 4.5\text{ V}$	35	60	75	90	ns
		$V_{CC} = 5.0\text{ V}$ ; $C_L = 15\text{ pF}$	33	-	-	-	ns
		$\bar{E}$ to Z					
		$V_{CC} = 4.5\text{ V}$	38	65	81	98	ns
		Sn to Z					
		$V_{CC} = 4.5\text{ V}$	38	65	81	98	ns
$C_{PD}$	power dissipation capacitance	per switch; $V_I = GND$ to $(V_{CC} - 1.5\text{ V})$ <a href="#">[5]</a>	29	-	-	-	pF

[1]  $t_{pd}$  is the same as  $t_{PHL}$  and  $t_{PLH}$ .

[2] Due to higher Z terminal capacitance (16 switches versus 1) the delay figures to the Z terminal are higher than those to the Y terminal.

[3]  $t_{on}$  is the same as  $t_{PHZ}$  and  $t_{PLZ}$ .

[4]  $t_{off}$  is the same as  $t_{PZH}$  and  $t_{PZL}$ .

[5]  $C_{PD}$  is used to determine the dynamic power dissipation ( $P_D$  in  $\mu\text{W}$ ).

$$P_D = C_{PD} \times V_{CC}^2 \times f_i + \sum\{(C_L + C_{sw}) \times V_{CC}^2 \times f_o\}$$

where:

$f_i$  = input frequency in MHz;

$f_o$  = output frequency in MHz;

$\sum\{(C_L + C_{sw}) \times V_{CC}^2 \times f_o\}$  = sum of outputs;

$C_L$  = output load capacitance in pF;

$C_{sw}$  = switch capacitance in pF;

$V_{CC}$  = supply voltage in V.

12. Waveforms

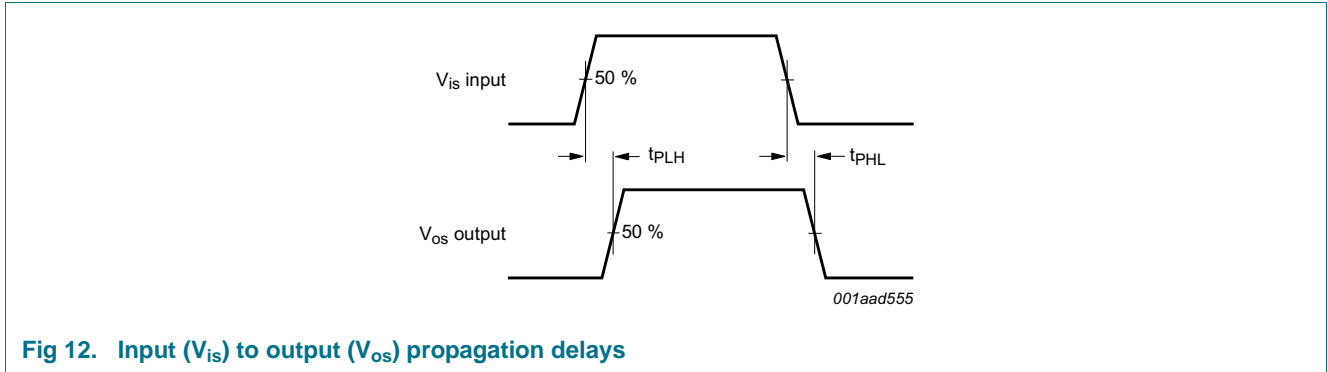
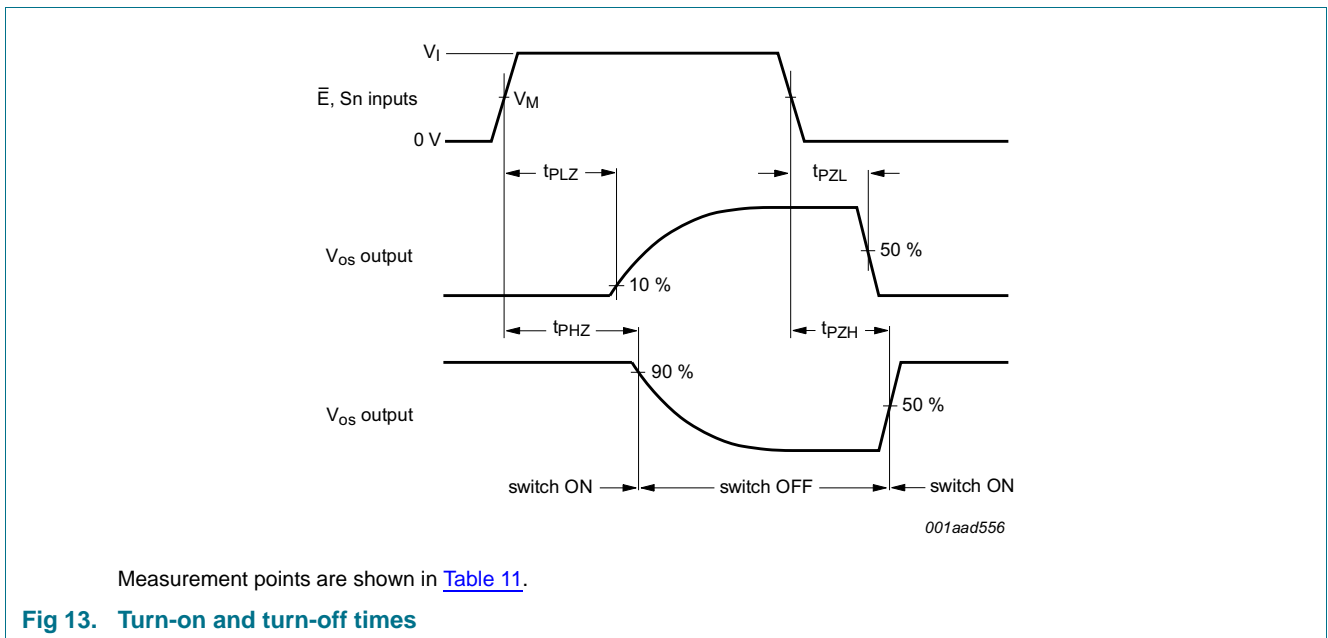


Fig 12. Input ( $V_{is}$ ) to output ( $V_{os}$ ) propagation delays



Measurement points are shown in [Table 11](#).

Fig 13. Turn-on and turn-off times

Table 11. Measurement points

Type	$V_I$	$V_M$
74HC4067	$V_{CC}$	$0.5V_{CC}$
74HCT4067	3.0 V	1.3 V



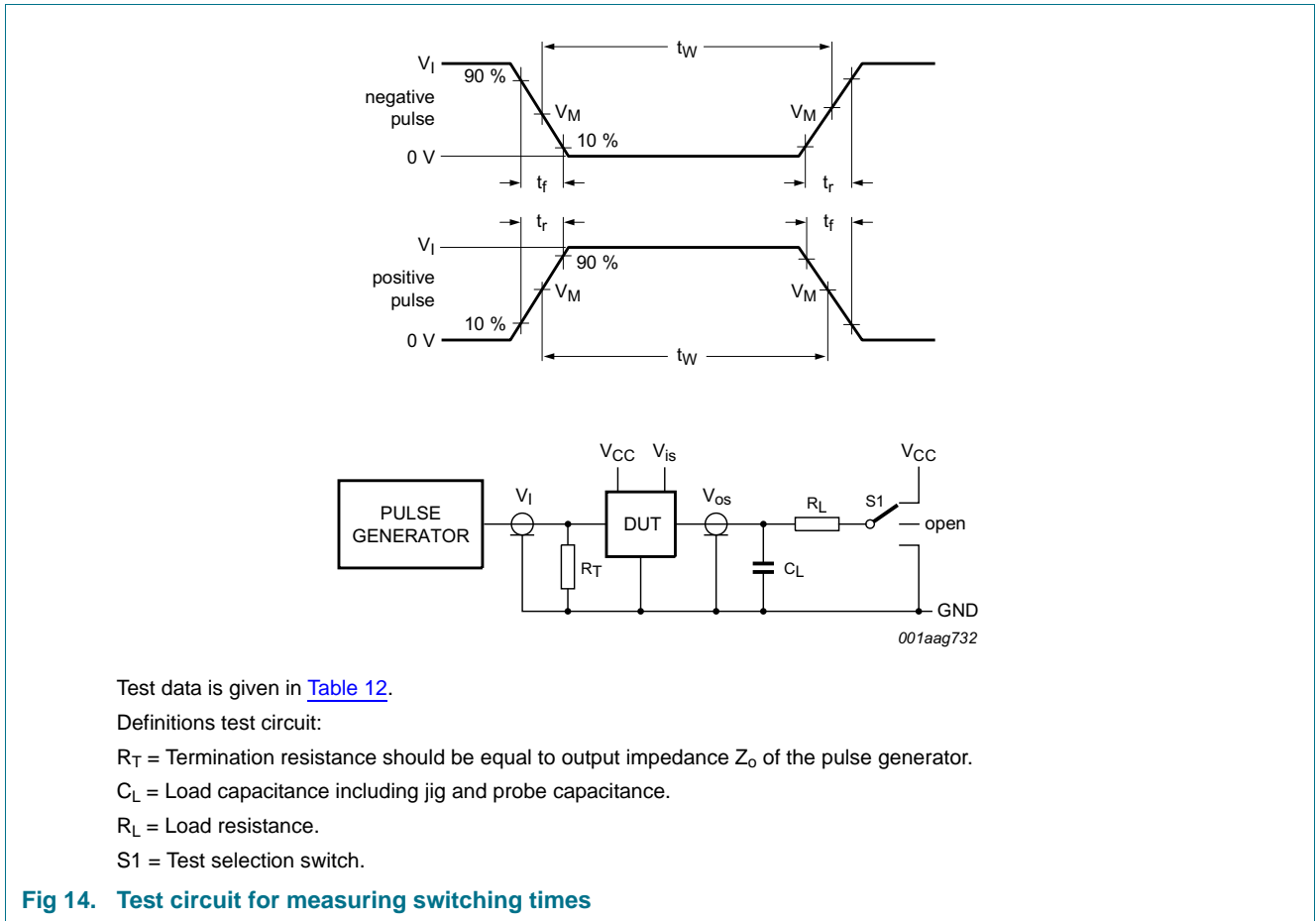


Table 12. Test data

Test	Input				Output		S1 position
	Control $\bar{E}$	Address Sn	Switch Yn (Z)	$t_r, t_f$	Switch Z (Yn)		
	$V_I$ [1]	$V_I$ [1]	$V_{is}$		$C_L$	$R_L$	
$t_{PHL}, t_{PLH}$	GND	GND or $V_{CC}$	GND to $V_{CC}$	6 ns	50 pF	-	open
$t_{PHZ}, t_{PZH}$	GND to $V_{CC}$	GND to $V_{CC}$	$V_{CC}$	6 ns	50 pF, 15 pF	1 k $\Omega$	GND
$t_{PLZ}, t_{PZL}$	GND to $V_{CC}$	GND to $V_{CC}$	GND	6 ns	50 pF, 15 pF	1 k $\Omega$	$V_{CC}$

[1] For 74HCT4067: maximum input voltage  $V_I = 3.0$  V.

### 13. Additional dynamic characteristics

**Table 13. Additional dynamic characteristics**

Recommended conditions and typical values;  $GND = 0\text{ V}$ ;  $T_{amb} = 25\text{ }^\circ\text{C}$ .

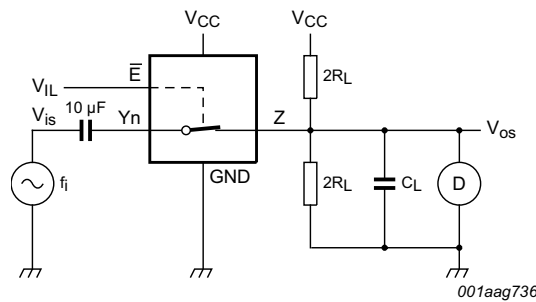
$V_{is}$  is the input voltage at a  $Y_n$  or  $Z$  terminal, whichever is assigned as an input.

$V_{os}$  is the output voltage at a  $Y_n$  or  $Z$  terminal, whichever is assigned as an output.

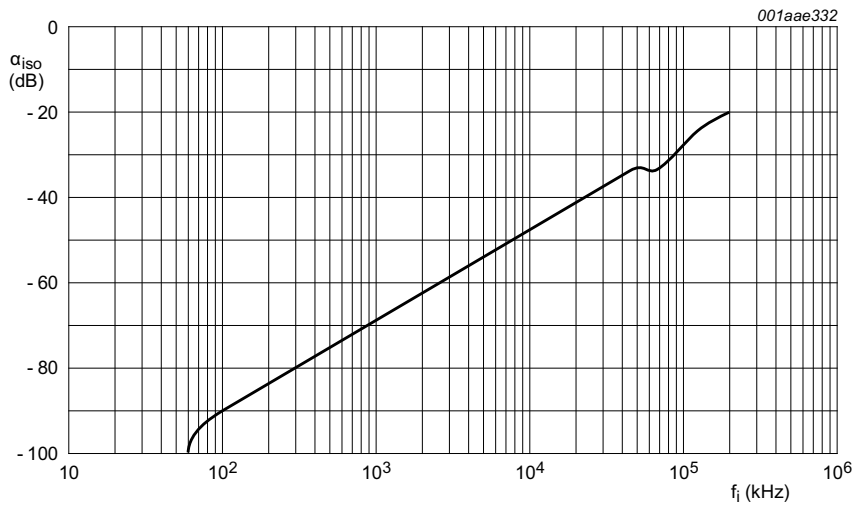
Symbol	Parameter	Conditions	Min	Typ	Max	Unit
THD	total harmonic distortion	$R_L = 10\text{ k}\Omega$ ; $C_L = 50\text{ pF}$ ; see <a href="#">Figure 15</a>				
		$f_i = 1\text{ kHz}$				
		$V_{CC} = 4.5\text{ V}$ ; $V_{is(p-p)} = 4.0\text{ V}$	-	0.04	-	%
		$V_{CC} = 9.0\text{ V}$ ; $V_{is(p-p)} = 8.0\text{ V}$	-	0.02	-	%
		$f_i = 10\text{ kHz}$				
		$V_{CC} = 4.5\text{ V}$ ; $V_{is(p-p)} = 4.0\text{ V}$	-	0.12	-	%
$\alpha_{iso}$	isolation (OFF-state)	$R_L = 600\text{ }\Omega$ ; $C_L = 50\text{ pF}$ ; see <a href="#">Figure 16</a> [1]				
		$V_{CC} = 4.5\text{ V}$	-	-50	-	dB
		$V_{CC} = 9.0\text{ V}$	-	-50	-	dB
$f_{(-3dB)}$	-3 dB frequency response	$R_L = 50\text{ }\Omega$ ; $C_L = 10\text{ pF}$ ; see <a href="#">Figure 17</a> [2]				
		$V_{CC} = 4.5\text{ V}$	-	90	-	MHz
		$V_{CC} = 9.0\text{ V}$	-	100	-	MHz
$C_{sw}$	switch capacitance	independent pins Y	-	5	-	pF
		common pin Z	-	45	-	pF

[1] Adjust input voltage  $V_{is}$  to 0 dBm level (0 dBm = 1 mW into 600  $\Omega$ ).

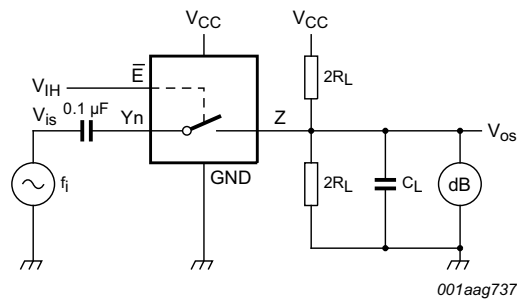
[2] Adjust input voltage  $V_{is}$  to 0 dBm level at  $V_{os}$  for  $f_i = 1\text{ MHz}$  (0 dBm = 1 mW into 50  $\Omega$ ). After set-up,  $f_i$  is increased to obtain a reading of -3 dB at  $V_{os}$ .



**Fig 15. Test circuit for measuring total harmonic distortion**



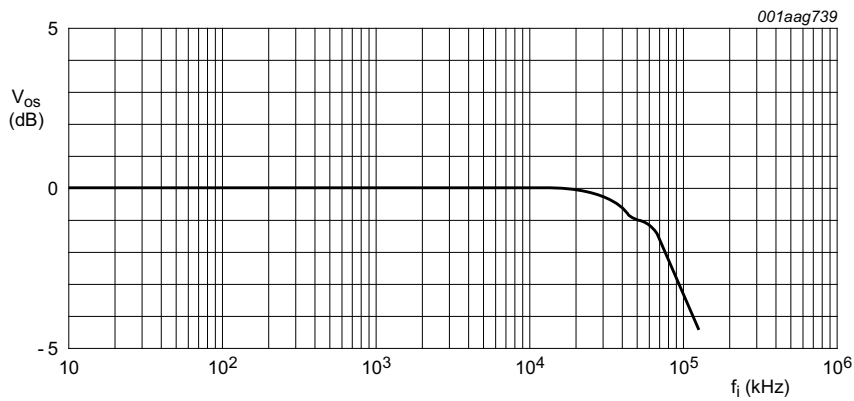
a. Isolation (OFF-state)



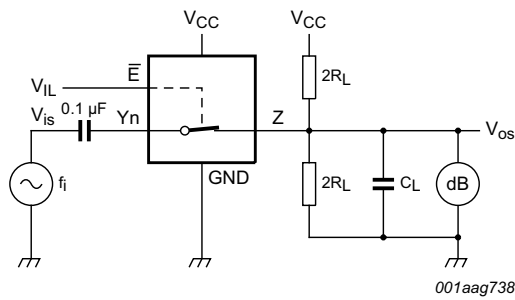
b. Test circuit

$V_{CC} = 4.5\text{ V}$ ;  $GND = 0\text{ V}$ ;  $R_L = 600\ \Omega$ ;  $R_{source} = 1\text{ k}\Omega$ .

**Fig 16. Isolation (OFF-state) as a function of frequency**



a. Typical -3 dB frequency response



b. Test circuit

$V_{CC} = 4.5\text{ V}$ ;  $GND = 0\text{ V}$ ;  $R_L = 50\ \Omega$ ;  $R_{source} = 1\text{ k}\Omega$ .

**Fig 17. -3 dB frequency response**

14. Package outline

SO24: plastic small outline package; 24 leads; body width 7.5 mm

SOT137-1

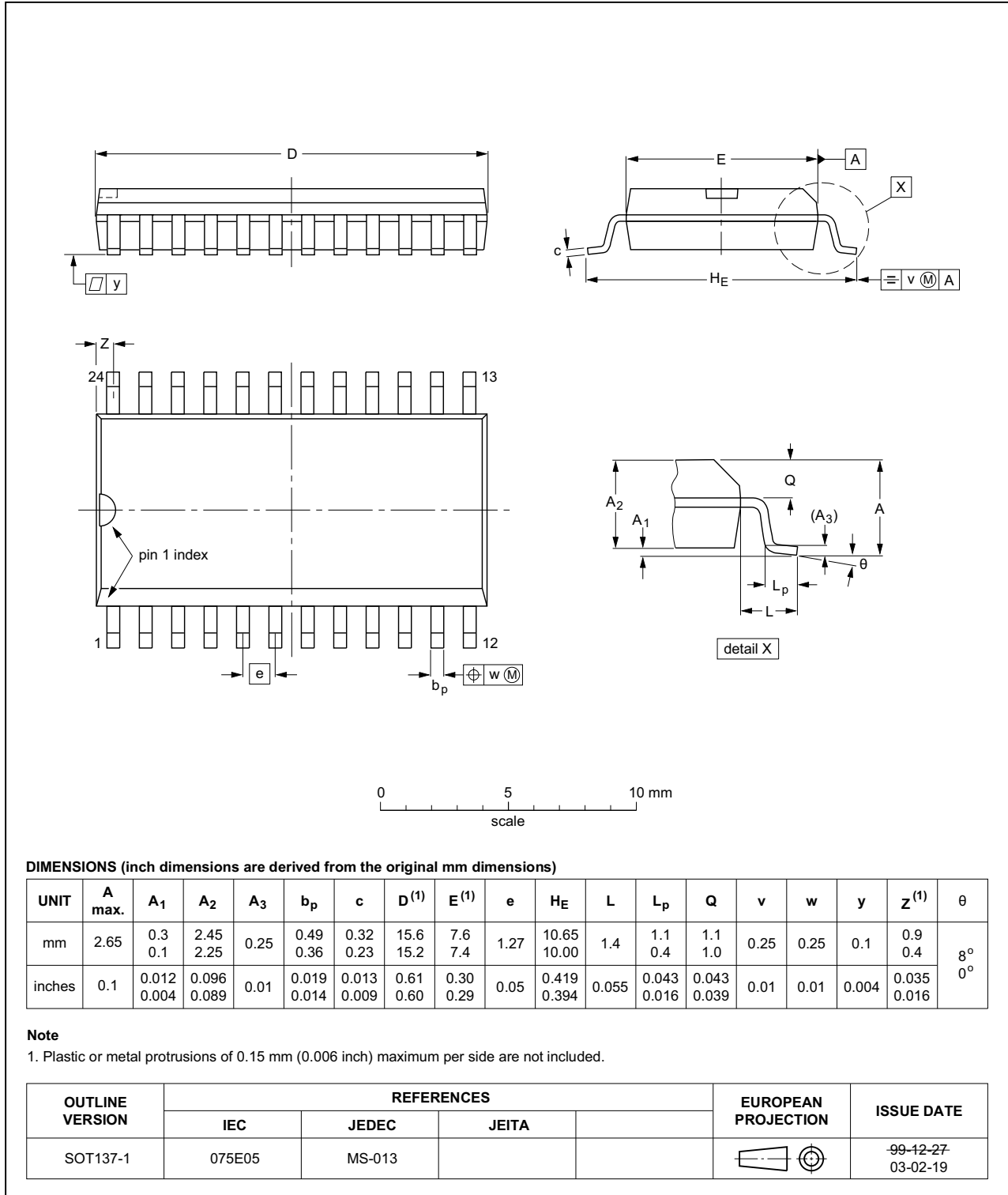


Fig 18. Package outline SOT137-1 (SO24)

SSOP24: plastic shrink small outline package; 24 leads; body width 5.3 mm

SOT340-1

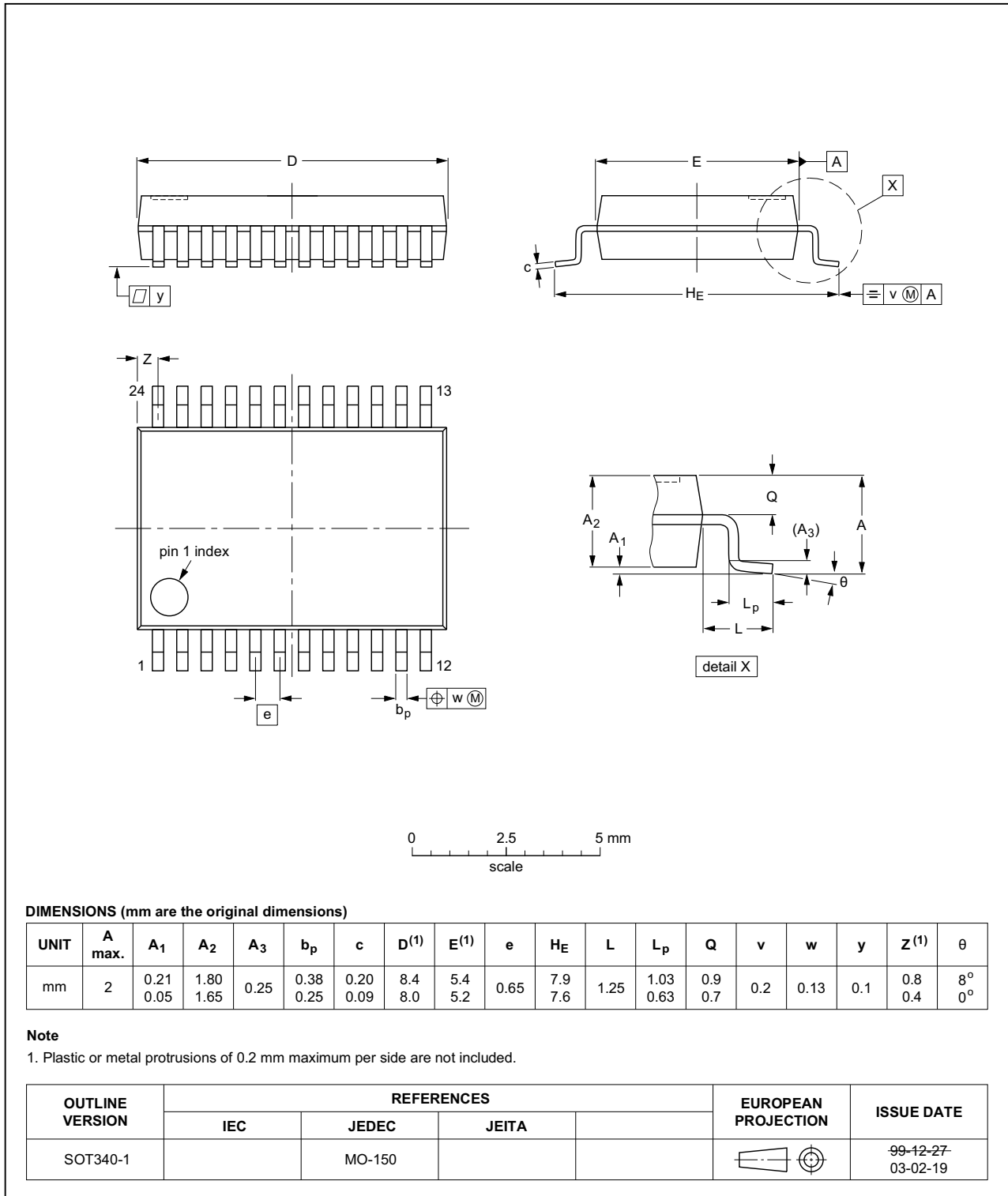


Fig 19. Package outline SOT340-1 (SSOP24)

TSSOP24: plastic thin shrink small outline package; 24 leads; body width 4.4 mm

SOT355-1

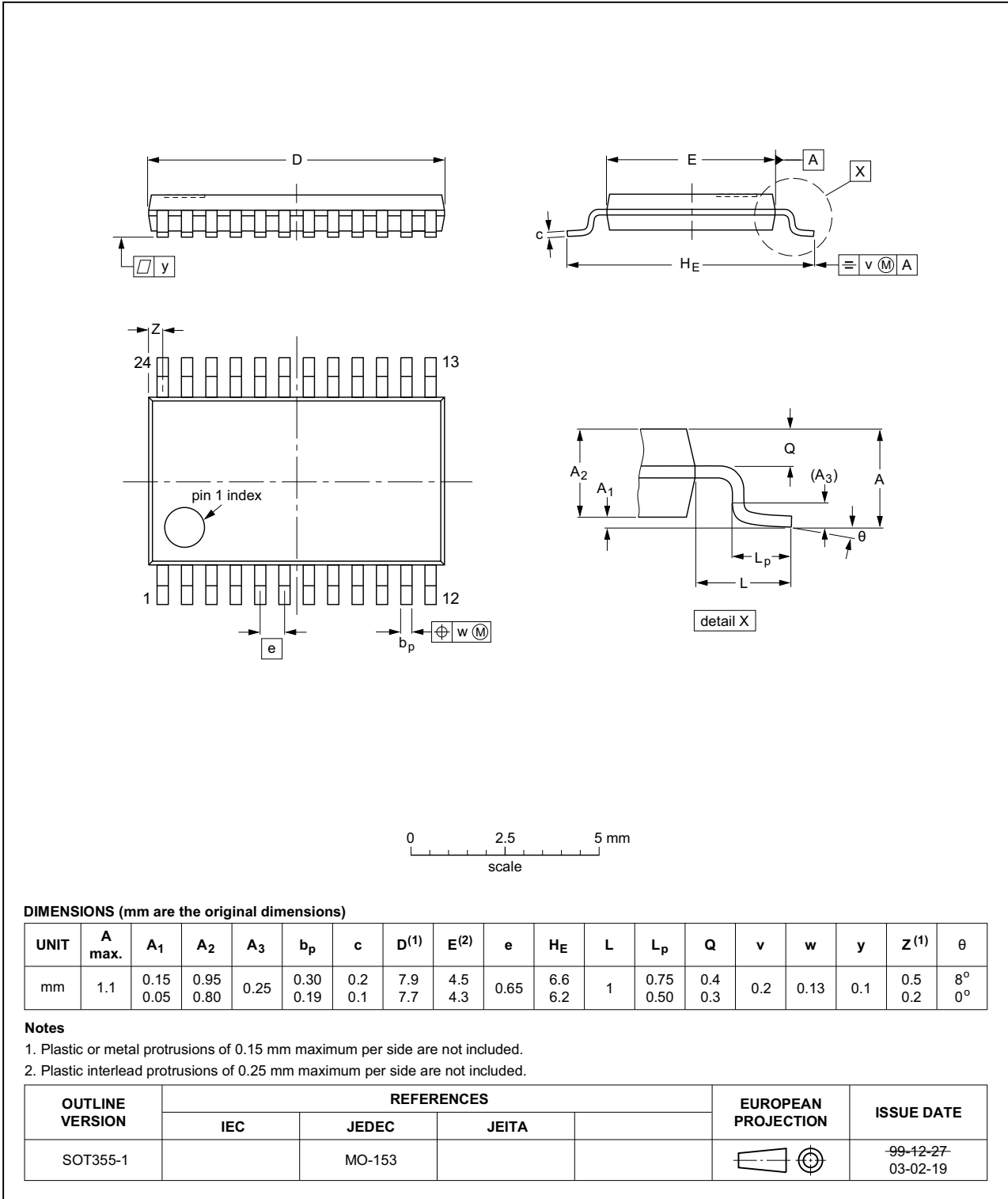


Fig 20. Package outline SOT355-1 (TSSOP24)

DHVQFN24: plastic dual in-line compatible thermal enhanced very thin quad flat package; no leads; 24 terminals; body 3.5 x 5.5 x 0.85 mm

SOT815-1

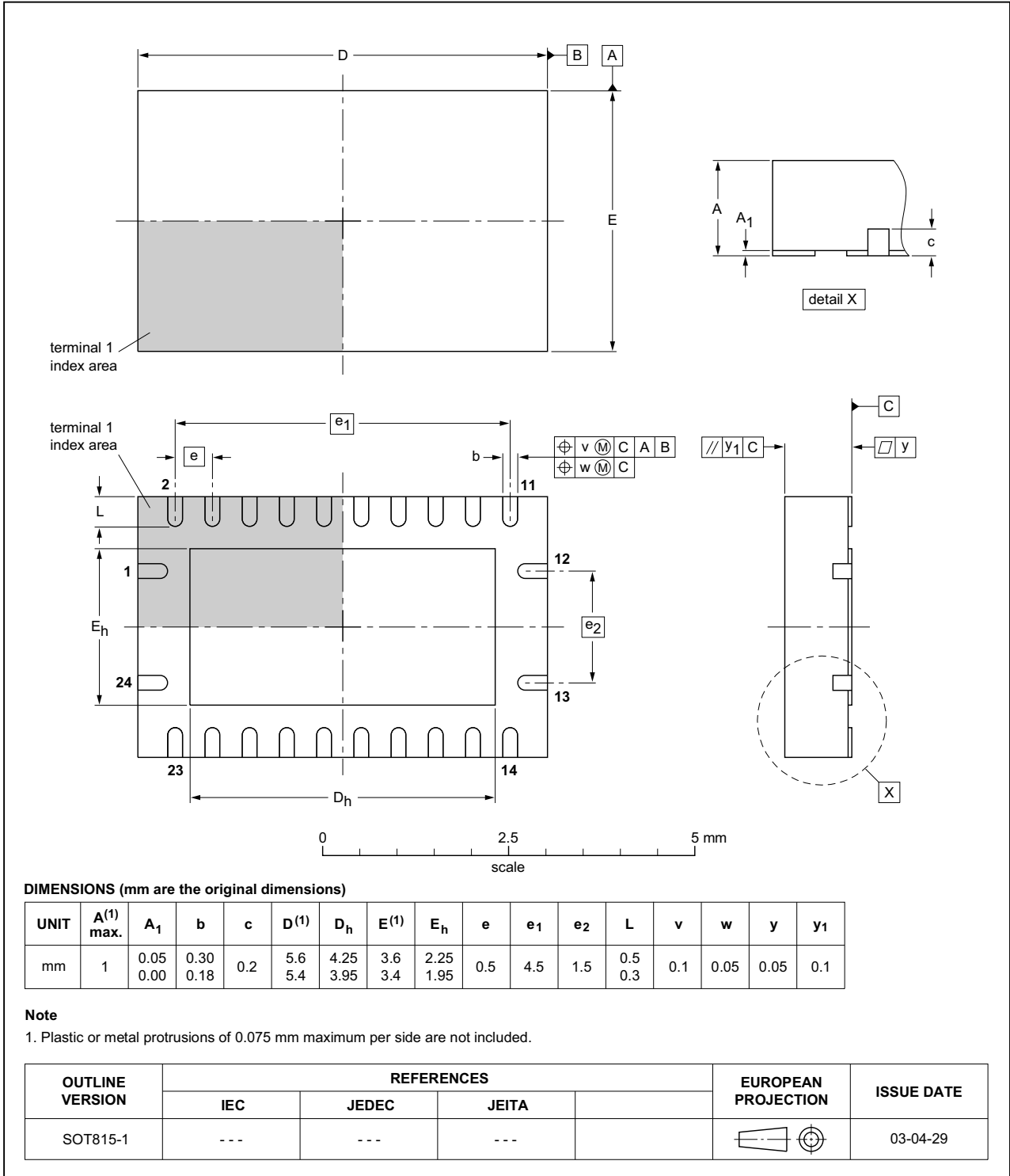


Fig 21. Package outline SOT815-1 (DHVQFN24)



## 15. Revision history

Table 14. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
74HC_HCT4067 v.6	20150522	Product data sheet	-	74HC_HCT4067 v.5
Modifications:	<ul style="list-style-type: none"> <li>Type numbers 74HC4067N and 74HCT4067N (SOT101-1) removed.</li> <li><a href="#">Figure 8</a>, <a href="#">Figure 9</a>: Figure note <math>V_{is} = 0\text{ V}</math> to (<math>V_{CC}-GND</math>) changed to <math>V_{is} = 0\text{ V}</math> to <math>V_{CC}</math>.</li> </ul>			
74HC_HCT4067 v.5	20111213	Product data sheet	-	74HC_HCT4067 v.4
Modifications:	<ul style="list-style-type: none"> <li>Legal pages updated.</li> </ul>			
74HC_HCT4067 v.4	20110518	Product data sheet	-	74HC_HCT4067 v.3
74HC_HCT4067 v.3	20071015	Product data sheet	-	74HC_HCT4067_CNV v.2
74HC_HCT4067_CNV v.2	19970901	Product specification	-	-

## 16. Legal information

### 16.1 Data sheet status

Document status <sup>[1][2]</sup>	Product status <sup>[3]</sup>	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term 'short data sheet' is explained in section "Definitions".

[3] The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices. The latest product status information is available on the Internet at URL <http://www.nxp.com>.

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## 18. Contents

<b>1</b>	<b>General description</b> .....	<b>1</b>
<b>2</b>	<b>Features and benefits</b> .....	<b>1</b>
<b>3</b>	<b>Applications</b> .....	<b>1</b>
<b>4</b>	<b>Ordering information</b> .....	<b>2</b>
<b>5</b>	<b>Functional diagram</b> .....	<b>2</b>
<b>6</b>	<b>Pinning information</b> .....	<b>5</b>
6.1	Pinning .....	5
6.2	Pin description .....	5
<b>7</b>	<b>Functional description</b> .....	<b>6</b>
<b>8</b>	<b>Limiting values</b> .....	<b>6</b>
<b>9</b>	<b>Recommended operating conditions</b> .....	<b>7</b>
<b>10</b>	<b>Static characteristics</b> .....	<b>8</b>
<b>11</b>	<b>Dynamic characteristics</b> .....	<b>13</b>
<b>12</b>	<b>Waveforms</b> .....	<b>16</b>
<b>13</b>	<b>Additional dynamic characteristics</b> .....	<b>18</b>
<b>14</b>	<b>Package outline</b> .....	<b>21</b>
<b>15</b>	<b>Revision history</b> .....	<b>25</b>
<b>16</b>	<b>Legal information</b> .....	<b>26</b>
16.1	Data sheet status .....	26
16.2	Definitions .....	26
16.3	Disclaimers .....	26
16.4	Trademarks .....	27
<b>17</b>	<b>Contact information</b> .....	<b>27</b>
<b>18</b>	<b>Contents</b> .....	<b>28</b>

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