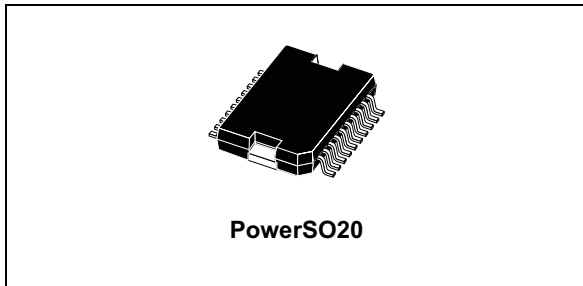


Three-phase motor driver

Datasheet - production data



Features

- Supply voltage from 7 to 52 V
- 5 A peak current
- R_{DSon} 0.3 Ω typ. value at 25 °C
- Cross conduction protection
- TTL compatible driver
- Operating frequency up to 150 kHz
- Thermal shutdown
- Intrinsic fast free wheeling diodes
- Input and enable function for each half bridge
- 10 V external reference available

Description

The L6234 is a triple half bridge to drive a brushless DC motor.

It is realized in BCDmultipower technology which combines isolated DMOS power transistors with CMOS and bipolar circuits on the same chip.

By using mixed technology it has been possible to optimize the logic circuitry and the power stage to achieve the best possible performance.

The output DMOS transistors can sustain a very high current due to the fact that the DMOS structure is not affected by the second breakdown effect, the RMS maximum current is practically limited by the dissipation capability of the package.

All the logic inputs are TTL, CMOS and μP compatible. Each channel is controlled by two separate logic inputs.

The L6234 device is available in a 20-pin PowerSO20 package.

Table 1. Device summary

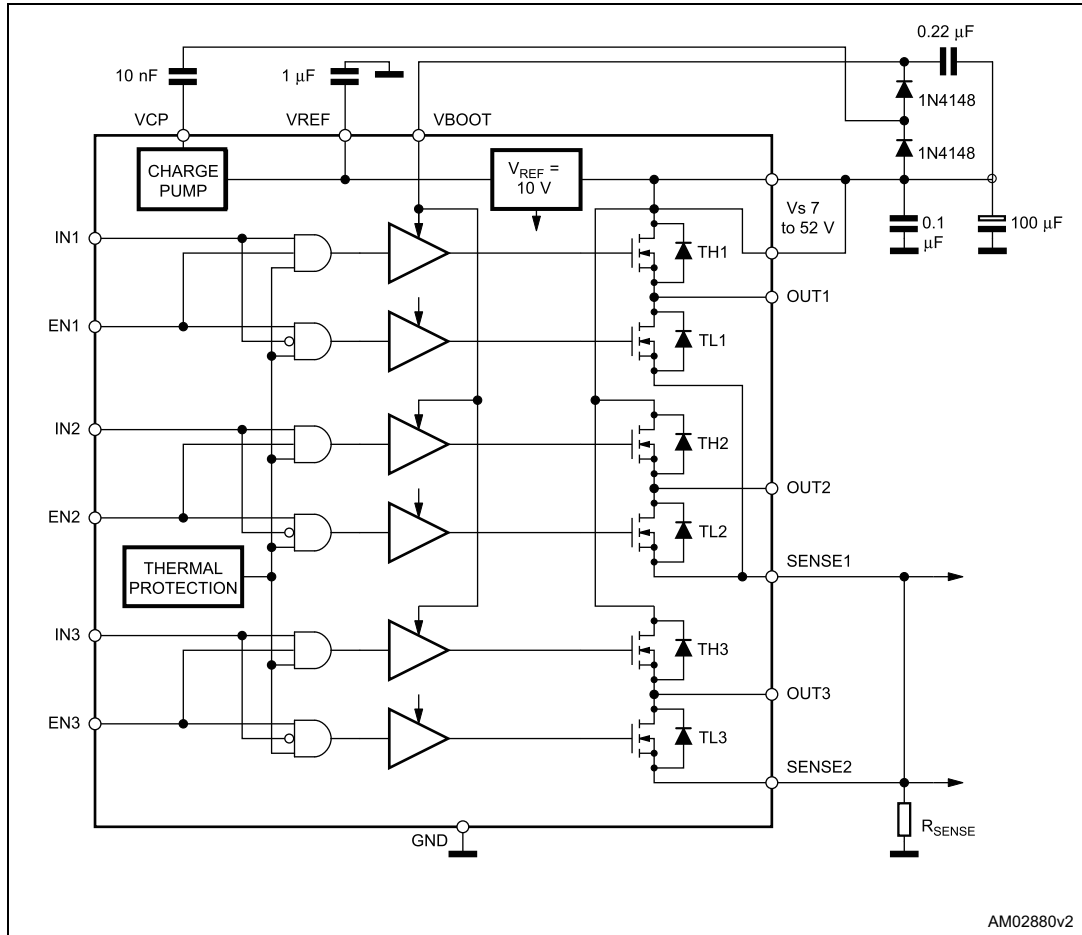
| Order code | Package | Packing |
|--------------|-----------|---------------|
| L6234PD | PowerSO20 | Tube |
| L6234PD013TR | PowerSO20 | Tape and reel |

Contents

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1 Block diagram

Figure 1. Block diagram



2 Pin connections

Figure 2. Pin connections

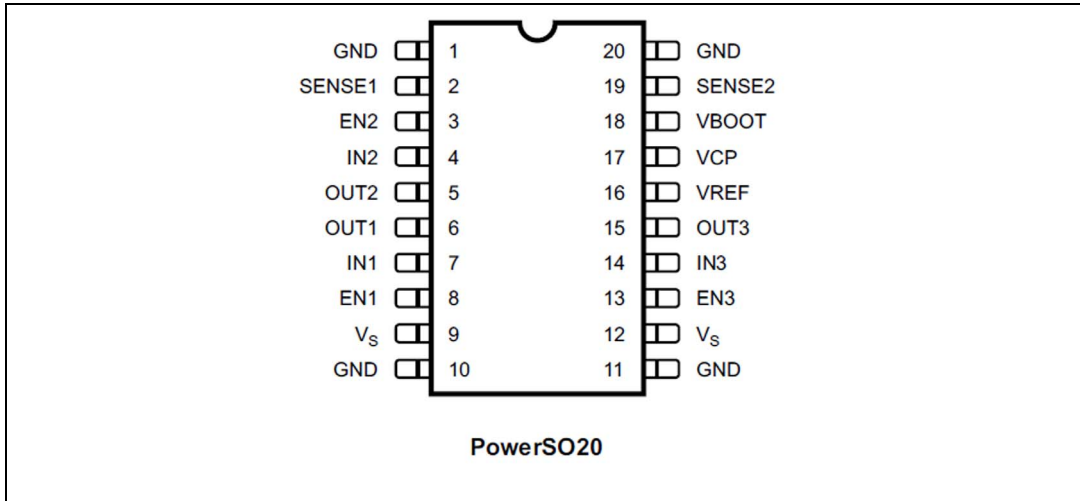


Table 2. Pin functions

| Pin no. | Name | Function |
|-----------------|-------------------------|---|
| 1, 10 11, 20 | GND | Common ground terminal. In the PowerSO package these pins are used to dissipate the heat forward the PCB. |
| 2 | SENSE1 | A sense resistor connected to this pin provides feedback for motor current control for the bridges 1 and 2. |
| 3 8 13 | EN 2 EN 1 EN 3 | Enable of the channels 1/2/3. A logic LOW level on this pin switches off both power DMOS of the related channel. |
| 4 7 14 | IN 2 IN 1 IN 3 | Logic input of channels 1/2/3. A logic HIGH level (when the corresponding EN pin is HIGH) switches ON the upper DMOS power transistor, while a logic LOW switches ON the corresponding low side power DMOS. |
| 5 6 15 | OUT 2 OUT 1 OUT 3 | Output of the channels 1/2/3. |
| 9, 12 | V _s | Power supply voltage. |
| 16 | VREF | Internal voltage reference. A capacitor connected from this pin to GND increases the stability of the power DMOS drive circuit. |
| 17 | VCP | Bootstrap oscillator. Oscillator output for the external charge pump. |
| 18 | VBOOT | Overvoltage input to drive the upper DMOS |
| 19 | SENSE2 | A sense resistor connected to this pin provides feedback for motor current control for the bridge 3. |

3 Thermal data

Table 3. Thermal data

| Symbol | Parameter | PowerSO20 | Unit |
|------------------|----------------------------------|-----------|------|
| $R_{th\ j-case}$ | Thermal resistance junction case | 1.5 | °C/W |

4 Maximum ratings

Table 4. Absolute maximum ratings

| Symbol | Parameter | Value | Unit |
|------------------|---|------------|------|
| V_S | Power supply voltage | 52 | V |
| V_{IN}, V_{EN} | Input enable voltage | - 0.3 to 7 | V |
| I_{peak} | Pulsed output current ⁽¹⁾ | 5 | A |
| V_{SENSE} | Sensing voltage (DC voltage) | -1 to 4 | V |
| V_{boot} | Bootstrap peak voltage | 62 | V |
| V_{OD} | Differential output voltage (between any of the 3 OUT pins) | 60 | V |
| f_C | Commutation frequency | 150 | kHz |
| V_{REF} | Reference voltage | 12 | V |
| P_{tot} | Total power dissipation ($T_A = 70\text{ °C}$) | 2.3 | W |
| T_{stg}, T_j | Storage and junction temperature range | -40 to 150 | °C |

1. Pulse width limited only by junction temperature and the transient thermal impedance.

Recommended operating conditions

Table 5. Recommended operating conditions

| Symbol | Parameter | Value | Unit |
|-------------|---|------------|------|
| V_S | Supply voltage | 7 to 42 | V |
| V_{OD} | Peak to peak differential voltage (between any of the 3 out pins) | 52 | V |
| I_{out} | DC output current ($T_A = 25\text{ °C}$) | 4 | A |
| V_{SENSE} | Sensing voltage (pulsed $t_w < 300\text{ nsec}$) | -4 to 4 | V |
| | Sensing voltage (DC) | -1 to 1 | V |
| T_j | Junction temperature range | -40 to 125 | °C |

5 Electrical characteristics

$V_S = 42\text{ V}$; $T_j = 25\text{ °C}$ unless otherwise specified.

Table 6. Electrical characteristics

| Symbol | Parameter | Test condition | Min. | Typ. | Max. | Unit |
|-------------------------------|--------------------------|----------------------------------|------|------|------|---------------|
| V_S | Supply voltage | - | 7 | - | 52 | V |
| V_{ref} | Reference voltage | - | - | 10 | - | V |
| I_S | Quiescent supply current | - | - | 6.5 | - | mA |
| T_S | Thermal shutdown | - | 150 | - | - | °C |
| T_D | Dead time protection | - | - | 300 | - | ns |
| Output DMOS transistor | | | | | | |
| I_{DSS} | Leakage current | - | - | - | 1 | mA |
| R_{DSon} | ON resistance | - | - | 0.3 | - | Ω |
| Source drain diode | | | | | | |
| V_{SD} | Forward ON voltage | $I_{SD} = 4\text{ A}$; EN = LOW | - | 1.2 | - | V |
| T_{RR} | Reverse recovery time | $I_F = 4\text{ A}$ | - | 900 | - | ns |
| T_{pr} | Forward recovery time | - | - | 200 | - | ns |
| Logic levels | | | | | | |
| V_{INL}, V_{ENL} | Input LOW voltage | - | -0.3 | - | 0.8 | V |
| V_{INH}, V_{ENH} | Input HIGH voltage | - | 2 | - | 7 | V |
| I_{INL}, I_{ENL} | Input LOW current | $V_{IN}, V_{EN} = L$ | - | - | -10 | μA |
| I_{INH}, I_{ENH} | Input HIGH current | $V_{IN}, V_{EN} = H$ | - | 30 | - | μA |

6 Circuit description

The L6234 is a triple half bridge designed to drive brushless DC motors. Each half bridge has 2 power DMOS transistors with $R_{DSon} = 0.3 \Omega$.

The 3 half bridges can be controlled independently by means of the 3 inputs IN1, IN2, IN3 and the 3 inputs EN1, EN2, and EN3. An external connection to the 3 common low side DMOS sources is provided to connect a sensing resistor for the constant current chopping application.

The driving stage and the logic stage are designed to work from 7 V to 52 V.

7 Typical characteristics

Figure 3. Quiescent current vs. supply voltage

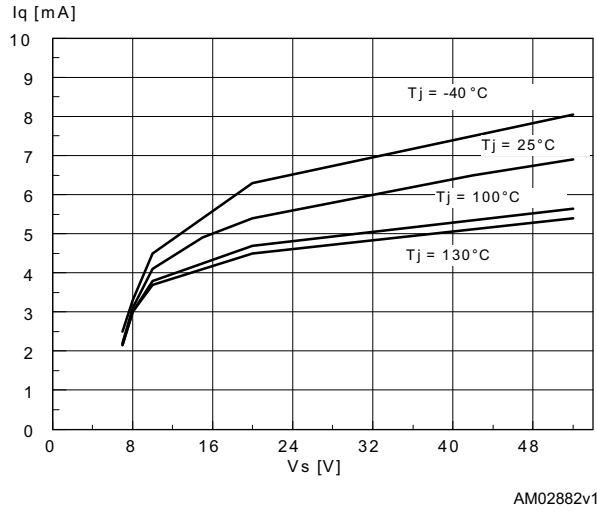


Figure 4. Normalized quiescent current vs. switching frequency

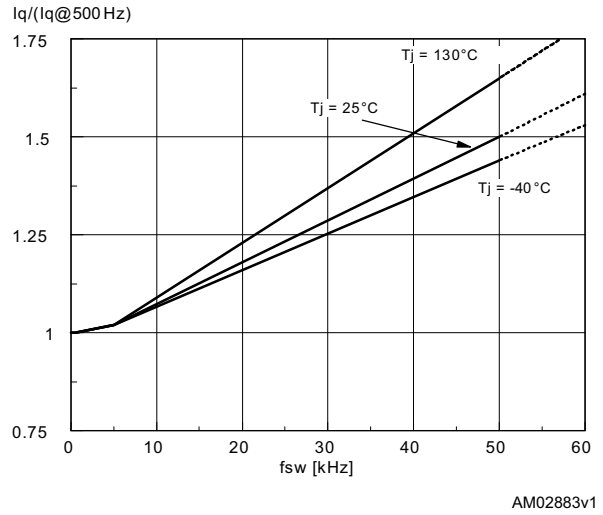


Figure 5. Typical $R_{DS(on)}$ vs. supply voltage

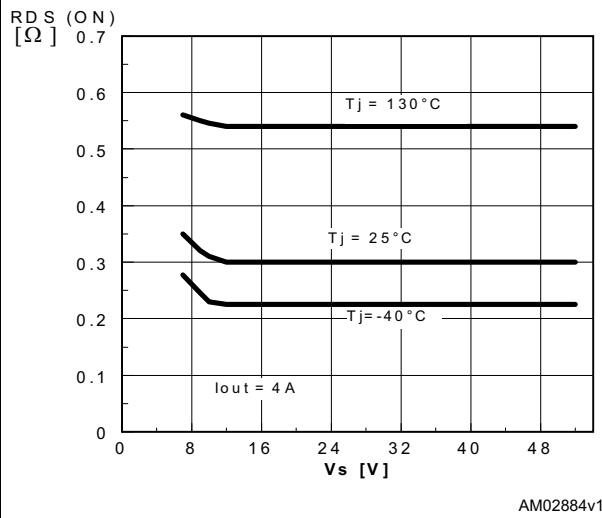
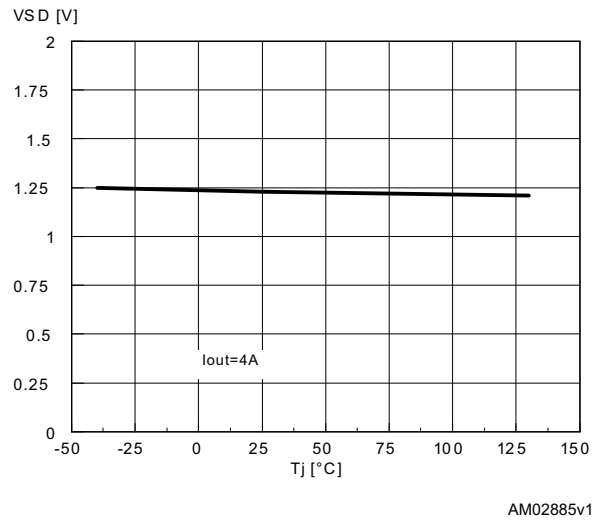


Figure 6. Source drain forward on voltage vs. junction temperature



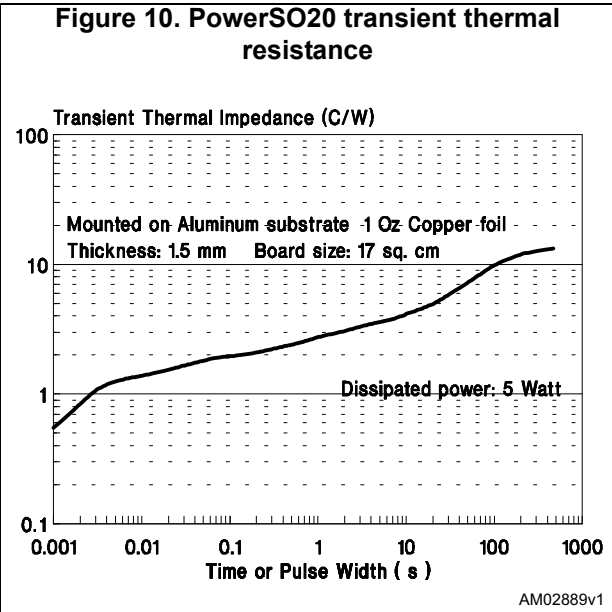
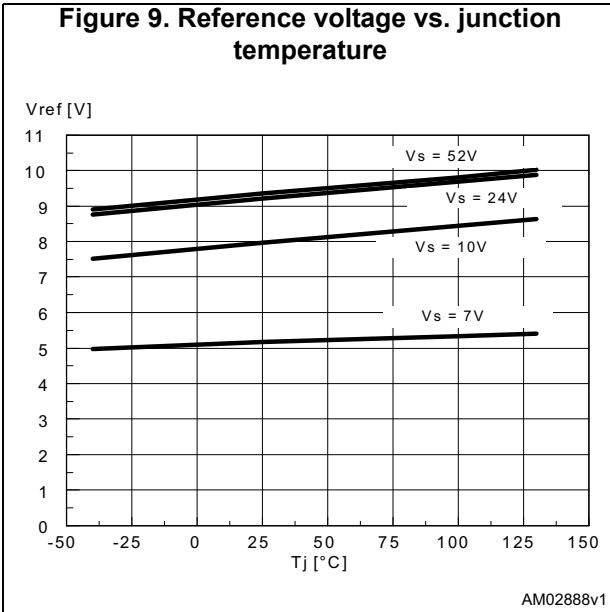
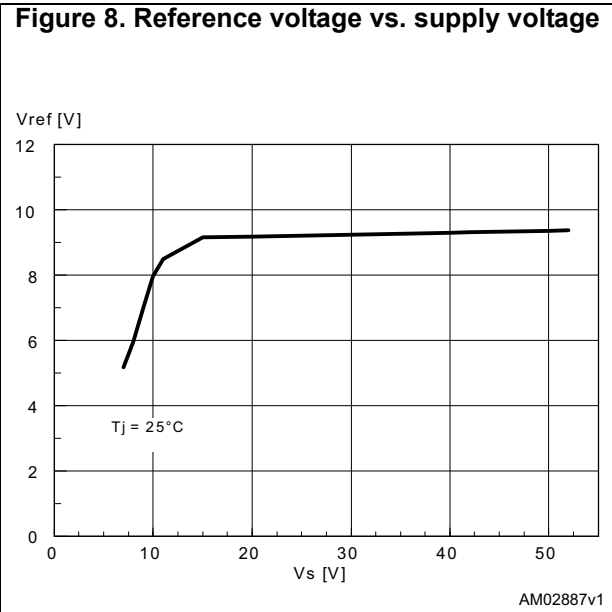
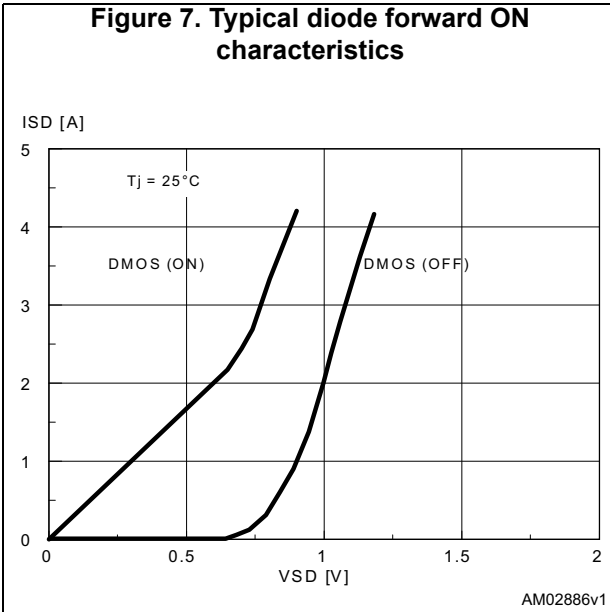


Figure 11. PowerSO20 thermal resistance (mounted on aluminium substrate)

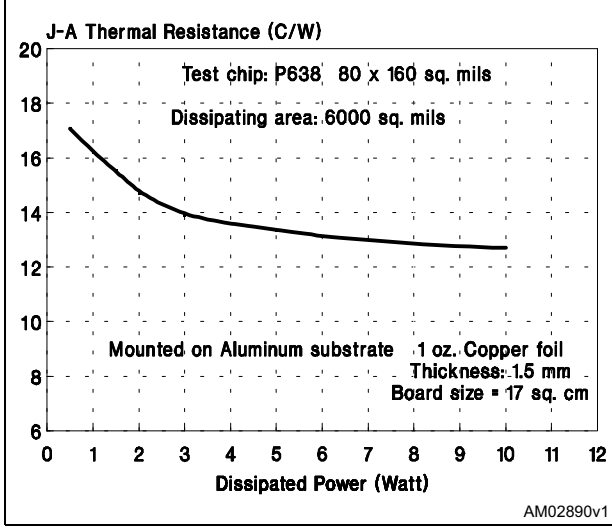


Figure 12. PowerSO20 thermal resistance (mounted on FR4 monolayer substrate)

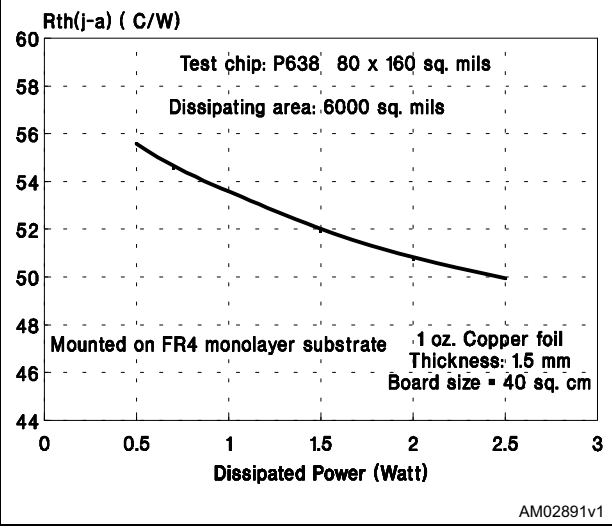


Figure 13. PowerSO20: with external heatsink

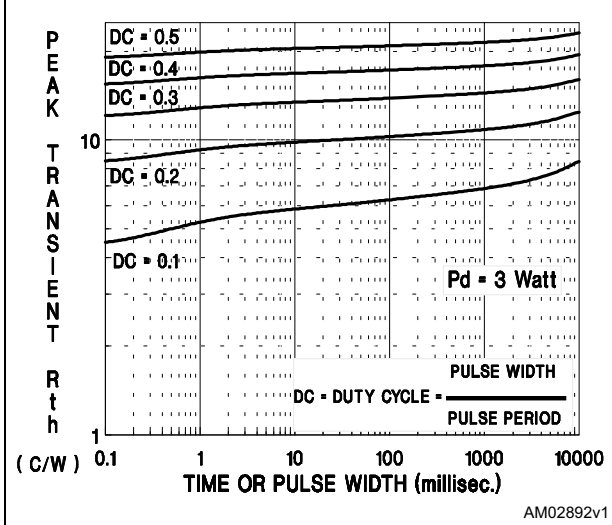
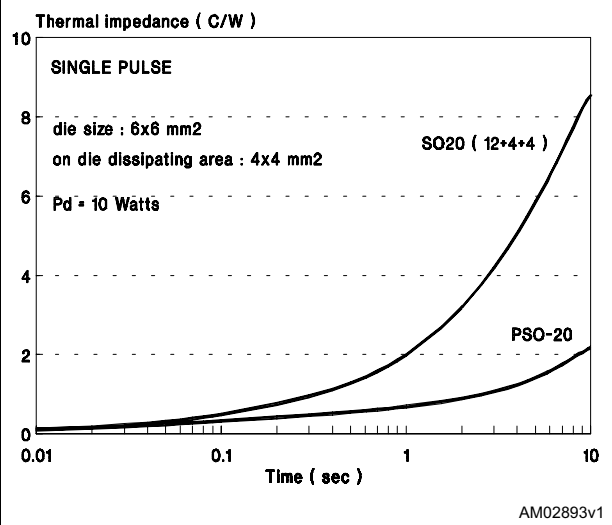


Figure 14. Thermal impedance of PowerSO20 and standard SO20



8 Package information

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK[®] packages, depending on their level of environmental compliance. ECOPACK[®] specifications, grade definitions and product status are available at: www.st.com. ECOPACK[®] is an ST trademark.

8.1 PowerSO20 package information

Figure 15. PowerSO20 package outline

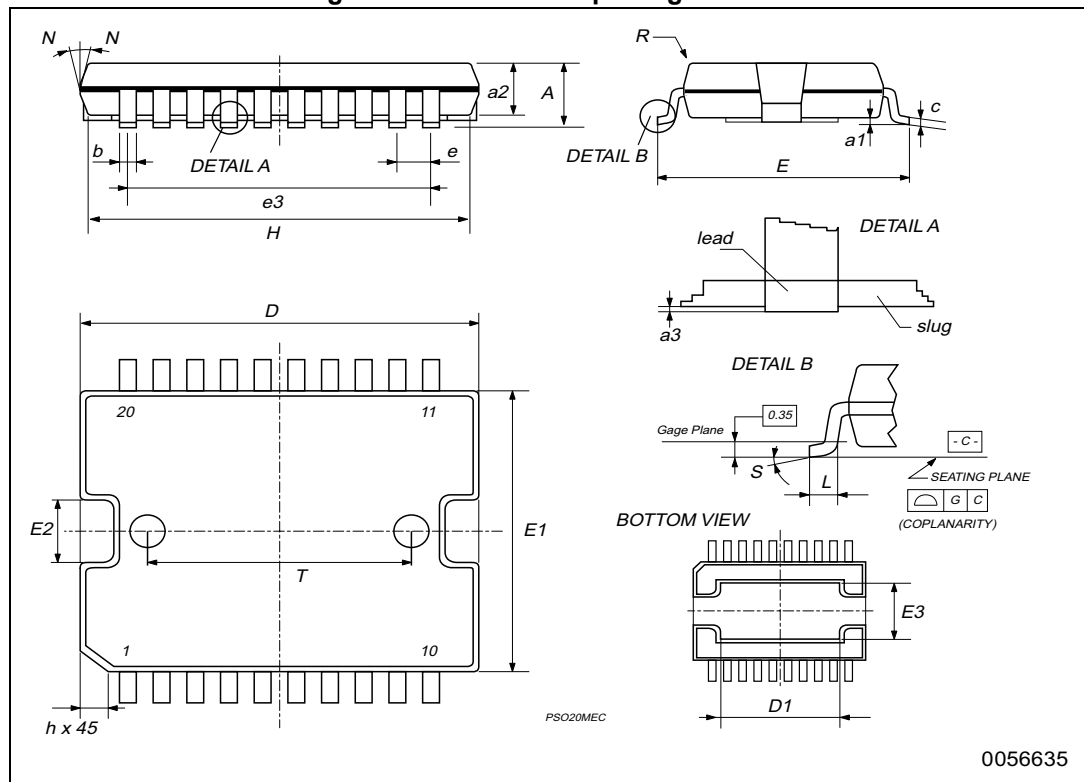


Table 7. PowerSO20 package mechanical data

| Symbol | Dimensions (mm) | | |
|-------------------|------------------|-------|------|
| | Min. | Typ. | Max. |
| A | - | - | 3.6 |
| a1 | 0.1 | - | 0.3 |
| a2 | - | - | 3.3 |
| a3 | 0 | - | 0.1 |
| b | 0.4 | - | 0.53 |
| c | 0.23 | - | 0.32 |
| D ⁽¹⁾ | 15.8 | - | 16 |
| D1 | 9.4 | - | 9.8 |
| E | 13.9 | - | 14.5 |
| e | - | 1.27 | - |
| e3 | - | 11.43 | - |
| E1 ⁽¹⁾ | 10.9 | - | 11.1 |
| E2 | - | - | 2.9 |
| E3 | 5.8 | - | 6.2 |
| G | 0 | - | 0.1 |
| H | 15.5 | - | 15.9 |
| h | - | - | 1.1 |
| L | 0.8 | - | 1.1 |
| N | 8° (typ.) | | |
| S | 8° (max.) | | |
| T | - | 10 | - |

1. "D" and "E1" do not include mold flash or protrusions.
 - Mold flash or protrusions shall not exceed 0.15 mm (0.006").

9 Revision history

Table 8. Document revision history

| Date | Revision | Changes |
|-------------|----------|---|
| 15-Nov-2011 | 10 | Updated Features in coverpage and <i>Table 4</i> . |
| 15-Mar-2017 | 11 | Removed PowerDIP 20-pin package and all references throughout document. Updated <i>Figure 1 on page 3</i> (replaced by new figure). Added note <i>1</i> . below <i>Table 7 on page 13</i> . Minor modifications throughout document. |

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