High Performance ISM Band OOK/FSK Transmitter IC

ADF7901

FEATURES

Single-chip, low power UHF transmitter
369.5 MHz to 395.9 MHz frequency operation using fractional-N PLL and fully integrated VCO
3.0 V supply voltage
Data rates up to 50 kbps supported
Low current consumption
26 mA at 12 dBm output at 384 MHz
Power-down mode (<1 µA)
24-lead TSSOP

GENERAL DESCRIPTION

The ADF7901 is a low power OOK/FSK UHF transmitter designed for use in RF remote control devices. It is capable of frequency shift keying (FSK) modulation on eight different channels, selectable by three external control lines. OOK modulation is performed by modulating the PA control line.

The on-chip VCO operates at 2× the output frequency. The division by 2 at the output of the VCO reduces the amount of PA feedthrough. As a result, OOK modulation depths of greater than 50 dB are easily achievable.

The FSK_ADJ and ASK_ADJ resistors can be adjusted in the system to optimize output power for each modulation scheme. An additional 1.5 dB of output power is provided for the lower bank of channels to adjust for antenna performance. The CE line allows the transmitter to be powered down completely. In this mode, the leakage current is typically 0.1 µA.

FUNCTIONAL BLOCK DIAGRAM

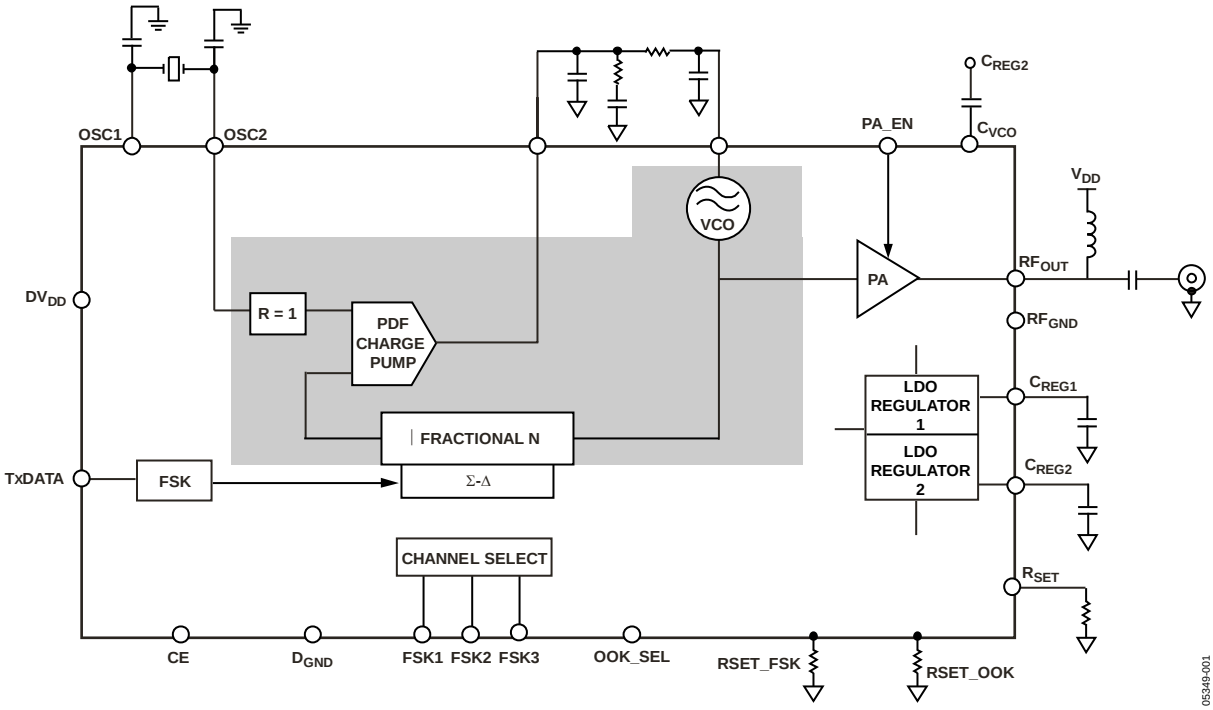

Figure 1.

Rev. A

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3/05—Revision 0: Initial Version

SPECIFICATIONS

V_{DD} =3.0 V; GND = 0 V; T_A = T_{MIN} to T_{MAX}, unless otherwise noted. Typical specifications, T_A = 25°C.[1]

Table 1.

Parameter	Min	Typ	Max	Unit	Comments/Conditions
RF CHARACTERISTICS					
Output Frequency Ranges					
Channel 1		369.5		MHz	
Channel 2		371.1		MHz	
Channel 3		375.3		MHz	
Channel 4		376.9		MHz	
Channel 5		384.0		MHz	
Channel 6		388.3		MHz	
Channel 7		391.5		MHz	
Channel 8		394.3		MHz	
Channel 9		395.9		MHz	
Phase Frequency Detector Frequency		9.8304		MHz	
TRANSMISSION PARAMETERS					
Transmit Rate					
FSK		50		kbps	
OOK		50		kbps	
Frequency Shift Keying					
FSK Separation[2]		−34.8		kHz	Data = 1
		+34.8		kHz	Data = 0
On/Off Keying					
Modulation Depth[3]		83		dB	Output power = 12 dBm
Output Power					
Min/Max Range[4]		15		dBm	
f_{OUT} ≤ 384 MHz	10	12		dBm	
f_{OUT} > 384 MHz	7	10.5		dBm	
Occupied 20 dB BW					
OOK at 1 kbps		±28	±461.9	kHz	
FSK (PA Off/On) at10 Hz[5]		±26	±461.9	kHz	
LOGIC INPUTS					
V_{INH}, Input High Voltage	2.124			V	
V_{INL}, Input Low Voltage			0.2 × V_{DD}	V	
I_{INH}/I_{INL}, Input Current			±1	µA	
C_{IN}, Input Capacitance			10	pF	
POWER SUPPLIES					
Voltage Supply					
DV_{DD}		3.0		V	
Transmit Current Consumption					
369.5 MHz to 376.9 MHz at 12 dBm		26		mA	
384 MHz at +12 dBm		26		mA	
388.3 MHz to 395.9 MHz at 10.5 dBm		21		mA	
384 MHz at 5 dBm		17		mA	
Power-Down Mode					
Low Power Sleep Mode[6]		0.2	1	µA	

Parameter	Min	Typ	Max	Unit	Comments/Conditions
PHASE-LOCKED LOOP					
VCO Gain		30		MHz/V	At 384 MHz
Spurious[3, 7]					100 kHz loop BW
Integer Boundary		−45	−23	dBc	
Reference		−70	−23	dBc	
Harmonics[3]					
Second Harmonic V_{DD} = 3.0 V		−24	−21	dBc	
Third Harmonic V_{DD} = 3.0 V		−14	−11	dBc	
All Other Harmonics			−18	dBc	
REFERENCE INPUT					
Crystal Reference		9.8304		MHz	
Crystal ESR[8]			80	Ω	
POWER AMPLIFIER					
PA Output Impedance		97 Ω + 6.4 pF			At 384 MHz
TIMING INFORMATION					
Crystal Oscillator to PLL Lock[3]		2	3	ms	
PA Enable to PA Ready–PLL Settle[9]		100	250	µs	
TEMPERATURE RANGE (T_A)	0		50	°C	

1 Operating temperature range is 0°C to 50°C.
[2] Frequency Deviation = 58 × (9.8304 MHz)/2^{14}. Error in the crystal is reflected in variation in the desired deviation.
[3] Not production tested; based on characterization.
[4] The output power can be varied in both ASK/FSK mode by altering the relevant external resistor.
[5] Measured using spectrum analyzer, 1 MHz span, 100 kHz RBW, maximum hold enabled.
[6] Maximum power-down current specification applies for the OSC2 pin grounded.
[7] Measured >461.9 kHz away from channel.
[8] Maximum recommended crystal ESR. The crystal oscillator works with crystals with higher ESR, but this results in longer power-up times.
[9] This specification refers to the time taken for the PLL to regain lock after the PA has been enabled. The PA is should only be enabled after the PLL has settled to the correct frequency.

ABSOLUTE MAXIMUM RATINGS

T_A = 25°C, unless otherwise noted.[1]

Table 2.

Parameter	Value
V_{DD} to GND[2]	−0.3 V to +4.0 V
RFVDD to GND	−0.3 V to +4.0 V
Digital I/O Voltage to GND	−0.3 V to V_{DD} + 0.3 V
Operating Temperature Range	
Industrial (B Version)	0°C to 50°C
Storage Temperature Range	−65°C to +125°C
Maximum Junction Temperature	125°C
TSSOP θ_{JA} Thermal Impedance	150.4°C/W
Lead Temperature, Soldering	
Vapor Phase (60 sec)	235°C
Infrared (15 sec)	240°C

[1] This device is a high performance, RF-integrated circuit with an ESD rating of <1 kV. It is ESD sensitive. Take proper precautions for handling and assembly.
[2] GND = RF_{GND} = D_{GND} = 0 V.

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those listed in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Electrostatic charges as high as 4000 V readily accumulate on the human body and test equipment and can discharge without detection. Although this product features proprietary ESD protection circuitry, permanent damage may occur on devices subjected to high energy electrostatic discharges. Therefore, proper ESD precautions are recommended to avoid performance degradation or loss of functionality.

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

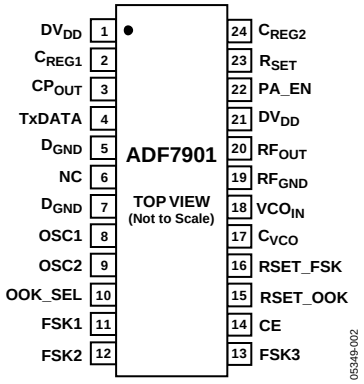

Figure 2. Pin Configuration

Table 3. Pin Function Descriptions

Pin No.	Mnemonic	Function
1	DV_{DD}	Positive Supply for the Digital Circuitry. This must be 3.0 V. Decoupling capacitors to the analog ground plane should be placed as close as possible to this pin.
2	C_{REG1}	A 2.2 µF capacitor should be added at CREG1 to reduce regulator noise and improve stability. A reduced capacitor improves regulator power-on time but can cause higher spurious.
3	CP_{OUT}	Charge Pump Output. This output generates current pulses that are integrated in the loop filter. The integrated current changes the control voltage on the input to the VCO.
4	TxDATA	Digital FSK data to be transmitted is inputted on this pin.
5	D_{GND}	Ground for Digital Section.
6	NC	No Connect.
7	D_{GND}	Ground for Digital Section.
8	OSC1	The reference crystal should be connected between this pin and the OSC2 pin. The necessary crystal load capacitor should be tied between this pin and ground.
9	OSC2	The reference crystal should be connected between this pin and the OSC1 pin. The necessary crystal load capacitor should be tied between this pin and ground. A TCXO or external square wave can also be connected to this pin, with OSC1 left floating. A DC-blocking capacitor (4.7 nF is adequate) should be placed between the TCXO output and OSC2 pin. When not using an external regulator, a 1 MΩ resistor can be tied between the OSC2 pin and ground to meet the power-down current specification of 1 µA.
10	OOK_SEL	A high on this pin selects operation in OOK mode at 384 MHz when CE is high.
11	FSK1	FSK Channel Select Pin. This represents the LSB of the channel select pins.
12	FSK2	FSK Channel Select Pin.
13	FSK3	FSK Channel Select Pin.
14	CE	Bringing CE low puts the ADF7901 into power-down, drawing <1 µA of current.
15	RSET_OOK	The value of this resistor sets the output power for data = 1 in OOK mode. A resistor of 3.6 kΩ provides the maximum output power. Increasing the resistor reduces the power and the current consumption. A lower resistor value than 3.6 kΩ can be used to increase the power to a maximum of 14 dBm. The PA does not operate efficiently in this mode.
16	RSET_FSK	The value of this resistor sets the output power in FSK mode. A resistor of 3.6 kΩ provides maximum output power. Increasing the resistor reduces the power and the current consumption. A resistor value lower than 3.6 kΩ can be used to increase the power to a maximum of 14 dBm. The PA does not operate efficiently in this mode.
17	C_{VCO}	A 22 nF capacitor should be tied between the C_{VCO} and C_{REG2} pins. This line should run underneath the ADF7901. The capacitor is necessary to ensure stable VCO operation.
18	VCO_{IN}	The tuning voltage on this pin determines the output frequency of the voltage controlled oscillator (VCO). The higher the tuning voltage the higher the output frequency. The output of the loop filter is connected here.
19	RF_{GND}	Ground for Output Stage of Transmitter.
20	RF_{OUT}	The modulated signal is available at this pin. Output power levels are from –5 dBm to +12 dBm. The output should be impedance matched using suitable components to the desired load.

Pin No.	Mnemonic	Function
21	DV_{DD}	Voltage Supply for VCO and PA Section. It should be supplied with 3.0 V. Decoupling capacitors to the ground plane should be placed as close as possible to this pin.
22	PA_EN	This pin is used to enable the power amplifier. It should be modulated with the OOK data in OOK mode. In FSK mode, it should be enabled when the PLL is locked.
23	R_{SET}	External Resistor. Sets charge pump current and some internal bias currents. Use 3.6 kΩ as default.
24	C_{REG2}	A 2.2 µF capacitor should be added at C_{REG2} to reduce regulator noise and improve stability. A reduced capacitor improves regulator power-on time but can cause higher spurs.

TYPICAL PERFORMANCE CHARACTERISTICS

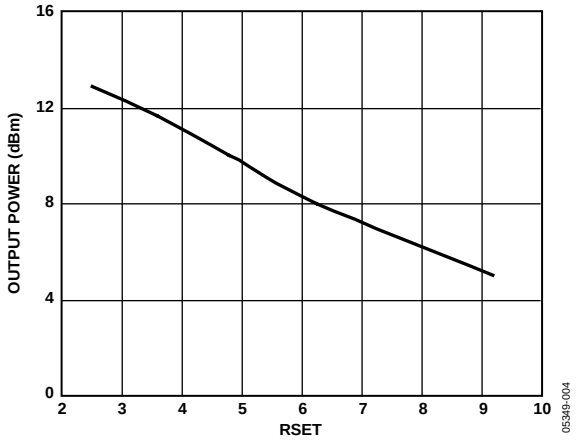

Figure 3. Output Power vs. R_{SET} FSK, Upper FSK Channels, Measured into 50 Ω

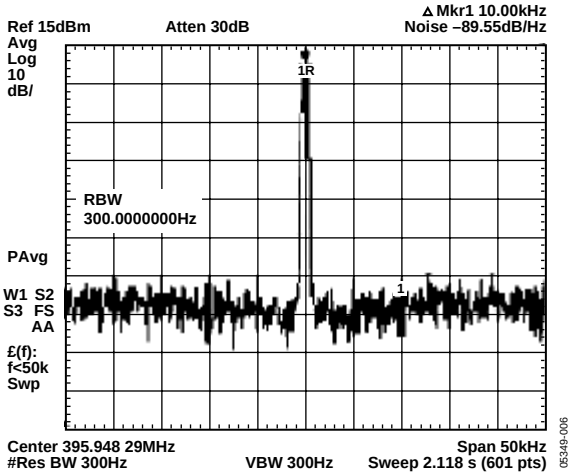

Figure 5. Phase Noise at Channel 9

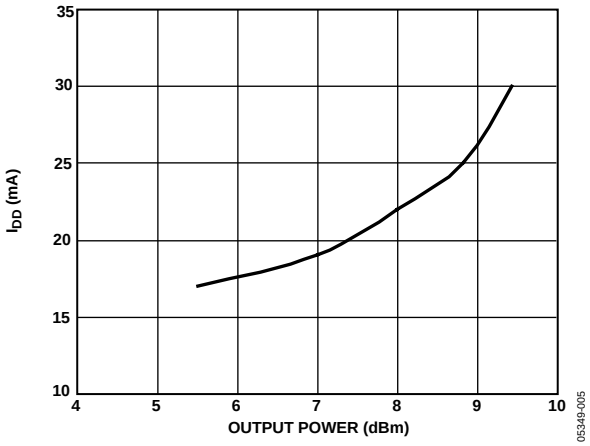

Figure 4. Current Consumption vs. Output Power, Upper FSK Channels, Measured into 50 Ω

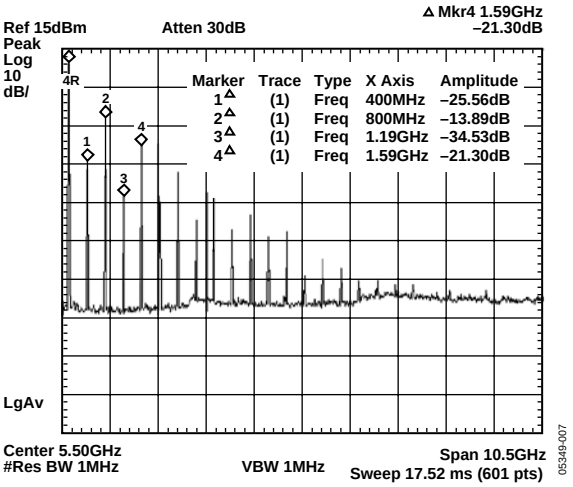

Figure 6. Harmonic Levels—Up to Fourth Harmonic, Measured at Channel 9 into 50 Ω

CIRCUIT DESCRIPTION

Table 4.

Frequency (MHz)	FSK3	FSK2	FSK1	OOK_SEL
369.5	0	0	0	0
371.1	0	0	1	0
375.3	0	1	0	0
376.9	0	1	0	0
384.0	Don't care	Don't care	Don't care	1
388.3	1	0	0	0
391.5	1	0	1	0
394.3	1	1	0	0
395.9	1	1	1	0

LOOP FILTER

The loop filter integrates the current pulses from the charge pump to form a voltage that tunes the output of the VCO to the desired frequency. It also attenuates spurious levels generated by the PLL. The recommended loop filter design for this circuit is 297 kHz. This is based on the trade-off between attenuation of beat note spurs and the need to minimize chirp when the PA is turned on.

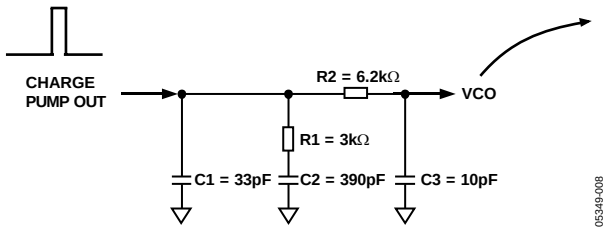

Figure 7.

Improved spurious performance in FSK mode can be achieved by using a narrower loop bandwidth. For a data rate of 20 kbps, a loop bandwidth of roughly 50 kHz would be suitable. The following components give a loop bandwidth of 51.1 kHz:

C1 = 680 pF

C2 = 15 nF

C3 = 180 pF

R1 = 510 Ω

R2 = 6.2 kΩ

ADIsimPLL is a free software tool offered by Analog Devices for assistance in designing with ADI's frequency synthesizers and ISM band transmitters. To select the correct loop filter components for use with the ADF7901, open a project for the ADF7012 device. Then, enter the desired output carrier frequency and loop bandwidth, and use the 870 µA charge pump current setting.

ADIsimPLL can be downloaded from www.analog.com.

CHANNEL FREQUENCIES

The nine channel frequencies listed in Table 4 are obtainable from a single 9.8304 MHz crystal reference by changing the value of the N and F numbers in the fractional PLL, using control lines FSK1, FSK2, and FSK3. The channel frequency is given by

$$F_{CHANNEL} = F_{REF} \times (N + F)$$

However, the VCO is tuned to operate over a frequency range of 344 MHz to 401 MHz (typically). Therefore, any channel frequency within this range can be obtained if the required reference frequency is used. The N and F numbers for each channel are listed in Table 5, together with the corresponding channel frequencies for 9.8304 MHz and, for example purposes, frequencies for 10 MHz. With the 10 MHz reference, the two largest N settings give channel frequencies above the maximum VCO output frequency and are therefore invalid.

Frequency deviation is also dependent on reference frequency. The relationship is given by

$$F_{DEV} = 58 \times (9.8304\ \text{MHz})/2^{14}$$

Therefore, the frequency deviation is 34.8 kHz when the 9.8304 MHz reference is used and 35.4 kHz when the 10 MHz reference is used.

Table 5.

		Channel Frequency (MHz)	
N	F	9.8304 MHz Ref	10 MHz Ref
37	2406/4096	369.5	375.9
37	3073/4096	371.1	377.5
38	727/4096	375.3	381.8
38	1374/4096	376.9	383.4
39	256/4096	384.0	390.6
39	2048/4096	388.3	395
39	3381/4096	391.5	398.3
40	452/4096	394.3	N/A
40	1118/4096	395.9	N/A

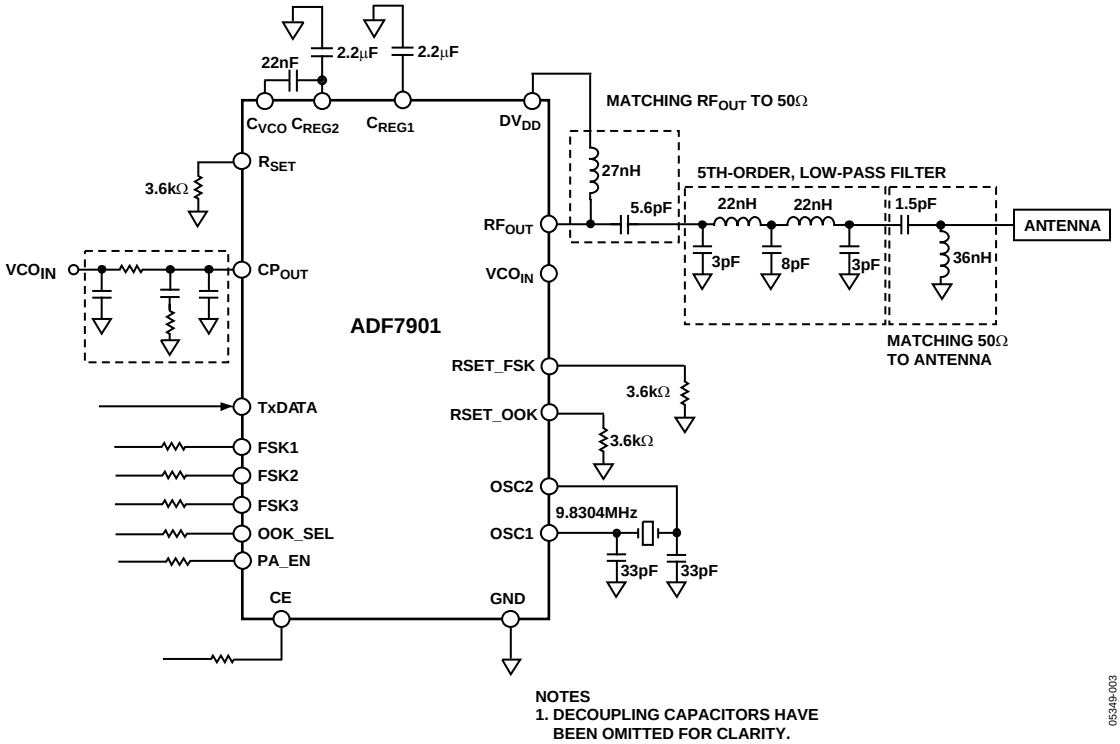

Figure 8. Applications Diagram for the ADF7901 in a Remote Control System

LAYOUT GUIDELINES

The layout of the board is crucial to ensuring low levels of spurious and harmonics.

Decoupling

Decoupling capacitors (high frequency 22 pF, low frequency 100 nF) should be placed as close as possible to the supply pins on the part. Low size 0402 and 0603 components are recommended for the high frequency rejection on the supply.

Regulator Stability

A minimum of 1 µF is needed on both C_{REG1} and C_{REG2} to ensure stability. An additional 22 pF capacitor can be added to reject higher frequency noise. Because many of the internal blocks run off the regulator, it is critical to reduce its noise. Low size 0402 and 0603 components are recommended for the high frequency rejection on the supply.

Grounding

Emphasis should be placed on grounding once the decoupling capacitors have been added. The PA stage switches currents of 15 mA in maximum power mode. This causes changes in the ground resulting in large return currents that can radiate to other parts of the board. The shortest and least obstructed ground from RF_{GND} back to the ground of the battery should be ensured. A 4-layer board helps, as well as flooding the top layer. The ground paths should not have any vias and should be wide tracks.

Supply

The supply tracks can be routed through vias, because they act as free inductors and make layout easier on a 2-layer board (see the Decoupling section). Tracks should be wide.

Digital Lines

Digital lines should contain a large resistor in series. This impedance blocks signals of many frequencies, including harmonics and the carrier frequency. Long control lines can act as antennae. It can be useful to add capacitance to ground. There is some capacitance to ground provided by the lines and at the input of the digital pins.

OUTLINE DIMENSIONS

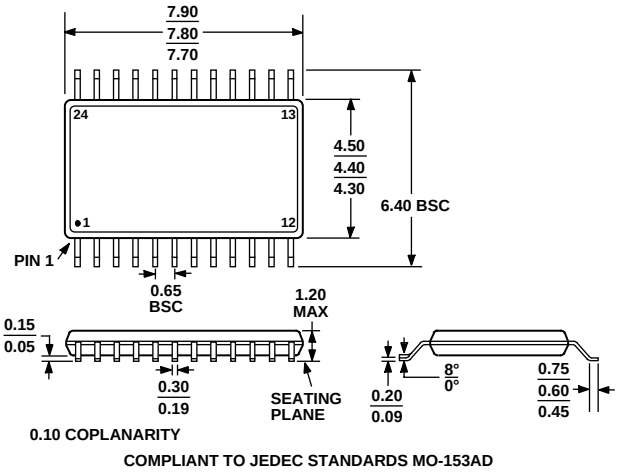

Figure 9. 24-Lead Thin Shrink Small Outline Package [TSSOP]
(RU-24)
Dimensions shown in millimeters

ORDERING GUIDE

Model	Temperature Range	Package Description	Package Option
ADF7901BRU	0°C to 50°C	24-Lead Thin Shrink Small Outline Package (TSSOP)	RU-24
ADF7901BRU-REEL	0°C to 50°C	24-Lead Thin Shrink Small Outline Package (TSSOP)	RU-24
ADF7901BRU-REEL7	0°C to 50°C	24-Lead Thin Shrink Small Outline Package (TSSOP)	RU-24
ADF7901BRUZ[1]	0°C to 50°C	24-Lead Thin Shrink Small Outline Package (TSSOP)	RU-24
ADF7901BRUZ-RL[1]	0°C to 50°C	24-Lead Thin Shrink Small Outline Package (TSSOP)	RU-24
ADF7901BRUZ-RL7[1]	0°C to 50°C	24-Lead Thin Shrink Small Outline Package (TSSOP)	RU-24
EVAL-ADF7901EB		Evaluation Board	

[1] Z = Pb-free part.

NOTES

D05349-0-3/06(A)