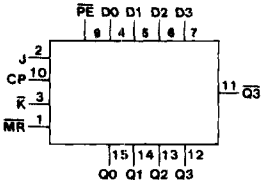
File Number **1482**

CD54/74HC195
CD54/74HCT195

High-Speed CMOS Logic

4-Bit Parallel Access Register



FUNCTIONAL DIAGRAM

Type Features:

- *Asynchronous Master Reset*
- *J, $\overline{K}$, (D) inputs to first stage*
- *Fully synchronous serial or parallel data transfer*
- *Shift right and parallel load capability*
- *Complementary output from last stage*
- *Buffered inputs*
- *Typical f_{MAX}=50 MHz @ V_{CC}=5 V, C_L=15 pF, T_A=25°C*

The functional characteristics of the RCA-CD54/74HC195 and CD54/74HCT195 4-Bit Parallel Access Register are indicated in the Logic Diagram and Function Table. The device is useful in a wide variety of shifting, counting and storage applications. It performs serial, parallel, serial-to-parallel, or parallel-to-serial data transfers at very high speeds.

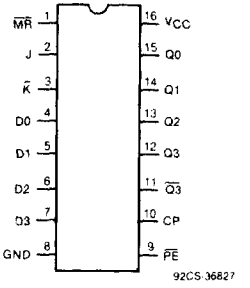
The two modes of operation, shift right (Q0-Q1) and parallel load, are controlled by the state of the Parallel Enable ($\overline{PE}$) input. Serial data enters the first flip-flop (Q0) via the J and $\overline{K}$ inputs when the $\overline{PE}$ input is high, and is shifted one bit in the direction Q0-Q1-Q2-Q3 following each LOW-to-HIGH clock transition. The J and $\overline{K}$ inputs provide the flexibility of the JK-type input for special applications and, by tying the two pins together, the simple D-type input for general applications. The device appears as four common-clocked D flip-flops when the $\overline{PE}$ input is LOW. After the LOW-to-HIGH clock transition, data on the parallel inputs (D0-D3) is transferred to the respective Q0-Q3 outputs. Shift left operation (Q3-Q2) can be achieved by tying the Qn outputs to the Dn-1 inputs and holding the $\overline{PE}$ input low.

All parallel and serial data transfers are synchronous, occurring after each LOW-to-HIGH clock transition. The HC/HCT195 series utilizes edge-triggering; therefore, there is no restriction on the activity of the J, $\overline{K}$, Pn and $\overline{PE}$ inputs for logic operations, other than the set-up and hold time requirements. A LOW on the asynchronous Master Reset ($\overline{MR}$) input sets all Q outputs LOW, independent of any other input condition.

The CD54HC195 and CD54HCT195 are supplied in 16-lead hermetic dual-in-line ceramic packages (F suffix). The CD74HC195 and CD74HCT195 are supplied in 16-lead dual-in-line plastic packages (E suffix) and in 16-lead dual-in-line surface mount plastic package (M suffix). Both types are also available in chip form (H suffix).

Family Features:

- *Fanout (Over Temperature Range):*
  Standard Outputs - 10 LSTTL Loads
  Bus Driver Outputs - 15 LSTTL Loads
- *Wide Operating Temperature Range:*
  CD74HC/HCT: −40 to +85°C
- *Balanced Propagation Delay and Transition Times*
- *Significant Power Reduction Compared to LSTTL Logic ICs*
- *Alternate Source is Philips/Signetics*
- *CD54HC/CD74HC Types:*
  2 to 6 V Operation
  High Noise Immunity: N_{IL}=30%, N_{IH}=30% of V_{CC} @ V_{CC}=5 V
- *CD54HCT/CD74HCT Types:*
  4.5 to 5.5 V Operation
  Direct LSTTL Input Logic Compatibility
  V_{IL}=0.8 V Max., V_{IH}=2 V Min.
  CMOS Input Compatibility
  $I_I \leq 1\ \mu A$ @ V_{OL}, V_{OH}



TERMINAL ASSIGNMENT

CD54/74HC195
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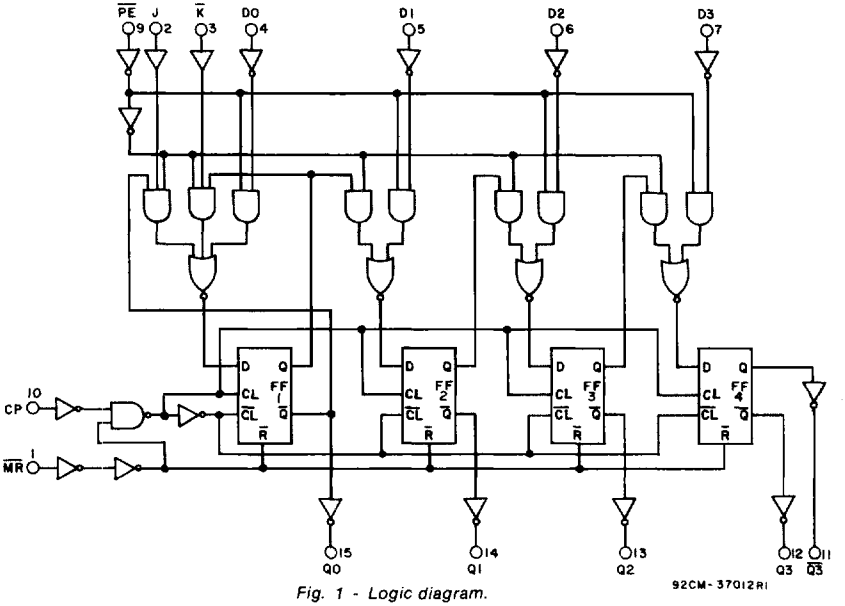

Fig. 1 - Logic diagram.

Function Table

Operating Modes	INPUTS						OUTPUTS				
	$\overline{MR}$	$\overline{CP}$	PE	J	$\overline{K}$	D_n	Q0	Q1	Q2	Q3	$\overline{Q3}$
Asynchronous Reset	L	X	X	X	X	X	L	L	L	L	H
Shift, Set first stage	H	⎍	h	h	h	X	H	q_0	q_1	q_2	$\overline{q}_2$
Shift, Reset first stage	H	⎍	h	l	l	X	L	q_0	q_1	q_2	$\overline{q}_2$
Shift, Toggle first stage	H	⎍	h	h	l	X	$\overline{q}_0$	q_0	q_1	q_2	$\overline{q}_2$
Shift, Retain first stage	H	⎍	h	l	h	X	q_0	q_0	q_1	q_2	$\overline{q}_2$
Parallel Load	H	⎍	l	X	X	d_n	d_0	d_1	d_2	d_3	$\overline{d}_3$

H=HIGH voltage level.
L=LOW voltage level.
X=Don't care.
l=LOW voltage level one set-up time prior to the LOW-to-HIGH clock transition.
h=HIGH voltage level one set-up time prior to the LOW-to-HIGH clock transition.
d_n (q_n)=Lower case letters indicate the state of the referenced input (or output) one set-up time prior to the LOW-to-HIGH clock transition.
⎍=LOW-to-HIGH clock transition.

MAXIMUM RATINGS, *Absolute-Maximum Values:*

DC SUPPLY-VOLTAGE, (V_{CC}):
(Voltages referenced to ground) ..... -0.5 to + 7 V
DC INPUT DIODE CURRENT, I_{IK} (FOR $V_I < -0.5$ V OR $V_I > V_{CC} + 0.5$V) ..... ±20mA
DC OUTPUT DIODE CURRENT, I_{OK} (FOR $V_o < -0.5$ V OR $V_o > V_{CC} + 0.5$V) ..... ±20mA
DC DRAIN CURRENT, PER OUTPUT (I_o) (FOR $-0.5\ V < V_o < V_{CC} + 0.5$V) ..... ±25mA
DC V_{CC} OR GROUND CURRENT (I_{CC}) ..... ±50mA
POWER DISSIPATION PER PACKAGE (P_D):
For T_A = -40 to +60° C (PACKAGE TYPE E) ..... 500 mW
For T_A = +60 to +85° C (PACKAGE TYPE E) ..... Derate Linearly at 8 mW/° C to 300 mW
For T_A = -55 to +100° C (PACKAGE TYPE F, H) ..... 500 mW
For T_A = +100 to +125° C (PACKAGE TYPE F, H) ..... Derate Linearly at 8 mW/° C to 300 mW
For T_A = -40 to +70° C (PACKAGE TYPE M) ..... 400 mW
For T_A = +70 to +125° C (PACKAGE TYPE M) ..... Derate Linearly at 6 mW/° C to 70 mW
OPERATING-TEMPERATURE RANGE (T_A):
PACKAGE TYPE F, H ..... -55 to +125° C
PACKAGE TYPE E, M ..... -40 to +85° C
STORAGE TEMPERATURE (T_{stg}) ..... -65 to +150° C
LEAD TEMPERATURE (DURING SOLDERING):
At distance 1/16 ± 1/32 in. (1.59 ± 0.79 mm) from case for 10 s max. ..... +265° C
Unit inserted into a PC Board (min. thickness 1/16 in., 1.59 mm)
with solder contacting lead tips only ..... +300° C

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STATIC ELECTRICAL CHARACTERISTICS

CHARACTERISTIC	CD74HC195/CD54HC195										CD74HCT195/CD54HCT195								UNITS
	TEST CONDITIONS			74HC/54HC TYPES			74HC TYPES		54HC TYPES		TEST CONDITIONS		74HCT/54HCT TYPES			74HCT TYPES		54HCT TYPES	
	V_I V	I_O mA	V_{CC} V	+25°C			-40/ +85°C		-55/ +125°C		V_I V	V_{CC} V	+25°C			-40/ +85°C		-55/ +125°C	
				Min	Typ	Max	Min	Max	Min	Max			Min	Typ	Max	Min	Max	Min	Max	
High-Level Input Voltage V_{IH}			2	1.5	—	—	1.5	—	1.5	—	—	4.5 to 5.5	2	—	—	2	—	2	—	V
			4.5	3.15	—	—	3.15	—	3.15	—										
			6	4.2	—	—	4.2	—	4.2	—										
Low-Level Input Voltage V_{IL}			2	—	—	0.5	—	0.5	—	0.5	—	4.5 to 5.5	—	—	0.8	—	0.8	—	0.8	V
			4.5	—	—	1.35	—	1.35	—	1.35										
			6	—	—	1.8	—	1.8	—	1.8										
High-Level Output Voltage V_{OH} CMOS Loads	V_{IL} or V_{IH}	-0.02	2	1.9	—	—	1.9	—	1.9	—	V_{IL} or V_{IH}	4.5	4.4	—	—	4.4	—	4.4	—	V
			4.5	4.4	—	—	4.4	—	4.4	—										
			6	5.9	—	—	5.9	—	5.9	—										
TTL Loads	V_{IL} or V_{IH}	-4	4.5	3.98	—	—	3.84	—	3.7	—	V_{IL} or V_{IH}	4.5	3.98	—	—	3.84	—	3.7	—	V
		-5.2	6	5.48	—	—	5.34	—	5.2	—										
Low-Level Output Voltage V_{OL} CMOS Loads	V_{IL} or V_{IH}	0.02	2	—	—	0.1	—	0.1	—	0.1	V_{IL} or V_{IH}	4.5	—	—	0.1	—	0.1	—	0.1	V
			4.5	—	—	0.1	—	0.1	—	0.1										
			6	—	—	0.1	—	0.1	—	0.1										
TTL Loads	V_{IL} or V_{IH}	4	4.5	—	—	0.26	—	0.33	—	0.4	V_{IL} or V_{IH}	4.5	—	—	0.26	—	0.33	—	0.4	V
		5.2	6	—	—	0.26	—	0.33	—	0.4										
Input Leakage Current I_I	V_{CC} or Gnd		6	—	—	±0.1	—	±1	—	±1	Any Voltage Between V_{CC} & Gnd	5.5	—	—	±0.1	—	±1	—	±1	μA
Quiescent Device Current I_{CC}	V_{CC} or Gnd	0	6	—	—	8	—	80	—	160	V_{CC} or Gnd	5.5	—	—	8	—	80	—	160	μA
Additional Quiescent Device Current per input pin: 1 unit load ΔI_{CC}*											V_{CC}-2.1	4.5 to 5.5	—	100	360	—	450	—	490	μA

*For dual-supply systems theoretical worst case (V_I = 2.4 V, V_{CC} = 5.5 V) specification is 1.8 mA.

HCT Input Loading Table

Input	Unit Loads*
D0-D3	0.3
$\overline{PE}$	0.65
$\overline{MR}$	0.3
CP	0.3
J, $\overline{K}$	0.3

*Unit Load is ΔI_{CC} limit specified in Static Characteristic Chart, e.g., 360 μA max. @ 25°C.

CD54/74HC195
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RECOMMENDED OPERATING CONDITIONS:

For maximum reliability, nominal operating conditions should be selected so that operation is always within the following ranges:

CHARACTERISTIC	LIMITS		UNITS
	MIN.	MAX.	
Supply-Voltage Range (For T_A=Full Package Temperature Range) V_{CC}*			
CD54/74HC Types	2	6	V
CD54/74HCT Types	4.5	5.5	V
DC Input or Output Voltage V_{in}, V_{out}	0	V_{CC}	V
Operating Temperature T_A:			
CD74 Types	-40	+85	°C
CD54 Types	-55	+125	°C
Input Rise and Fall Times t_r,t_f			
at 2 V	0	1000	ns
at 4.5 V	0	500	ns
at 6 V	0	400	ns

*Unless otherwise specified, all voltages are referenced to Ground.

SWITCHING CHARACTERISTICS (V_{CC} = 5 V, T_A = 25° C, Input t_r, t_f = 6 ns)

CHARACTERISTIC	SYMBOL	C_L pF	Typical		Units
			HC	HCT	
CP to Qn Propagation Delay	t_{PHL} t_{PLH}	15	14	14	ns
$\overline{MR}$ to Qn	t_{PHL}	15	13	14	ns
Maximum Clock Frequency	f_{MAX}	15	50	50	MHz
Power Dissipation Capacitance*	C_{PD}	—	45	50	pF

*C_{PD} is used to determine the dynamic power consumption, per register.

$PD = C_{PD} Vcc^2 fi + \Sigma C_L Vcc^2 fo$ where

fi = input frequency

fo = output frequency

C_L = output load capacitance

Vcc = supply voltage.

Pre-requisite for Switching Function

CHARACTERISTIC	SYMBOL	V_{CC}	25°C				-40°C to +85°C				-55°C to +125°C				UNITS
			HC		HCT		74HC		74HCT		54HC		54HCT		
			Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
Clock Frequency	f_{MAX}	2	6	—	—	—	5	—	—	—	4	—	—	—	
(Figure 3)		4.5	30	—	25	—	25	—	20	—	20	—	16	—	ns
		6	35	—	—	—	29	—	—	—	23	—	—	—	
$\overline{MR}$ Pulse Width	t_w	2	80	—	—	—	100	—	—	—	120	—	—	—	
(Figure 3)		4.5	16	—	20	—	20	—	25	—	24	—	30	—	ns
		6	14	—	—	—	17	—	—	—	20	—	—	—	
Clock Pulse Width	t_w	2	80	—	—	—	100	—	—	—	120	—	—	—	
(Figure 3)		4.5	16	—	20	—	20	—	25	—	24	—	30	—	ns
		6	14	—	—	—	17	—	—	—	20	—	—	—	
Set-up Time	t_{su}	2	100	—	—	—	125	—	—	—	150	—	—	—	
J, $\overline{K}$, $\overline{PE}$ to Clock		4.5	20	—	20	—	25	—	25	—	30	—	30	—	ns
(Figure 5)		6	17	—	—	—	21	—	—	—	26	—	—	—	
Hold Time	t_h	2	3	—	—	—	3	—	—	—	3	—	—	—	
J, $\overline{K}$, $\overline{PE}$ to Clock		4.5	3	—	3	—	3	—	3	—	3	—	3	—	ns
(Figure 5)		6	3	—	—	—	3	—	—	—	3	—	—	—	
Removal Time	t_{REM}	2	80	—	—	—	100	—	—	—	120	—	—	—	
$\overline{MR}$ to Clock		4.5	16	—	16	—	20	—	20	—	24	—	24	—	ns
(Figure 3)		6	14	—	—	—	17	—	—	—	20	—	—	—	

SWITCHING CHARACTERISTICS (C_L=50 pF, Input t_r,t_f=6 ns)

CHARACTERISTIC	SYMBOL	V_{CC}	25°C				-40°C to +85°C				-55°C to +125°C				UNITS
			HC		HCT		74HC		74HCT		54HC		54HCT		
			Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
Propagation Delay	t_{PLH}	2	—	175	—	—	—	220	—	—	—	265	—	—	
CP to Output	t_{PHL}	4.5	—	35	—	35	—	44	—	44	—	53	—	53	ns
(Figure 3)		6	—	30	—	—	—	37	—	—	—	45	—	—	
Propagation Delay	t_{PHL}	2	—	150	—	—	—	190	—	—	—	225	—	—	
$\overline{MR}$ to Output	t_{PLH}	4.5	—	30	—	35	—	38	—	44	—	45	—	53	ns
(Figure 3)		6	—	26	—	—	—	33	—	—	—	38	—	—	
Output Transition	t_{TLH}	2	—	75	—	—	—	95	—	—	—	110	—	—	
Time	t_{THL}	4.5	—	15	—	15	—	19	—	19	—	22	—	22	ns
		6	—	13	—	—	—	16	—	—	—	19	—	—	
Input Capacitance	C_I		—	10	—	10	—	10	—	10	—	10	—	10	pF

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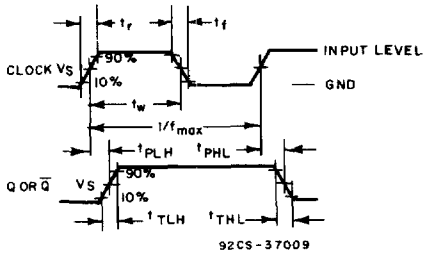

Fig. 3 - Clock pre-requisite and propagation delays and output transition times.

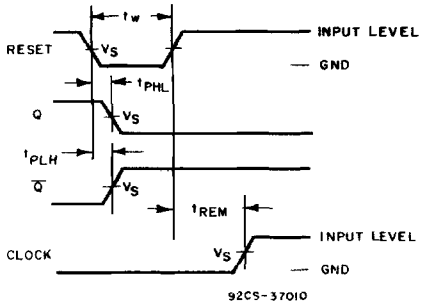

Fig. 4 - Master Reset pre-requisite and propagation delays.

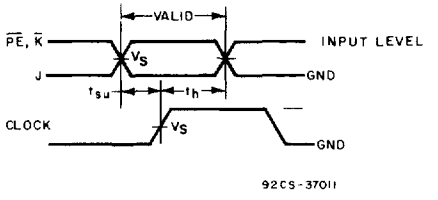

Fig. 5 - J, $\overline{K}$ or Parallel Enable pre-requisite times.

	HC	HCT
INPUT LEVEL	V_{CC}	3V
V_S	50%	1.3V