



# PMDT290UNE

20 V, 800 mA dual N-channel Trench MOSFET

28 December 2022

Product data sheet

## 1. General description

Dual N-channel enhancement mode Field-Effect Transistor (FET) in an ultra small and flat lead SOT666 Surface-Mounted Device (SMD) plastic package using Trench MOSFET technology.

## 2. Features and benefits

- Very fast switching
- Trench MOSFET technology
- ESD protection up to 2 kV

## 3. Applications

- Relay driver
- High-speed line driver
- Low-side loadswitch
- Switching circuits

## 4. Quick reference data

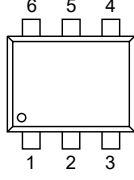
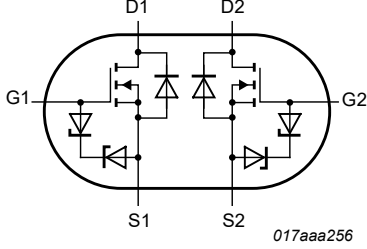
Table 1. Quick reference data

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
<b>Per transistor</b>						
$V_{DS}$	drain-source voltage	$T_j = 25\text{ °C}$	-	-	20	V
$V_{GS}$	gate-source voltage		-8	-	8	V
$I_D$	drain current	$V_{GS} = 4.5\text{ V}; T_{amb} = 25\text{ °C}$	[1]	-	800	mA
<b>Static characteristics (per transistor)</b>						
$R_{DSon}$	drain-source on-state resistance	$V_{GS} = 4.5\text{ V}; I_D = 500\text{ mA}; T_j = 25\text{ °C}$	-	290	380	m $\Omega$

[1] Device mounted on an FR4 Printed-Circuit Board (PCB), single-sided copper, tin-plated, mounting pad for drain 1 cm<sup>2</sup>.

## 5. Pinning information

Table 2. Pinning information

Pin	Symbol	Description	Simplified outline	Graphic symbol
1	S1	source TR1	 <p><b>SOT666</b></p>	 <p>017aaa256</p>
2	G1	gate TR1		
3	D2	drain TR2		
4	S2	source TR2		
5	G2	gate TR2		
6	D1	drain TR1		

## 6. Ordering information

Table 3. Ordering information

Type number	Package		
	Name	Description	Version
PMDT290UNE	SOT666	plastic, surface-mounted package; 6 leads; 0.5 mm pitch; 1.6 mm x 1.2 mm x 0.55 mm body	SOT666

## 7. Marking

Table 4. Marking codes

Type number	Marking code
PMDT290UNE	AE

## 8. Limiting values

**Table 5. Limiting values**

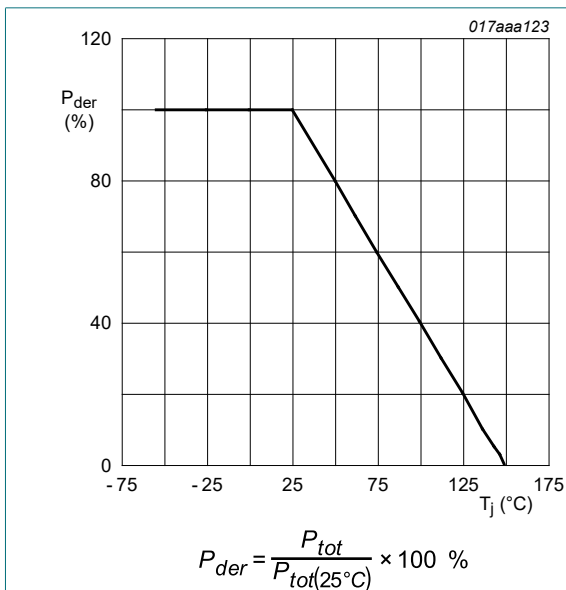
In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions		Min	Max	Unit
<b>Per transistor</b>						
V <sub>DS</sub>	drain-source voltage	T <sub>j</sub> = 25 °C		-	20	V
V <sub>GS</sub>	gate-source voltage			-8	8	V
I <sub>D</sub>	drain current	V <sub>GS</sub> = 4.5 V; T <sub>amb</sub> = 25 °C	[1]	-	800	mA
		V <sub>GS</sub> = 4.5 V; T <sub>amb</sub> = 100 °C	[1]	-	500	mA
I <sub>DM</sub>	peak drain current	T <sub>amb</sub> = 25 °C; single pulse; t <sub>p</sub> ≤ 10 μs		-	3.2	A
P <sub>tot</sub>	total power dissipation	T <sub>amb</sub> = 25 °C	[2]	-	330	mW
			[1]	-	390	mW
		T <sub>sp</sub> = 25 °C		-	1090	mW
<b>Per device</b>						
P <sub>tot</sub>	total power dissipation	T <sub>amb</sub> = 25 °C	[2]	-	500	mW
T <sub>j</sub>	junction temperature			-55	150	°C
T <sub>amb</sub>	ambient temperature			-55	150	°C
T <sub>stg</sub>	storage temperature			-65	150	°C
<b>Source-drain diode</b>						
I <sub>S</sub>	source current	T <sub>amb</sub> = 25 °C		-	370	mA
<b>ESD maximum rating</b>						
V <sub>ESD</sub>	electrostatic discharge voltage	HBM	[3]	-	2000	V

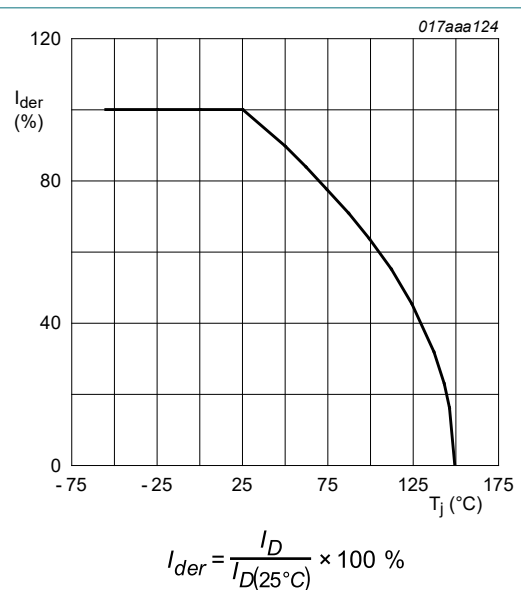
[1] Device mounted on an FR4 Printed-Circuit Board (PCB), single-sided copper, tin-plated, mounting pad for drain 1 cm<sup>2</sup>.

[2] Device mounted on an FR4 Printed-Circuit Board (PCB), single-sided copper, tin-plated and standard footprint.

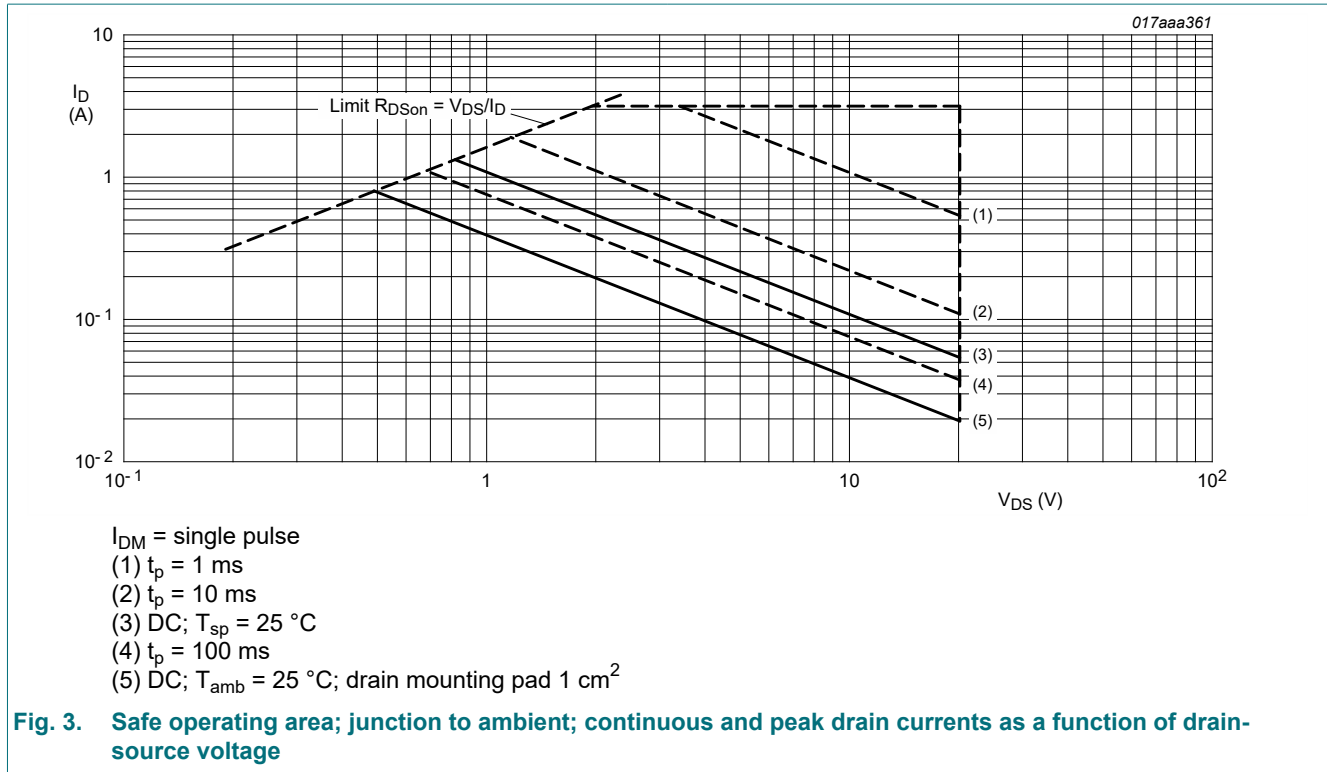
[3] Measured between all pins.



**Fig. 1. Normalized total power dissipation as a function of junction temperature**



**Fig. 2. Normalized continuous drain current as a function of junction temperature**



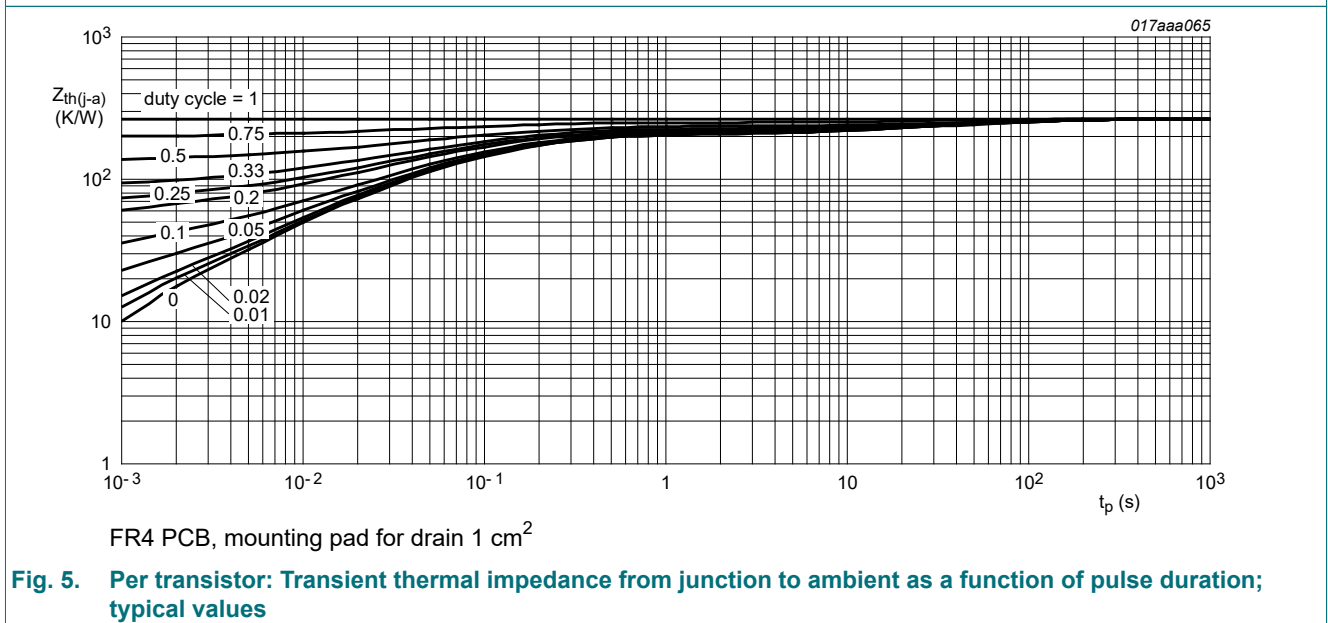
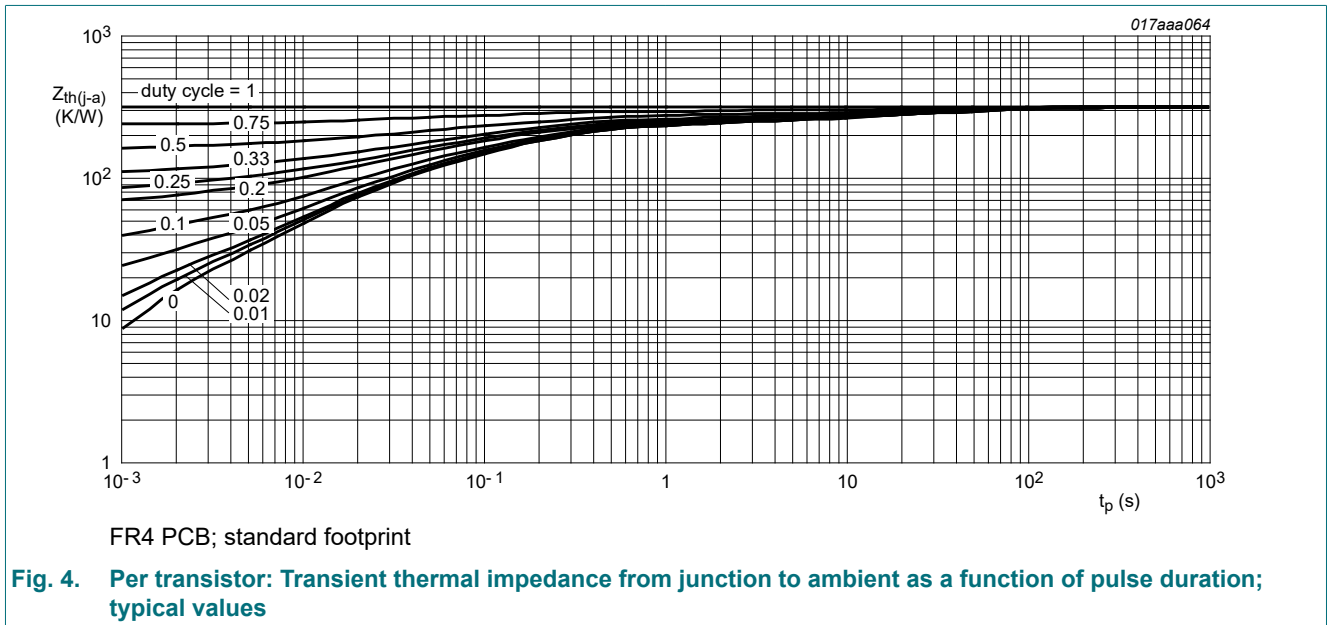
## 9. Thermal characteristics

Table 6. Thermal characteristics

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
<b>Per transistor</b>							
$R_{th(j-a)}$	thermal resistance from junction to ambient	in free air	[1]	-	330	380	K/W
			[2]	-	280	320	K/W
$R_{th(j-sp)}$	thermal resistance from junction to solder point			-	-	115	K/W
<b>Per device</b>							
$R_{th(j-a)}$	thermal resistance from junction to ambient	in free air	[1]	-	-	250	K/W

[1] Device mounted on an FR4 PCB, single-sided copper, tin-plated and standard footprint.

[2] Device mounted on an FR4 PCB, single-sided copper, tin-plated, mounting pad for drain 1 cm<sup>2</sup>.



## 10. Characteristics

Table 7. Characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
<b>Static characteristics (per transistor)</b>						
$V_{(BR)DSS}$	drain-source breakdown voltage	$I_D = 250 \mu\text{A}; V_{GS} = 0 \text{ V}; T_j = 25 \text{ }^\circ\text{C}$	20	-	-	V
$V_{GSth}$	gate-source threshold voltage	$I_D = 250 \mu\text{A}; V_{DS} = V_{GS}; T_j = 25 \text{ }^\circ\text{C}$	0.5	0.75	0.95	V
$I_{DSS}$	drain leakage current	$V_{DS} = 20 \text{ V}; V_{GS} = 0 \text{ V}; T_j = 25 \text{ }^\circ\text{C}$	-	-	1	$\mu\text{A}$
		$V_{DS} = 20 \text{ V}; V_{GS} = 0 \text{ V}; T_j = 150 \text{ }^\circ\text{C}$	-	-	10	$\mu\text{A}$
$I_{GSS}$	gate leakage current	$V_{GS} = 8 \text{ V}; V_{DS} = 0 \text{ V}; T_j = 25 \text{ }^\circ\text{C}$	-	-	2	$\mu\text{A}$
		$V_{GS} = -8 \text{ V}; V_{DS} = 0 \text{ V}; T_j = 25 \text{ }^\circ\text{C}$	-	-	2	$\mu\text{A}$
		$V_{GS} = 4.5 \text{ V}; V_{DS} = 0 \text{ V}; T_j = 25 \text{ }^\circ\text{C}$	-	-	500	nA
		$V_{GS} = -4.5 \text{ V}; V_{DS} = 0 \text{ V}; T_j = 25 \text{ }^\circ\text{C}$	-	-	500	nA
$R_{DSon}$	drain-source on-state resistance	$V_{GS} = 4.5 \text{ V}; I_D = 500 \text{ mA}; T_j = 25 \text{ }^\circ\text{C}$	-	290	380	m $\Omega$
		$V_{GS} = 4.5 \text{ V}; I_D = 500 \text{ mA}; T_j = 150 \text{ }^\circ\text{C}$	-	460	610	m $\Omega$
		$V_{GS} = 2.5 \text{ V}; I_D = 400 \text{ mA}; T_j = 25 \text{ }^\circ\text{C}$	-	420	620	m $\Omega$
		$V_{GS} = 1.8 \text{ V}; I_D = 100 \text{ mA}; T_j = 25 \text{ }^\circ\text{C}$	-	600	1100	m $\Omega$
$g_{fs}$	forward transconductance	$V_{DS} = 10 \text{ V}; I_D = 200 \text{ mA}; T_j = 25 \text{ }^\circ\text{C}$	-	1.6	-	S
<b>Dynamic characteristics (per transistor)</b>						
$Q_{G(tot)}$	total gate charge	$V_{DS} = 10 \text{ V}; I_D = 500 \text{ mA}; V_{GS} = 4.5 \text{ V}; T_j = 25 \text{ }^\circ\text{C}$	-	0.45	0.68	nC
$Q_{GS}$	gate-source charge		-	0.15	-	nC
$Q_{GD}$	gate-drain charge		-	0.15	-	nC
$C_{iss}$	input capacitance	$V_{DS} = 10 \text{ V}; f = 1 \text{ MHz}; V_{GS} = 0 \text{ V}; T_j = 25 \text{ }^\circ\text{C}$	-	55	83	pF
$C_{oss}$	output capacitance		-	15	-	pF
$C_{rss}$	reverse transfer capacitance		-	7	-	pF
$t_{d(on)}$	turn-on delay time		$V_{DS} = 10 \text{ V}; R_L = 250 \Omega; V_{GS} = 4.5 \text{ V}; R_{G(ext)} = 6 \Omega; T_j = 25 \text{ }^\circ\text{C}$	-	6	12
$t_r$	rise time	-		4	-	ns
$t_{d(off)}$	turn-off delay time	-		86	172	ns
$t_f$	fall time	-		31	-	ns
<b>Source-drain diode (per transistor)</b>						
$V_{SD}$	source-drain voltage	$I_S = 300 \text{ mA}; V_{GS} = 0 \text{ V}; T_j = 25 \text{ }^\circ\text{C}$	0.48	0.77	1.2	V

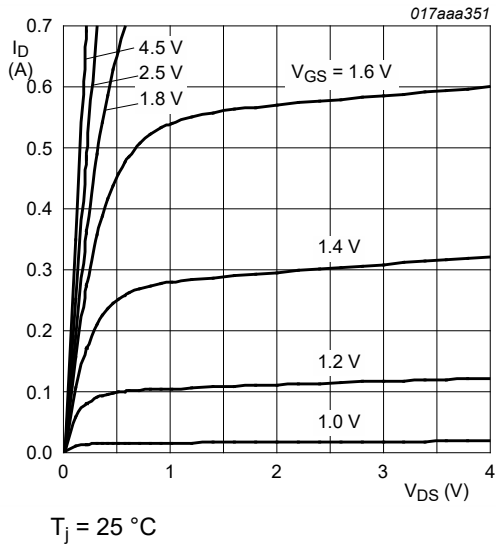


Fig. 6. Output characteristics: drain current as a function of drain-source voltage; typical values

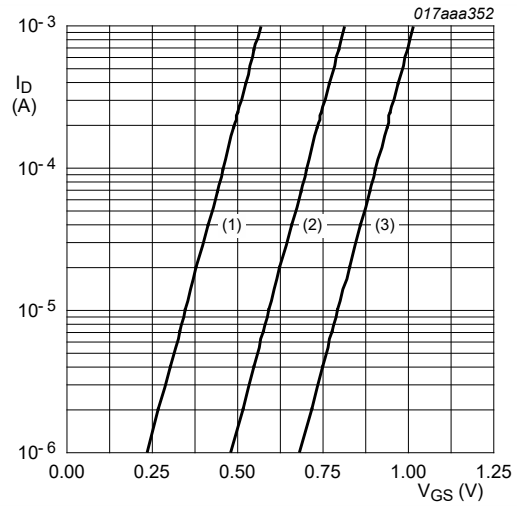
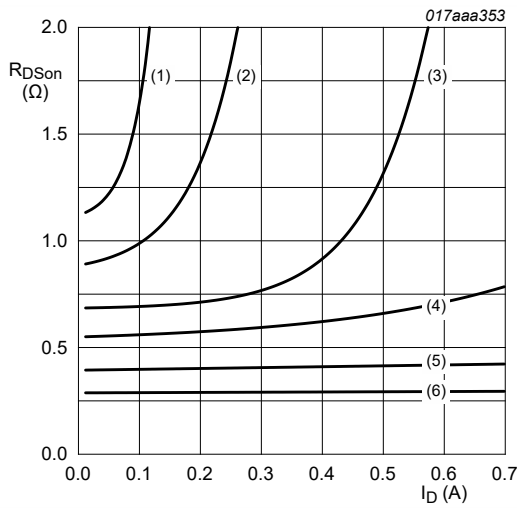


Fig. 7. Sub-threshold drain current as a function of gate-source voltage



- (1)  $V_{GS} = 1.3\text{ V}$
- (2)  $V_{GS} = 1.4\text{ V}$
- (3)  $V_{GS} = 1.6\text{ V}$
- (4)  $V_{GS} = 1.8\text{ V}$
- (5)  $V_{GS} = 2.5\text{ V}$
- (6)  $V_{GS} = 4.5\text{ V}$

Fig. 8. Drain-source on-state resistance as a function of drain current; typical values

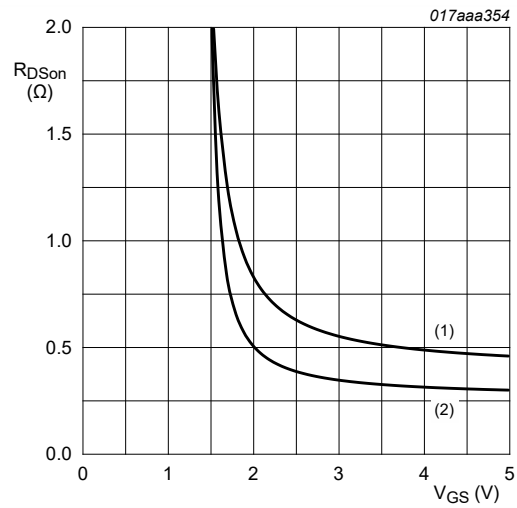


Fig. 9. Drain-source on-state resistance as a function of gate-source voltage; typical values

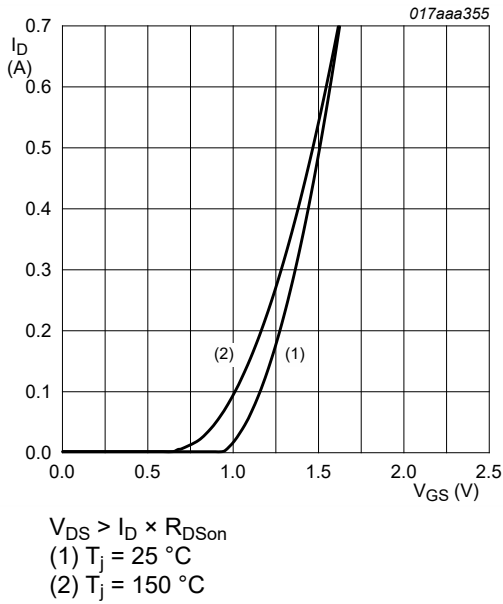


Fig. 10. Transfer characteristics: drain current as a function of gate-source voltage; typical values

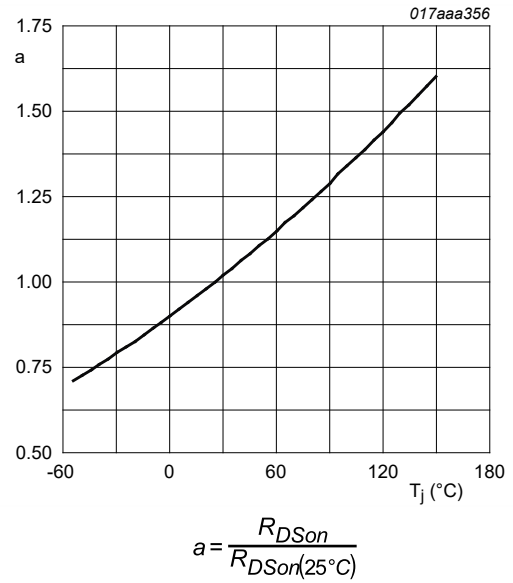


Fig. 11. Normalized drain-source on-state resistance as a function of junction temperature; typical values

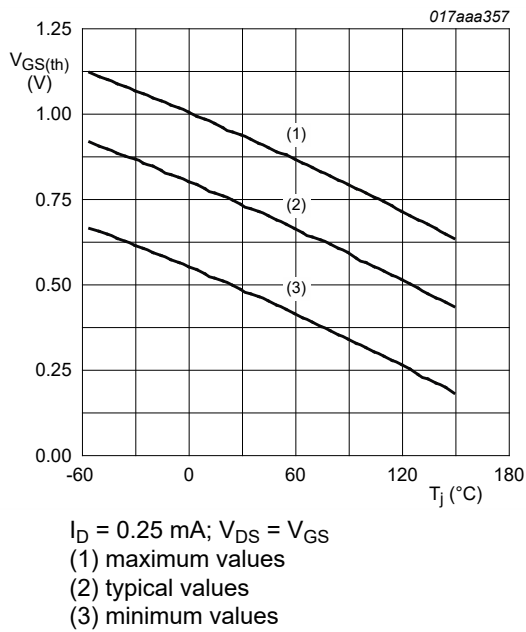


Fig. 12. Gate-source threshold voltage as a function of junction temperature

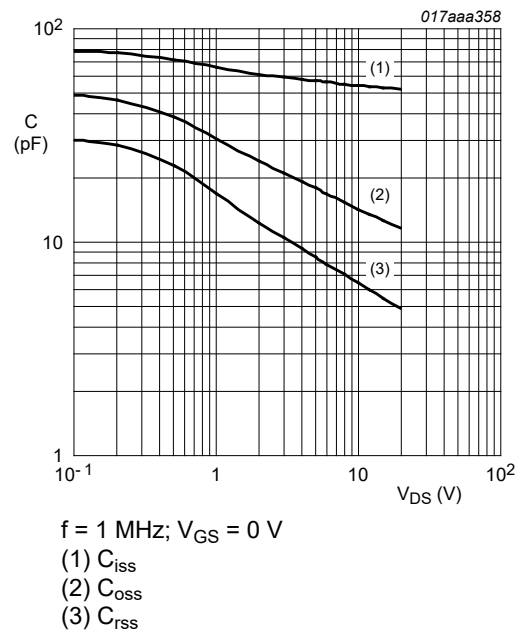
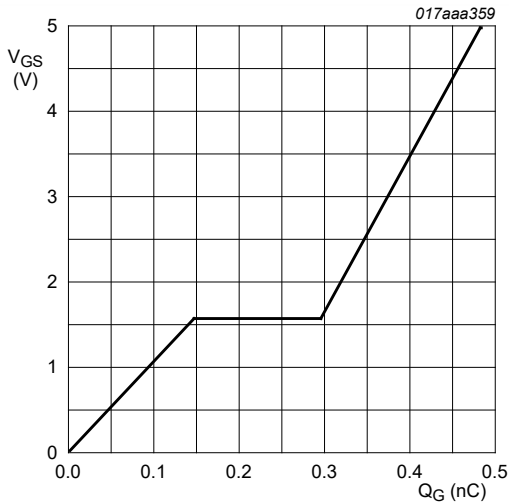


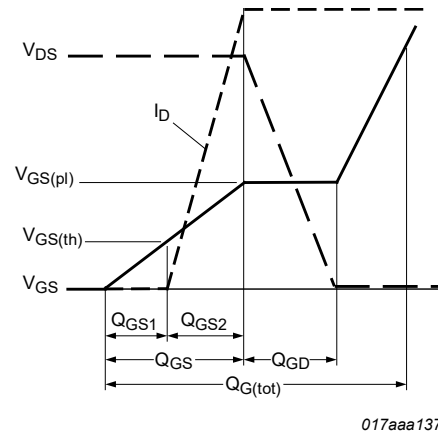
Fig. 13. Input, output and reverse transfer capacitances as a function of drain-source voltage; typical values



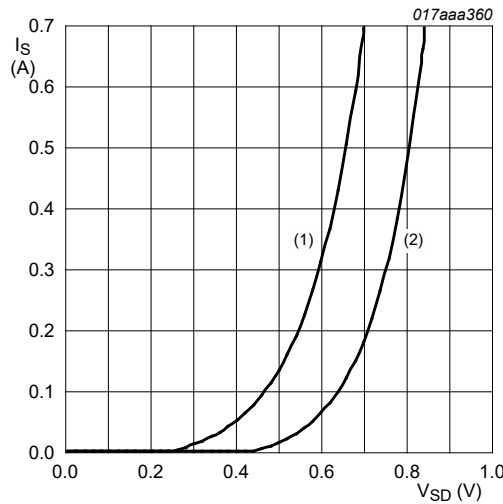


$I_D = 0.5 \text{ A}; V_{DS} = 10 \text{ V}; T_{amb} = 25 \text{ }^\circ\text{C}$

**Fig. 14. Gate-source voltage as a function of gate charge; typical values**



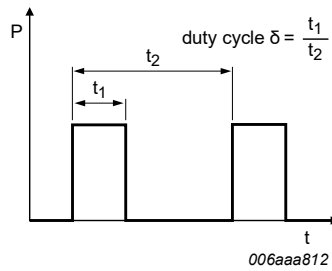
**Fig. 15. Gate charge waveform definitions**



$V_{GS} = 0 \text{ V}$   
 (1)  $T_j = 150 \text{ }^\circ\text{C}$   
 (2)  $T_j = 25 \text{ }^\circ\text{C}$

**Fig. 16. Source current as a function of source-drain voltage; typical values**

## 11. Test information



**Fig. 17. Duty cycle definition**

## 12. Package outline

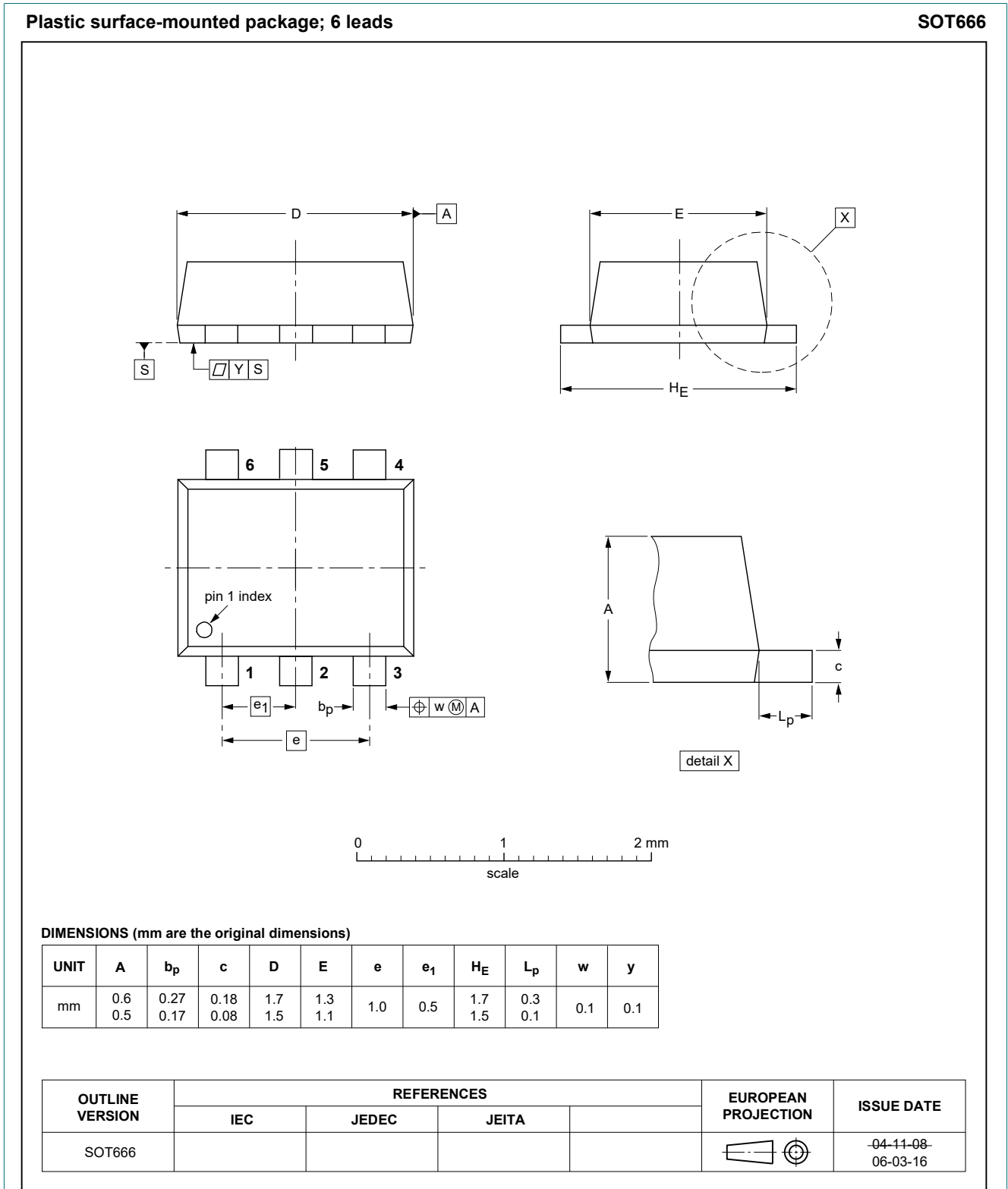


Fig. 18. Package outline SOT666

### 13. Soldering

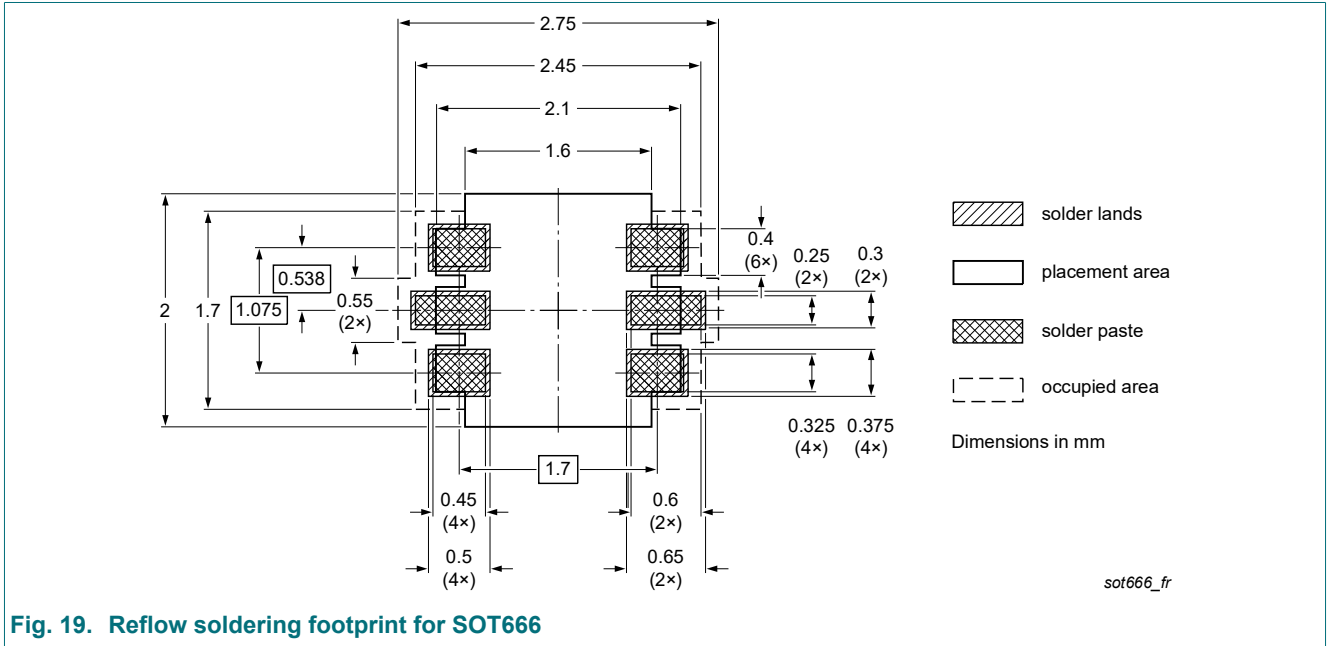


Fig. 19. Reflow soldering footprint for SOT666

## 14. Revision history

Table 8. Revision history

Data sheet ID	Release date	Data sheet status	Change notice	Supersedes
PMDT290UNE v.2	20221228	Product data sheet	-	PMDT290UNE v.1
Modifications:	<ul style="list-style-type: none"><li>• The format of this data sheet has been redesigned to comply with the identity guidelines of Nexperia</li><li>• Legal texts have been adapted to the new company name where appropriate</li><li>• Product changed to non-automotive qualification</li></ul>			
PMDT290UNE v.1	20110913	Product data sheet	-	-

## 15. Legal information

### Data sheet status

Document status [1][2]	Product status [3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

- [1] Please consult the most recently issued document before initiating or completing a design.
- [2] The term 'short data sheet' is explained in section "Definitions".
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## Contents

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1. General description.....	1
2. Features and benefits.....	1
3. Applications.....	1
4. Quick reference data.....	1
5. Pinning information.....	2
6. Ordering information.....	2
7. Marking.....	2
8. Limiting values.....	3
9. Thermal characteristics.....	5
10. Characteristics.....	6
11. Test information.....	9
12. Package outline.....	10
13. Soldering.....	11
14. Revision history.....	12
15. Legal information.....	13

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