

# 74F125

## Quad buffers; 3-State

Rev. 4 — 23 January 2013

Product data sheet

### 1. General description

The 74F125 provides four non-inverting buffer/line drivers with 3-state outputs. The 3-state outputs ( $nY$ ) are controlled by the output enable input ( $n\overline{OE}$ ). A HIGH at  $n\overline{OE}$  causes the outputs to assume a high-impedance OFF-state.

### 2. Features and benefits

- High impedance NPN base inputs for reduced loading (20  $\mu$ A in HIGH and LOW states)

### 3. Ordering information

Table 1. Ordering information

Type number	Package			
	Temperature range	Name	Description	Version
N74F125N	0 °C to +70 °C	DIP14	plastic dual in-line package; 14 leads (300 mil)	SOT27-1
N74F125D	0 °C to +70 °C	SO14	plastic small outline package; 14 leads; body width 3.9 mm	SOT108-1



## 4. Functional diagram

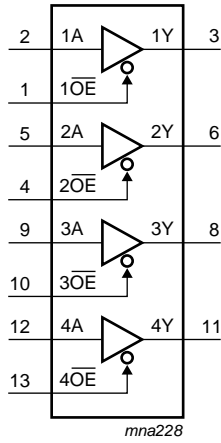


Fig 1. Logic symbol

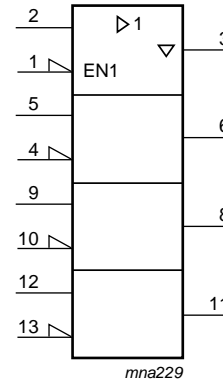


Fig 2. IEC logic symbol

## 5. Pinning information

### 5.1 Pinning

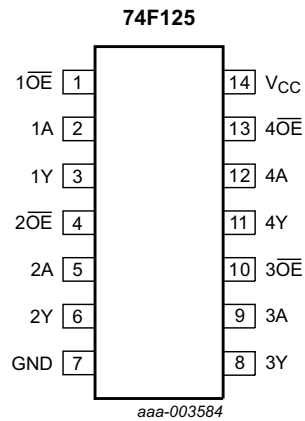


Fig 3. Pin configuration DIP14 and SO14 package

## 5.2 Pin description

**Table 2.** Pin description

Symbol	Pin	Description	Unit load HIGH/LOW	Load value <sup>[1]</sup> HIGH/LOW
$\overline{1OE}$ to $\overline{4OE}$	1, 4, 10, 13	output enable input (active LOW)	1.0/0.033	20 $\mu$ A/20 $\mu$ A
1A to 4A	2, 5, 9, 12	data input	1.0/0.033	20 $\mu$ A/20 $\mu$ A
1Y to 4Y	3, 6, 8, 11	data output	750/106.7	15 mA/64 mA
GND	7	ground (0 V)	-	-
V <sub>CC</sub>	14	supply voltage	-	-

[1] One FAST Unit Load (UL) is defined as 20  $\mu$ A in HIGH state, 0.6  $\mu$ A in LOW state.

## 6. Functional description

**Table 3.** Function table<sup>[1]</sup>

Control	Input	Output
$\overline{nOE}$	nA	nY
L	L	L
	H	H
H	X	Z

[1] H = HIGH voltage level; L = LOW voltage level; X = don't care; Z = high-impedance OFF-state.

## 7. Limiting values

**Table 4.** Limiting values

*In accordance with the Absolute Maximum Rating System (IEC 60134).*

Symbol	Parameter	Conditions	Min	Max	Unit
V <sub>CC</sub>	supply voltage		-0.5	+7.0	V
V <sub>I</sub>	input voltage		<sup>[1]</sup> -0.5	+7.0	V
V <sub>O</sub>	output voltage	output in HIGH-state	<sup>[1]</sup> -0.5	V <sub>CC</sub>	V
I <sub>IK</sub>	input clamping current	V <sub>I</sub> < 0 V	-30	+5	mA
I <sub>O</sub>	output current	output in LOW-state	-	128	mA
T <sub>amb</sub>	ambient temperature	in free air	<sup>[2]</sup> 0	70	°C
T <sub>stg</sub>	storage temperature		-65	+150	°C

[1] The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

[2] The performance capability of a high-performance integrated circuit in conjunction with its thermal environment can create junction temperatures which are detrimental to reliability. The maximum junction temperature of this integrated circuit should not exceed 150 °C.

## 8. Recommended operating conditions

**Table 5. Recommended operating conditions**

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$V_{CC}$	supply voltage		4.5	5.0	5.5	V
$V_{IH}$	HIGH-level input voltage		2.0	-	-	V
$V_{IL}$	LOW-level input voltage		-	-	0.8	V
$I_{IK}$	input clamping current		-18	-	-	mA
$I_{OH}$	HIGH-level output current		-15	-	-	mA
$I_{OL}$	LOW-level output current		-	-	64	mA
$T_{amb}$	ambient temperature		0		70	°C

## 9. Static characteristics

**Table 6. Static characteristics**

Symbol	Parameter	Conditions	25 °C			0 °C to +70 °C		Unit	
			Min	Typ <sup>[1]</sup>	Max	Min	Max		
$V_{IK}$	input clamping voltage	$V_{CC} = 4.5 \text{ V}; I_{IK} = -18 \text{ mA}$	-1.2	-0.73	-	-1.2	-	V	
$V_{OH}$	HIGH-level output voltage	$V_{CC} = 4.5 \text{ V}; V_{IL} = 0.8 \text{ V}; V_{IH} = 2.0 \text{ V}$ $I_{OH} = -3 \text{ mA}$	-	-	-	2.4	-	V	
		$V_{CC} = \pm 10 \%$	-	-	-	2.7	-	V	
		$V_{CC} = \pm 5 \%$	-	3.3	-	-	-	V	
		$I_{OH} = -15 \text{ mA}$ $V_{CC} = \pm 10 \%$	-	-	-	2.0	-	V	
$V_{OL}$	LOW-level output voltage	$V_{CC} = 4.5 \text{ V}; V_{IL} = 0.8 \text{ V}; V_{IH} = 2.0 \text{ V}$ $I_{OL} = 64 \text{ mA}$	-	-	-	-	0.55	V	
		$V_{CC} = \pm 10 \%$	-	-	-	-	0.55	V	
		$V_{CC} = \pm 5 \%$	-	0.42	-	-	-	V	
$I_I$	input leakage current	$V_{CC} = 0 \text{ V}; V_I = 7.0 \text{ V}$	-	-	-	-	100	μA	
$I_{IH}$	HIGH-level input current	$V_{CC} = 5.5 \text{ V}; V_I = 2.7 \text{ V}$	-	-	-	-	20	μA	
$I_{IL}$	LOW-level input current	$V_{CC} = 5.5 \text{ V}; V_I = 0.5 \text{ V}$	-	-	-	-20	-	μA	
$I_{OZ}$	OFF-state output current	$V_{CC} = 5.5 \text{ V}$	-	-	-	-	50	μA	
		$V_O = 2.7 \text{ V}$	-	-	-	-	50	μA	
		$V_O = 0.5 \text{ V}$	-	-	-	-50	-	μA	
$I_O$	output current	$V_{CC} = 5.5 \text{ V}$	<sup>[2]</sup>	-	-	-	-225	-100	mA
$I_{CC}$	supply current	$V_{CC} = 5.5 \text{ V}; V_I = \text{GND or } V_{CC}$	-	-	-	-	-	-	mA
		outputs HIGH-state	-	17	-	-	-	24	mA
		outputs LOW-state	-	28	-	-	-	40	mA
		outputs OFF-state	-	25	-	-	-	35	mA

[1] All typical values are measured at  $V_{CC} = 5 \text{ V}$ .

[2] No more than one output should be tested at a time, and the duration of the test should not exceed one second.

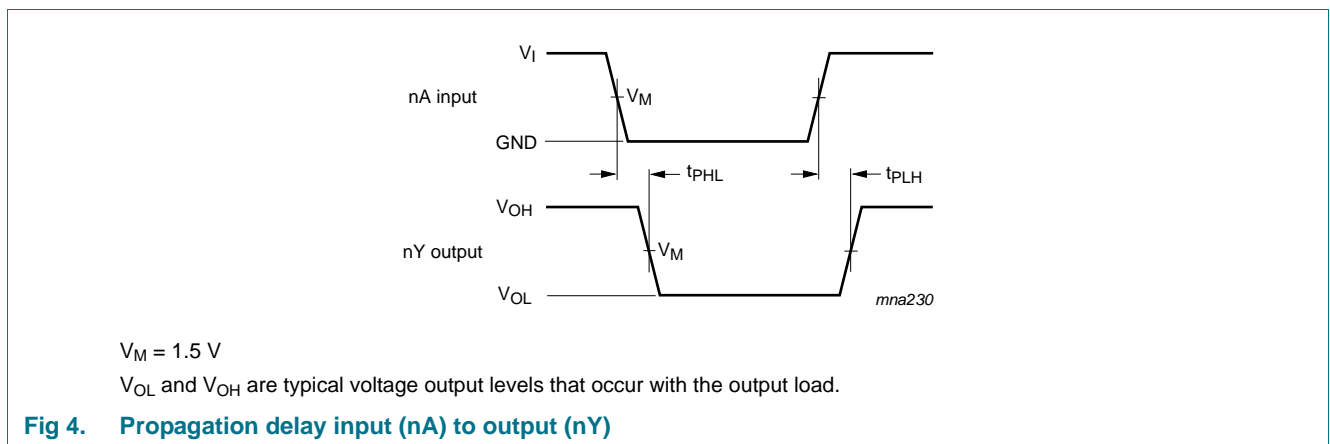
10. Dynamic characteristics

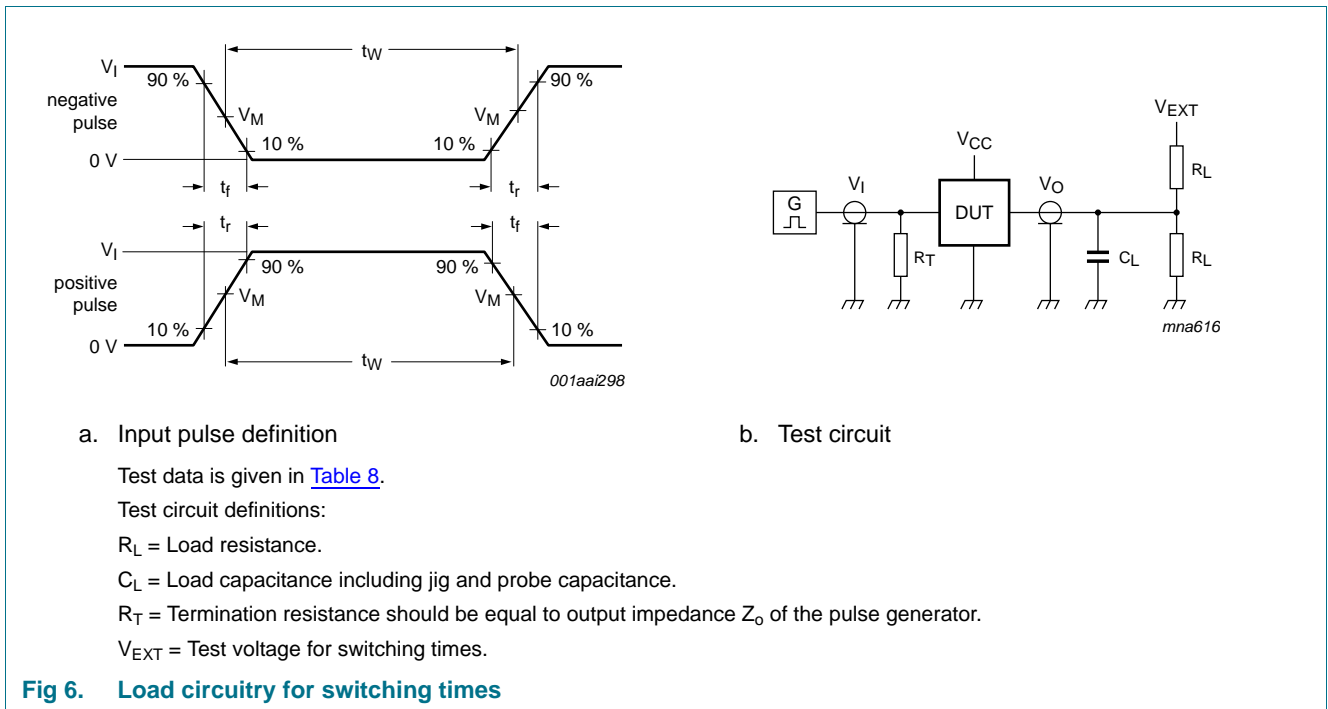
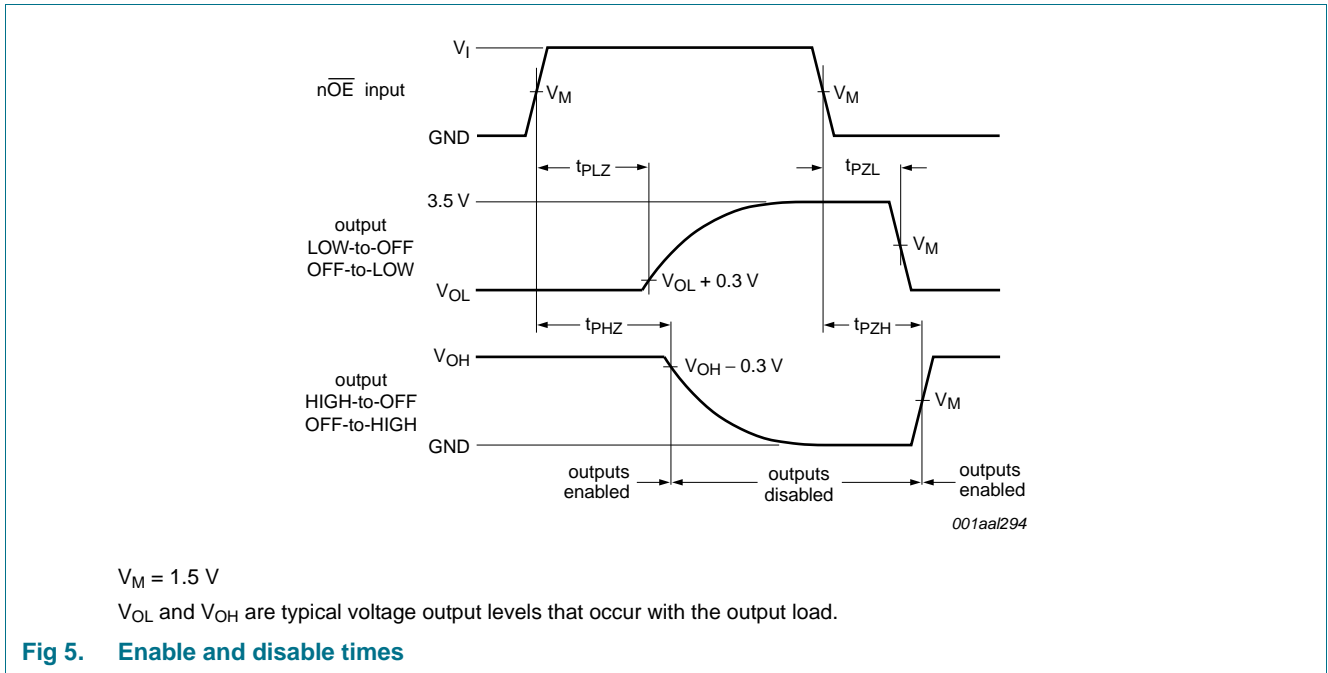
Table 7. Dynamic characteristics

GND = 0 V. Test circuit is shown in Figure 6.

Symbol	Parameter	Conditions	25 °C; V <sub>CC</sub> = 5.0 V			0 °C to +70 °C; V <sub>CC</sub> = 5.0 V ± 0.5 V		Unit
			Min	Typ	Max	Min	Max	
t <sub>PLH</sub>	LOW to HIGH propagation delay	nA to nY; see <a href="#">Figure 4</a>	2.0	4.0	6.0	2.0	6.5	ns
t <sub>PHL</sub>	HIGH to LOW propagation delay	nA to nY; see <a href="#">Figure 4</a>	3.0	5.5	7.5	3.0	8.0	ns
t <sub>PZH</sub>	OFF-state to HIGH propagation delay	n $\overline{\text{OE}}$ to nY; see <a href="#">Figure 5</a>	3.5	5.5	7.5	3.5	8.5	ns
t <sub>PZL</sub>	OFF-state to LOW propagation delay	n $\overline{\text{OE}}$ to nY; see <a href="#">Figure 5</a>	4.0	6.0	8.0	4.0	9.0	ns
t <sub>PHZ</sub>	HIGH to OFF-state propagation delay	n $\overline{\text{OE}}$ to nY; see <a href="#">Figure 5</a>	1.5	3.5	5.0	1.5	6.0	ns
t <sub>PLZ</sub>	LOW to OFF-state propagation delay	n $\overline{\text{OE}}$ to nY; see <a href="#">Figure 5</a>	1.5	3.5	5.5	1.5	6.0	ns

11. Waveforms





**Table 8. Test data**

Input				Load		$V_{EXT}$		
$V_I$	$f_i$	$t_w$	$t_r, t_f$	$C_L$	$R_L$	$t_{PHL}, t_{PLH}$	$t_{PZH}, t_{PHZ}$	$t_{PZL}, t_{PLZ}$
3.0 V	1 MHz	500 ns	$\leq 2.5\text{ ns}$	50 pF	500 $\Omega$	open	open	7.0 V

12. Package outline

DIP14: plastic dual in-line package; 14 leads (300 mil)

SOT27-1

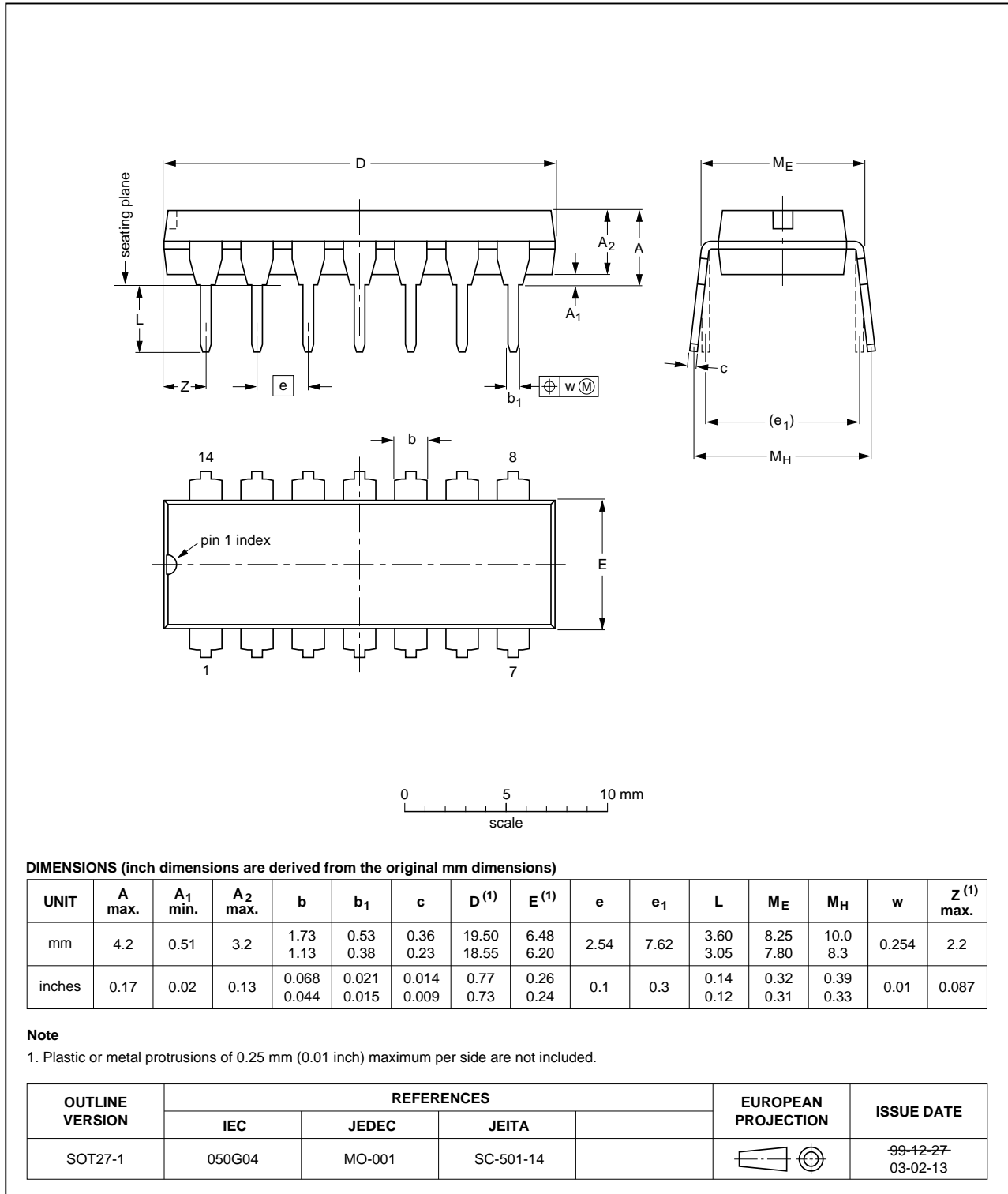


Fig 7. Package outline SOT27-1 (DIP14)

SO14: plastic small outline package; 14 leads; body width 3.9 mm

SOT108-1

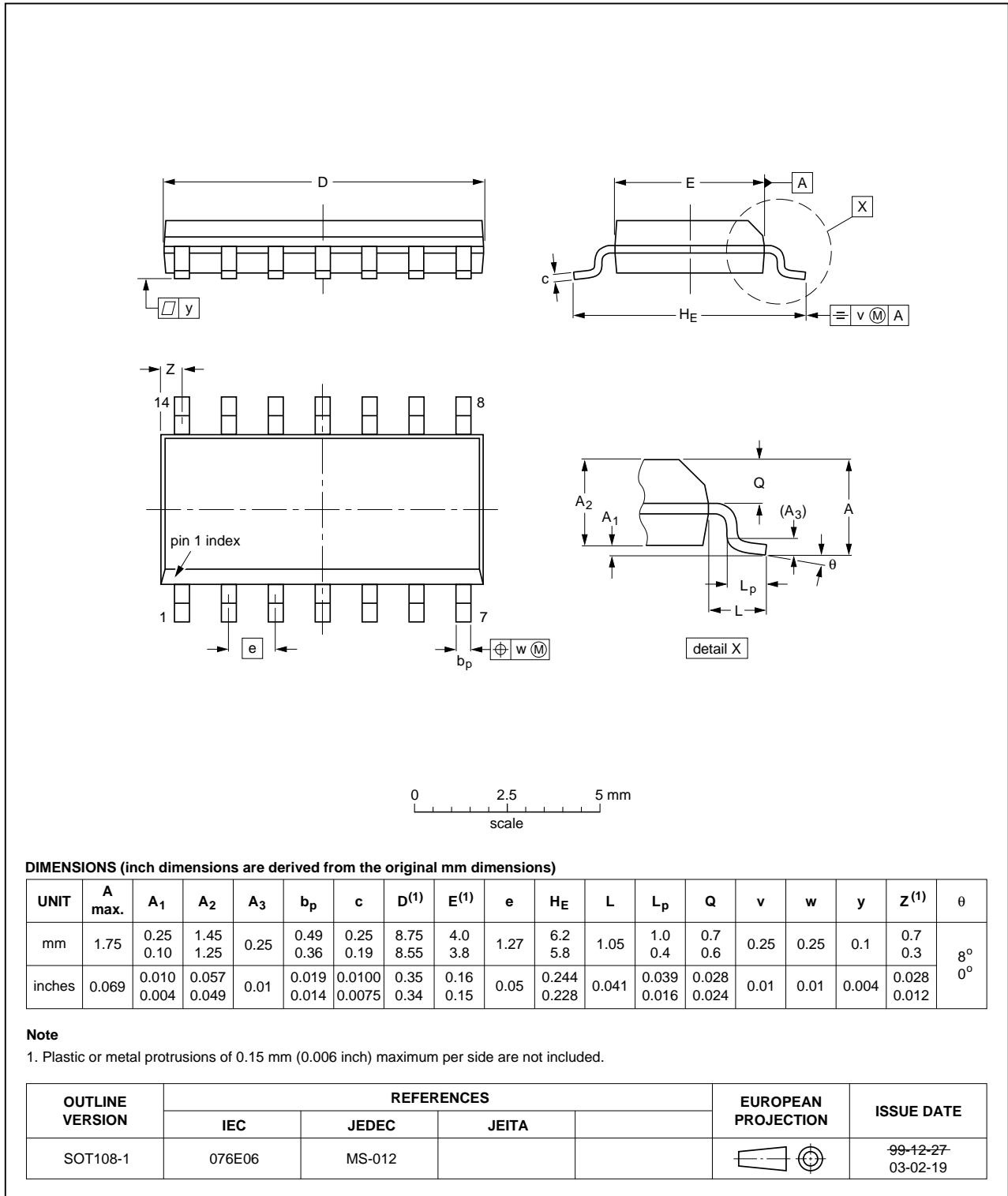


Fig 8. Package outline SOT108-1 (SO14)



## 13. Abbreviations

Table 9. Abbreviations

Acronym	Description
CMOS	Complementary Metal Oxide Semiconductor
LSTTL	Low-power Schottky Transistor-Transistor Logic
ESD	ElectroStatic Discharge
HBM	Human Body Model
MM	Machine Model
CDM	Charge-Device Model
TTL	Transistor-Transistor Logic

## 14. Revision history

Table 10. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
74F125 v.4	20130123	Product data sheet	-	74F125 v.3
Modifications:	<ul style="list-style-type: none"> <li>• Features and benefits: Changed mA into <math>\mu</math>A (errata).</li> </ul>			
74F125 v.3	20130118	Product data sheet	-	74F125 v.2
Modifications:	<ul style="list-style-type: none"> <li>• The format of this data sheet has been redesigned to comply with the new identity guidelines of NXP Semiconductors.</li> <li>• Legal texts have been adapted to the new company name where appropriate.</li> </ul>			
74F125 v.2	19890328	Product data sheet	-	74F125 v.1

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