19-1674; Rev 0; 4/00

MAXIM

32-Channel Sample/Hold Amplifier with a Single Multiplexed Input

General Description

The MAX5168 contains 32 sample/hold amplifiers and four 1-of-8 multiplexers. The logic controlling the muxes and sample/hold amplifiers combines the four muxes into a unified 1-of-32 multiplexer with a sample/hold at each output. Additional logic allows two devices to function as a single 64-channel unit. The MAX5168 is available with an output impedance of 50Ω, 500Ω, or 1kΩ.

The MAX5168 operates with +10V and -5V supplies, and a separate +5V digital logic supply. Manufactured with a proprietary BiCMOS process, it provides high accuracy, fast acquisition time, a low droop rate, and a low hold step. The MAX5168 has a typical linearity error of less than 0.01% and can accurately acquire 8V step input signals to 0.01% accuracy in 2.5µs within the +7V to -4V input signal range. Transitions from sample mode to hold mode result in only a 0.5mV error. While in hold mode, the output voltage slowly droops at a rate of 1mV/s.

The MAX5168 is available in a 48-pin TQFP package and is specified for both the commercial (0°C to +70°C) and extended industrial (-40°C to +85°C) temperature ranges.

Features

- **32-Channel Sample/Hold**
- **0.01% Accuracy of Acquired Signal**
- **0.01% Linearity Error**
- **Fast Acquisition Time: 2.5µs**
- **Low Droop Rate: 1mV/s**
- **Low Hold Step: 0.25mV**
- **Wide Output Voltage Range: +7V to -4V**

Ordering Information

PART	TEMP. RANGE	PIN-PACKAGE	R_{OUT} (Ω)
MAX5168LCCM	0°C to +70°C	48 TQFP	50
MAX5168MCCM	0°C to +70°C	48 TQFP	500
MAX5168NCCM	0°C to +70°C	48 TQFP	1k
MAX5168LECM	-40°C to +85°C	48 TQFP	50
MAX5168MECM	-40°C to +85°C	48 TQFP	500
MAX5168NECM	-40°C to +85°C	48 TQFP	1k

Applications

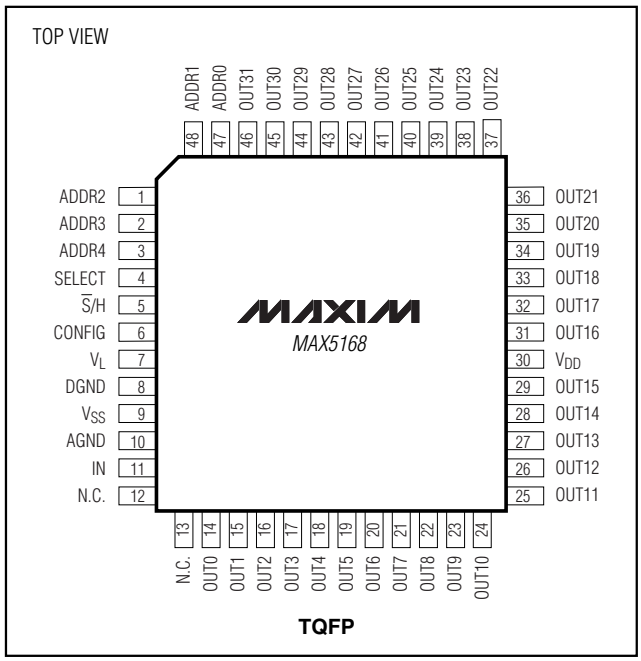
Automatic Test Systems (ATE)

Industrial Process Controls

Arbitrary Function Generators

Avionics Equipment

Pin Configuration



32-Channel Sample/Hold Amplifier with a Single Multiplexed Input

ABSOLUTE MAXIMUM RATINGS

V_{DD} to AGND .....-0.3V to +11.0V
V_{SS} to AGND .....-6.0V to +0.3V
V_{DD} to V_{SS} .....+15.75V
V_L to DGND .....-0.3V to +6.0V
V_L to AGND .....-0.3V to +6.0V
DGND to AGND.....-0.3V to +2.0V
IN, OUT_ .....V_{SS} to V_{DD}
Logic Inputs to DGND .....-0.3V to +6.0V
Maximum Current into OUT_ .....±10mA
Maximum Current into Logic Inputs .....±20mA
Continuous Power Dissipation (T_A = +70°C)
48-Pin TQFP (derate 12.5mW/°C above +70°C).....1000mW
Operating Temperature Ranges
MAX5168_CCM .....0°C to +70°C
MAX5168_ECM.....-40°C to +85°C
Storage Temperature Range .....-65°C to +150°C
Lead Temperature (soldering, 10s) .....+300°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

(V_{DD} = +10.0V, V_{SS} = -5.0V, V_L = +5.0V ±5%, AGND = DGND = 0, R_L = 5kΩ, C_L = 50pF, T_A = T_{MIN} to T_{MAX}, unless otherwise noted. Typical values are at T_A = +25°C.)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
ANALOG SECTION							
Linearity Error		-4.0V < V_{IN} < +7V, R_L = ∞			0.01	0.08	%
Hold Step	V_{HS}	IN = AGND			0.25	1.00	mV
Droop Rate		IN = AGND, T_A = +25°C			1	40	mV/s
Offset Voltage	V_{OS}	IN = AGND, T_A = +25°C		-30	-5	+30	mV
		+15°C ≤ T_A ≤ +65°C (Note 1)			20	40	µV/°C
Output Voltage Range	$V_{OUT\_}$	R_L = ∞		V_{SS} + 0.75		V_{DD} - 2.4	V
Analog Crosstalk		8V step with 500ns rising edge (Note 1)	C_L = 250pF for MAX5168L	-72	-76		dB
			C_L = 10nF for MAX5168M/N	-72	-76		
Input Capacitance	C_{IN}	(Note 1)			10	20	pF
DC Output Impedance	$R_{OUT\_}$	R_L = ∞, C_L = 250pF	MAX5168L	35	50	65	Ω
			MAX5168M	350	500	650	
			MAX5168N	700	1000	1300	
Output Source Current	I_{SOURCE}	V_{IN} = 0, sample mode		2			mA
Output Sink Current	I_{SINK}	V_{IN} = 0, sample mode		2			mA
Output Clamp High	V_{CH}			V_{SS}		V_{DD}	V
TIMING PERFORMANCE							
Acquisition Time	t_{AQ}	T_A = +25°C, R_L = ∞, Figure 2	8V step to 0.08%		2.5	4	µs
			100mV step to ±1mV		1		
Hold-Mode Settling Time	t_H	To ±1mV of final value, Figure 2 (Note 1)			1	2	µs
Aperture Delay	t_{AP}	Figure 2 (Note 1)				200	ns

ELECTRICAL CHARACTERISTICS (continued)

(V_{DD} = +10.0V, V_{SS} = -5.0V, V_L = +5.0V ±5%, AGND = DGND = 0, R_L = 5kΩ, C_L = 50pF, T_A = T_{MIN} to T_{MAX}, unless otherwise noted. Typical values are at T_A = +25°C.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
$\overline{S}$/H Pulse Width	t_{PW}	Figure 2 (Note 1)	200			ns
Data Setup Time	t_{SET}	Figure 2 (Note 1)	50			ns
Data Hold Time	t_{DH}	Figure 2 (Note 1)	150			ns
DIGITAL INPUTS						
Input Voltage High	V_{IH}		2.0			V
Input Voltage Low	V_{IL}				0.8	V
Input Current	I_I	IN = DGND or V_{CC}	-1		+1	µA
POWER SUPPLIES						
Positive Analog Supply	V_{DD}	(Note 2)	9.5	10	10.5	V
Negative Analog Supply	V_{SS}	(Note 2)	-4.75	-5	-5.45	V
Digital Logic Supply	V_L		4.75	5	5.25	V
Positive Analog Supply Current	I_{DD}	R_L = ∞			36	mA
Negative Analog Supply Current	I_{SS}	R_L = ∞			36	mA
Digital Logic Supply Current	I_L	ADDR_ = DGND or V_L, $\overline{S}$/H = DGND or V_L			0.5	mA
		ADDR_ = 0.8V or 2.0V, $\overline{S}$/H = 0.8V or 2.0V			5	mA
Power-Supply Rejection Ratio	PSRR	For V_{DD} and V_{SS}, sample mode, IN = AGND	-60	-75		dB

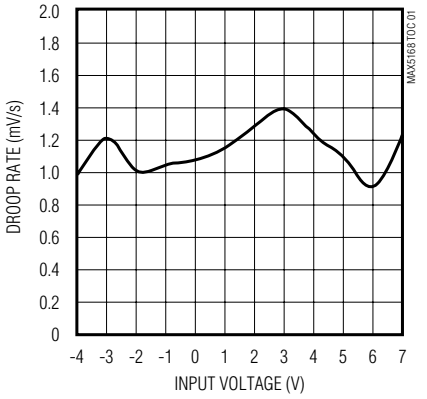
Note 1: Guaranteed by design.
Note 2: Do not exceed the absolute maximum rating for V_{DD} to V_{SS} of +15.75V (see *Absolute Maximum Ratings*).

32-Channel Sample/Hold Amplifier with a Single Multiplexed Input

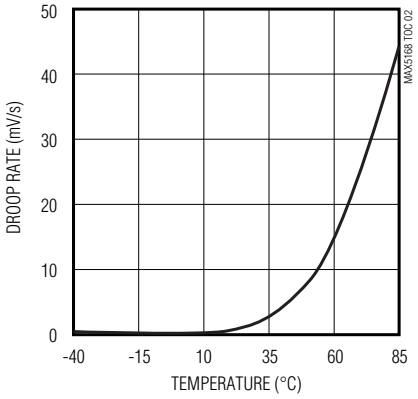
Typical Operating Characteristics

(V_{DD} = +10V, V_{SS} = -5V, V_L = +5V, V_{IN} = +5V, R_L = ∞, C_L = 0, AGND = DGND = 0, V_{CH} = V_{DD}, V_{CL} = V_{SS}, T_A = +25°C, unless otherwise noted.)

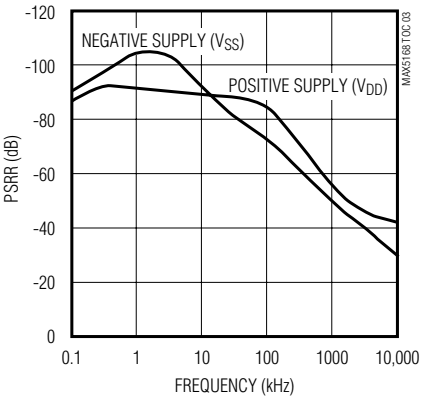
DROOP RATE vs. INPUT VOLTAGE



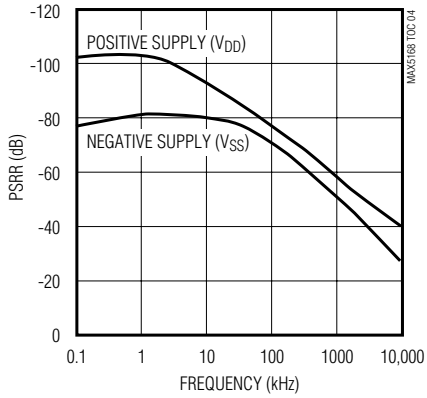
DROOP RATE vs. TEMPERATURE



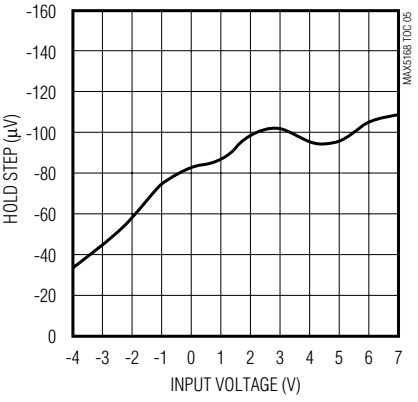
POWER-SUPPLY REJECTION RATIO SAMPLE MODE



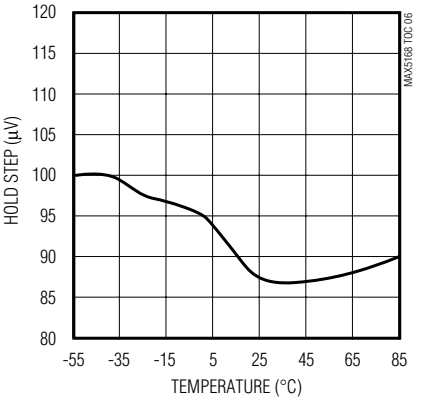
POWER-SUPPLY REJECTION RATIO HOLD MODE



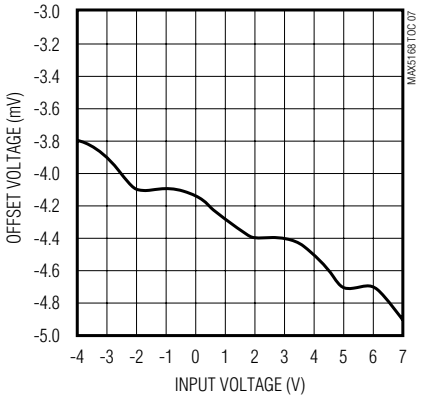
HOLD STEP vs. INPUT VOLTAGE



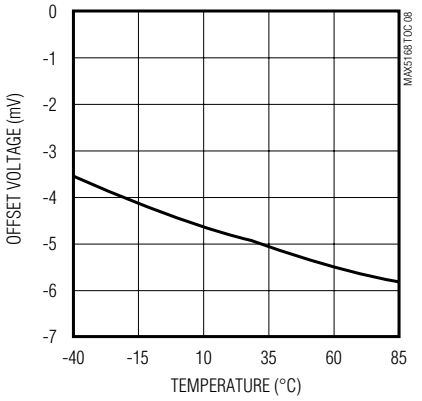
HOLD STEP vs. TEMPERATURE



OFFSET VOLTAGE vs. INPUT VOLTAGE



OFFSET VOLTAGE vs. TEMPERATURE



Pin Description

PIN	NAME	FUNCTION
1	ADDR2	Bit 2 of the Address Decoder
2	ADDR3	Bit 3 of the Address Decoder
3	ADDR4	Bit 4 of the Address Decoder
4	SELECT	Enables the $\overline{S}$/H pin. The polarity of SELECT is determined by the state of the CONFIG pin. If CONFIG is low, then SELECT is active-high. If CONFIG is high, then SELECT is active-low. When SELECT is not in its active state, all 32 channels are in hold mode independent of the $\overline{S}$/H pin.
5	$\overline{S}$/H	Puts the selected channel into sample mode when low. Places all channels into hold mode when high.
6	CONFIG	Sets the polarity of the SELECT pin.
7	V_L	+5V Logic Supply
8	DGND	Digital GND
9	V_{SS}	-5V Analog Supply
10	AGND	Analog GND
11	IN	Input Pin
12, 13	N.C.	No connection. Not internally connected.
14–29	OUT0–OUT15	Outputs 0–15 Pins
30	V_{DD}	+10V Analog Supply
31–46	OUT16–OUT31	Outputs 16–31 Pins
47	ADDR0	Bit 0 of the Address Decoder
48	ADDR1	Bit 1 of the Address Decoder

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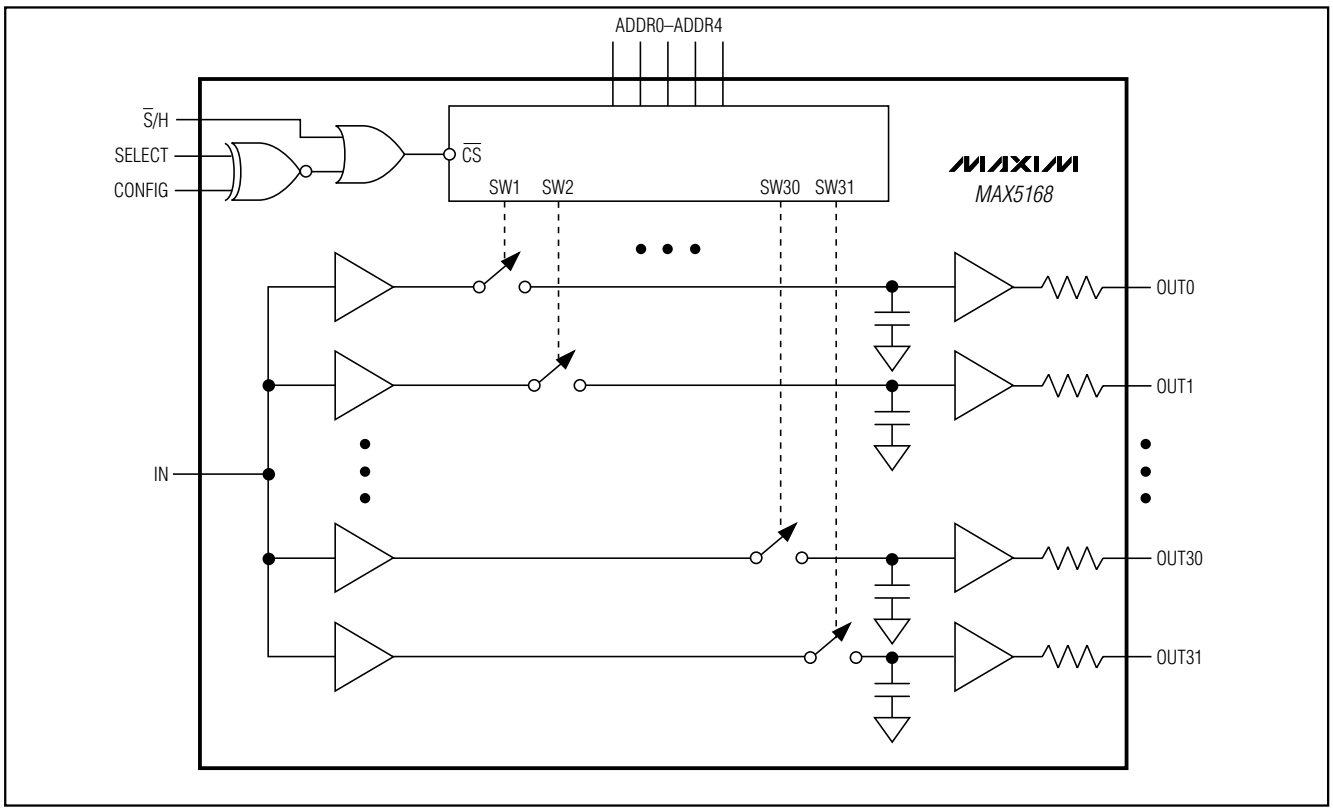


Figure 1. Functional Diagram

Detailed Description

Digital Interface

The MAX5168 has three logic control inputs and five address lines. The address lines are inputs to a demultiplexer that selects one of the 32 outputs in a standard addressing scheme (Table 1). The analog input is connected to the addressed sample/hold when directed by the control logic (Table 2).

The three logic control lines determine the state of the addressed sample/hold. The normal circuit connection for this device is to hardwire CONFIG and SELECT to opposing logic voltages. When SELECT and CONFIG are in opposite states (one high and the other low), the five address lines select one of the sample/holds. Use the $\overline{S}$/H line to place the selected channel into sample or hold mode. The other 31 channels will remain in hold mode.

If an active-high sampling mode is desired, tie $\overline{S}$/H and CONFIG low. In this case, SELECT controls the addressed channel with a high state putting that channel into sample mode.

The SELECT and CONFIG pins allow the design of a virtual 64-channel device using two of the MAX5168s. See the *Applications Information* section for more information about 64-plus output addressing schemes.

Sample/Hold

The MAX5168 contains 32 buffered sample/hold circuits with internal hold capacitors. Internal hold capacitors minimize leakage current, dielectric absorption, feedthrough, and required board space. The value of the hold capacitor affects acquisition time and droop rate. Smaller capacitance allows faster acquisition times but increases the droop rate. Larger values increase hold acquisition time. The hold capacitor used in the MAX5168 provides fast 2.5µs (typ) acquisition time while maintaining a relatively low 1mV/s (typ) droop rate, making the sample/hold ideal for high-speed sampling.

Sample Mode

When SELECT and CONFIG are in opposing logic states, the $\overline{S}$/H line controls the mode of operation. Sample mode is entered when $\overline{S}$/H is low. During sample mode, the

Table 1. Channel/Output Selection

ADDR4	ADDR3	ADDR2	ADDR1	ADDR0	OUTPUT	
0	0	0	0	0	VOUT0	SELECTED
0	0	0	0	1	VOUT1	SELECTED
0	0	0	1	0	VOUT2	SELECTED
0	0	0	1	1	VOUT3	SELECTED
0	0	1	0	0	VOUT4	SELECTED
0	0	1	0	1	VOUT5	SELECTED
0	0	1	1	0	VOUT6	SELECTED
0	0	1	1	1	VOUT7	SELECTED
0	1	0	0	0	VOUT8	SELECTED
0	1	0	0	1	VOUT9	SELECTED
0	1	0	1	0	VOUT10	SELECTED
0	1	0	1	1	VOUT11	SELECTED
0	1	1	0	0	VOUT12	SELECTED
0	1	1	0	1	VOUT13	SELECTED
0	1	1	1	0	VOUT14	SELECTED
0	1	1	1	1	VOUT15	SELECTED
1	0	0	0	0	VOUT16	SELECTED
1	0	0	0	1	VOUT17	SELECTED
1	0	0	1	0	VOUT18	SELECTED
1	0	0	1	1	VOUT19	SELECTED
1	0	1	0	0	VOUT20	SELECTED
1	0	1	0	1	VOUT21	SELECTED
1	0	1	1	0	VOUT22	SELECTED
1	0	1	1	1	VOUT23	SELECTED
1	1	0	0	0	VOUT24	SELECTED
1	1	0	0	1	VOUT25	SELECTED
1	1	0	1	0	VOUT26	SELECTED
1	1	0	1	1	VOUT27	SELECTED
1	1	1	0	0	VOUT28	SELECTED
1	1	1	0	1	VOUT29	SELECTED
1	1	1	1	0	VOUT30	SELECTED
1	1	1	1	1	VOUT31	SELECTED

Table 2. Logic Table for CONFIG, SELECT, and $\overline{S}$/H

$\overline{S}$/H (SAMPLE/HOLD)	CONFIG	SELECT	CHANNEL FUNCTION
0	0	0	Hold
0	0	1	Sampling
0	1	0	Sampling
0	1	1	Hold
1	X	X	Hold

X = Don't care.

32-Channel Sample/Hold Amplifier with a Single Multiplexed Input

selected multiplexer channel connects to IN, allowing the hold capacitor to acquire the input signal. To guarantee an accurate sample, maintain sample mode for at least 4µs. The output of the sample/hold amplifier tracks the input after 4µs. Only the addressed channel on the selected multiplexer samples the input; all other channels remain in hold mode.

Hold Mode

No matter what the condition of the other control lines, $\overline{S}$/H = high places the MAX5168 into an all-channel hold mode. Hold mode disables the multiplexer and disconnects all 32 sample/holds from the input. When a channel is disconnected, the hold capacitor maintains the sampled voltage at the output with a 1mV/s typical droop rate (towards V_{DD}).

Hold Step

When switching between sample mode and hold mode, the voltage of the hold capacitor changes due to charge injection from stray capacitance. This voltage change, called a hold step, is minimized by limiting the amount of stray capacitance seen by the hold capacitor. The MAX5168 limits the hold step to 0.25mV (typ). An output capacitor to ground can be used to filter out this small hold-step error.

Output

The MAX5168 contains an output buffer for each multiplexer channel (32 total), so the hold capacitor sees a high-impedance input that reduces the droop rate. The capacitor droops at 1mV/s (typ) while in hold mode. The buffer also provides a low output impedance; however, the device contains output resistors in series with the buffer output (Figure 1) for selected output filtering. To provide greater design flexibility, the MAX5168 is available with an output impedance of 50Ω, 500Ω, or 1kΩ.

Output loads increase the analog supply current (I_{DD} and I_{SS}). Excessive loading of the output(s) drastically increases power dissipation. Do not exceed the maximum power dissipation specified in the *Absolute Maximum Ratings*.

The resistor-divider formed by the output resistor (R_O) and load impedance (R_L) scales the sampled voltage (V_{SAMP}). Determine the output voltage ($V_{OUT\_}$) as follows:

$$\text{Voltage Gain} = A_V = R_L / (R_L + R_O)$$

$$V_{OUT\_} = V_{SAMP} \times A_V$$

The maximum output voltage range depends on the analog supply voltages available and the scaling factor used:

$$(V_{SS} + 0.75V) \times A_V \le V_{OUT\_} \le (V_{DD} - 2.4V) \times A_V$$

when $R_L = \infty$, then $A_V = 1$, and this equation becomes

$$(V_{SS} + 0.75V) \le V_{OUT} \le (V_{DD} - 2.4V)$$

Timing Definitions

Acquisition time (t_{AQ}) is the time the MAX5168 must remain in sample mode for the hold capacitor to acquire an accurate sample. The hold-mode settling time (t_H) is the time necessary for the output voltage to settle to its final value. Aperture delay (t_{AP}) is the time interval required to disconnect the input from the hold capacitor. The hold pulse width (t_{PW}) is the time the MAX5168 must remain in hold mode while the address is changed. Data setup time (t_{DS}) is the time an address must be maintained at the digital input pins before the address becomes valid. Data hold time (t_{DH}) is the time an address must be maintained after the device is placed in hold mode (Figure 2).

Applications Information

Multiplexing a DAC

Figure 3 shows a typical demultiplexer application. Different digital codes are converted by the digital-to-analog converter (DAC) and then stored on 32 different channels of the MAX5168. The 40mV/s (max) droop rate requires refreshing the hold capacitors every 250ms before the voltage droops by 1/2LSB for an 8-bit DAC with a 5V full-scale voltage.

Virtual 64 Output Sample/Hold

Two MAX5168s can be configured to operate as a single 64 output sample/hold. The upper and lower addressed devices are identified by CONFIG's logic level. Connect the CONFIG pin of the upper device low, making its SELECT pin active high. Connect the CONFIG pin of the lower device high to make the SELECT pin active low. Figure 4 shows how to configure the devices.

The devices now use only six address lines and a single $\overline{S}$/H control to decode 64 outputs. Address lines A0–A4 from the control logic connect to ADDR0–ADDR4 on both of the 32-channel devices. The A5 line toggles the SELECT pins of both devices to select the active one. The device that has CONFIG tied high responds to the lower 32 addresses (000000 through 011111). The device that has CONFIG grounded responds to the upper 32 addresses (100000 through 111111).

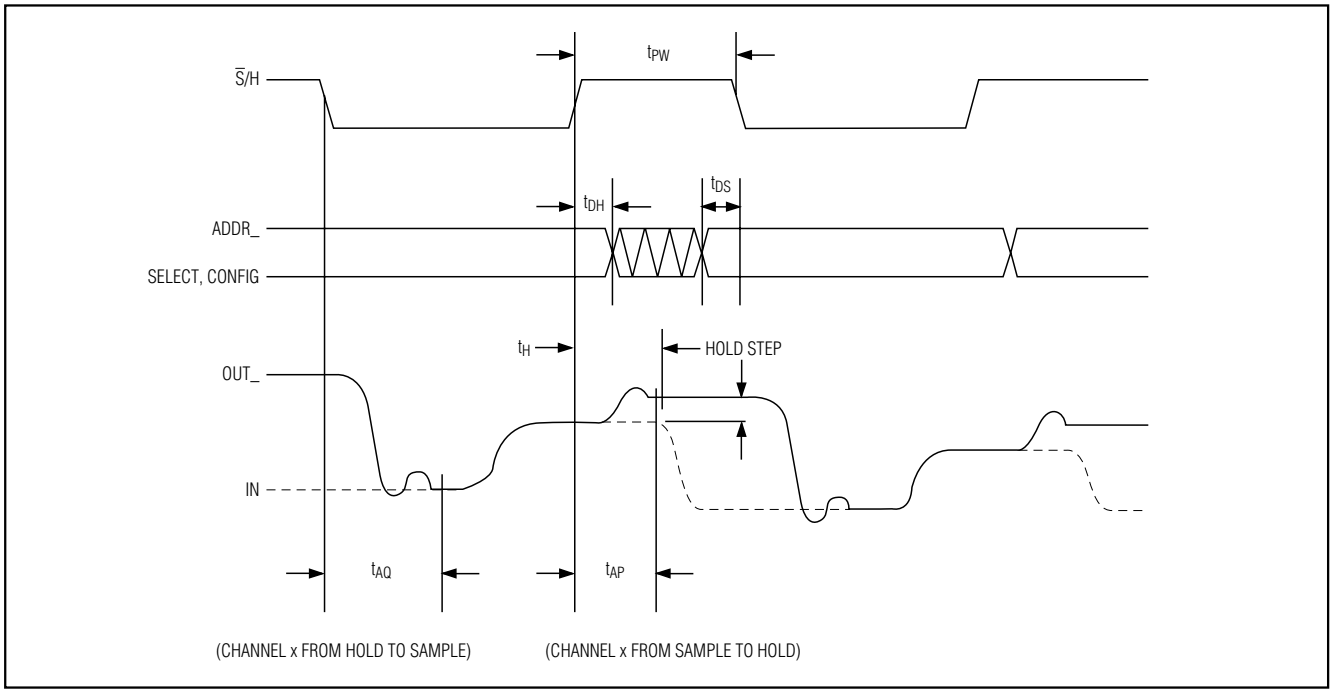


Figure 2. Timing Diagram

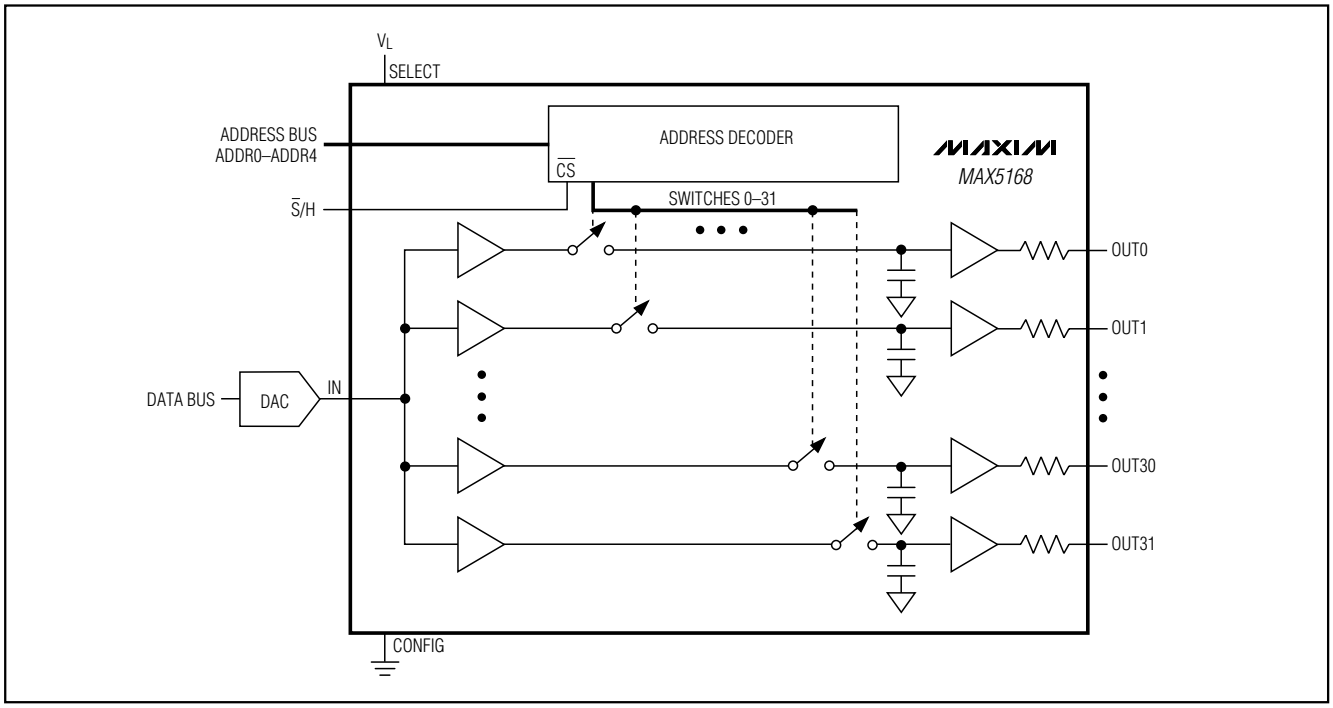


Figure 3. Multiplexing a DAC

32-Channel Sample/Hold Amplifier with a Single Multiplexed Input

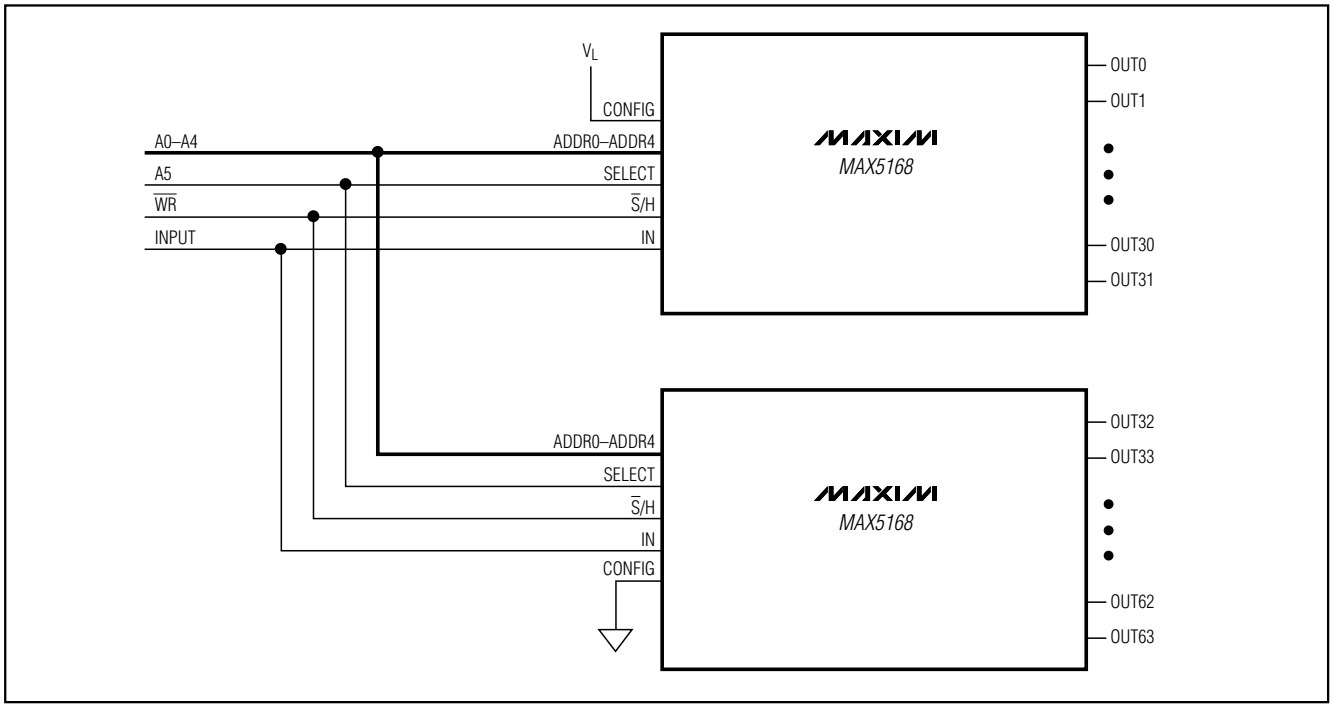


Figure 4. 64-Output Sample/Hold Circuit

Input Drive Requirements

The input of the MAX5168 feeds the inputs of 32 high-impedance buffers. These buffers are what charge the sample/hold capacitor through the multiplexer switch resistance. The bias current of a selected buffer is 10µA, and this feeds into the 10pF input capacitance. Figure 5 shows an equivalent input circuit. The bias currents of the other 31 sample and holds are very small in comparison to the bias current of the selected channel.

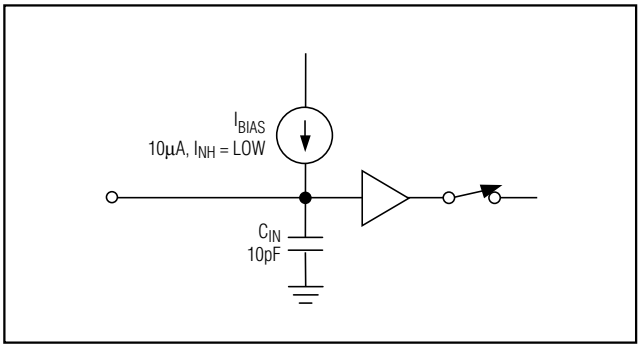


Figure 5. Input Equivalent Circuit

Powering the MAX5168

The MAX5168 does not require a special power-up sequence to avoid latchup. The device requires three separate supply voltages for operation. However, when one or two of the voltages are not available, DC-DC charge-pump (switched-capacitor) converters provide a simple, efficient solution. The MAX860 provides voltage doubling or inversion, ideal for conversions from +5V to +10V or from +5V to -5V.

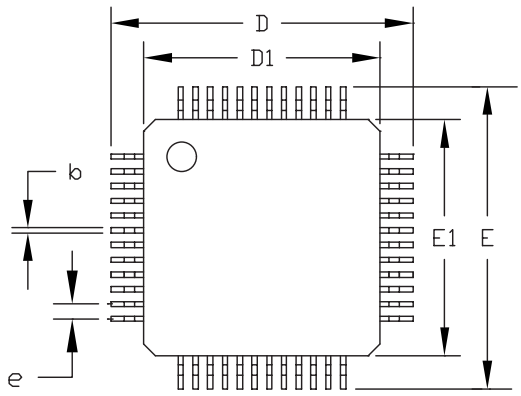
Chip Information

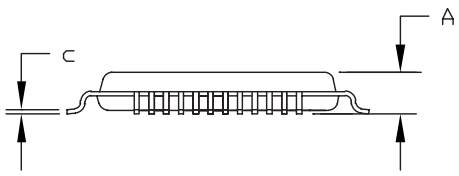
TRANSISTOR COUNT: 6961

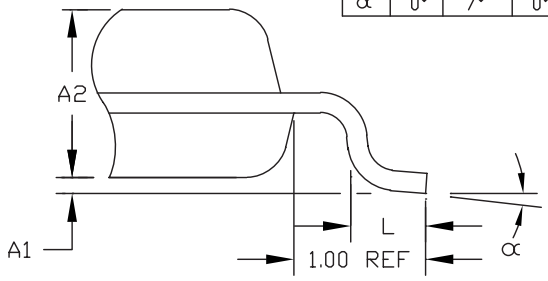
32-Channel Sample/Hold Amplifier with a Single Multiplexed Input

Package Information

32L/48L_TQFP.EPS







JEDEC VARIATION				
	BC		BE	
	32 LEAD		48 LEAD	
	MIN.	MAX.	MIN.	MAX.
A	---	1.60	---	1.60
A_1	0.05	0.15	0.05	0.15
A_2	1.35	1.45	1.35	1.45
D	8.90	9.10	8.90	9.10
D_1	7.00 BSC.		7.00 BSC.	
E	8.90	9.10	8.90	9.10
E_1	7.00 BSC.		7.00 BSC.	
e	0.8 BSC.		0.5 BSC.	
L	0.45	0.75	0.45	0.75
b	0.30	0.45	0.17	0.27
c	0.09	0.20	0.09	0.20
α	0°	7°	0°	7°

NOTES:

1. ALL DIMENSIONING AND TOLERANCING CONFORM TO ANSI Y14.5-1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. THIS OUTLINE CONFORMS TO JEDEC PUBLICATION 95 REGISTRATION MO-136, VARIATIONS BC AND BE.
4. LEADS SHALL BE COPLANAR WITHIN .004 INCH.

MAXIM

PROPRIETARY INFORMATION

TITLE: PACKAGE OUTLINE, 32/48L, 7x7x1.4 MM TQFP

APPROVAL	DOCUMENT CONTROL NO.	REV	
	21-0054	D	1/1

32-Channel Sample/Hold Amplifier with a Single Multiplexed Input

NOTES