Tactical Grade, Six Degrees of Freedom Inertial Sensor

Data Sheet

ADIS16490

FEATURES

- **Triaxial, digital gyroscope, ±100°/sec dynamic range**
  - **±0.05° axis to axis misalignment error**
  - **±0.25° axis to package misalignment error**
  - **1.8°/hr in run bias stability**
  - **0.09°/√hr angular random walk**
- **Triaxial, digital accelerometer, ±8 *g***
  - **3.6 µ*g* in run bias stability**
- **Triaxial, delta angle and delta velocity outputs**
- **Factory calibrated sensitivity, bias, and axial alignment**
  - **Calibration temperature range: −40°C to +85°C**
- **Serial peripheral interface (SPI) compatible**
- **Programmable operation and control**
  - **Automatic and manual bias correction controls**
  - **4 finite impulse response (FIR) filter banks,**
    - **120 configurable taps**
  - **Digital input/output (I/O): data ready, external clock**
  - **Sample clock options: internal, external, or scaled**
  - **On demand self test of inertial sensors**
- **Single-supply operation: 3.0 V to 3.6 V**
- **2000 *g* shock survivability**
- **Operating temperature range: −40°C to +105°C**

APPLICATIONS

- **Precision instrumentation, stabilization**
- **Guidance, navigation, control**
- **Avionics, unmanned vehicles**
- **Precision autonomous machines, robotics**

GENERAL DESCRIPTION

The ADIS16490 is a complete inertial system that includes a triaxis gyroscope and a triaxis accelerometer. Each inertial sensor in the ADIS16490 combines industry leading *i*MEMS® technology with signal conditioning that optimizes dynamic performance. The factory calibration characterizes each sensor for sensitivity, bias, alignment, and linear acceleration (gyroscope bias). As a result, each sensor has its own dynamic compensation formulas that provide accurate sensor measurements.

The ADIS16490 provides a simple, cost effective method for integrating accurate, multiaxis inertial sensing into industrial systems, especially when compared with the complexity and investment associated with discrete designs. All necessary motion testing and calibration are part of the production process at the factory, greatly reducing system integration time. Tight orthogonal alignment simplifies inertial frame alignment in navigation systems. The SPI and register structure provide a simple interface for data collection and configuration control.

The ADIS16490 uses the same footprint and connector system as the ADIS16375, ADIS16480, ADIS16485, and ADIS16488A, which greatly simplifies the upgrade process. The ADIS16490 is packaged in a module that is approximately 47 mm × 44 mm × 14 mm and includes a standard connector interface.

FUNCTIONAL BLOCK DIAGRAM

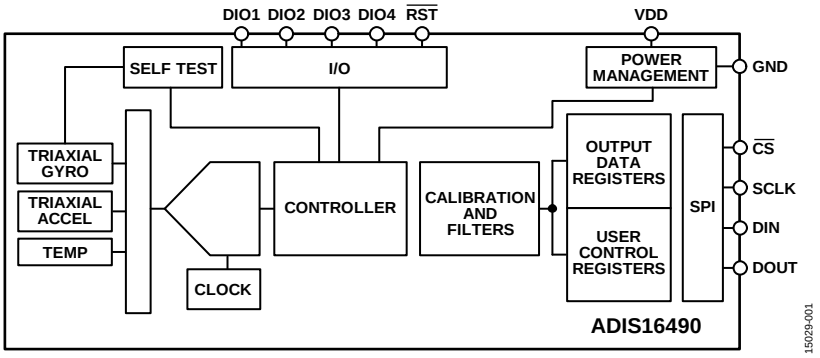

Figure 1.

Document Feedback

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10/2016—Revision 0: Initial Version

SPECIFICATIONS

T_C = 25°C, VDD = 3.3 V, angular rate = 0°/sec, dynamic range = ±100°/sec ± 1 *g*, unless otherwise noted.

Table 1.

Parameter	Test Conditions/Comments	Min	Typ	Max	Unit
GYROSCOPES					
Dynamic Range		±100			°/sec
Sensitivity	x_GYRO_OUT and x_GYRO_LOW (32-bit)		7.6294×10^{-8}		°/sec/LSB
Repeatability[1]	−40°C ≤ T_C ≤ +85°C			0.5	%
Sensitivity Temperature Coefficient	−40°C ≤ T_C ≤ +85°C, 1 σ		±24		ppm/°C
Misalignment	Axis to axis[2]		±0.05		Degrees
	Axis to frame (package)		±0.25		Degrees
Nonlinearity	Best fit straight line, full scale (FS) = 100°/sec		0.3		% FS
Bias					
Repeatability[1, 3]	−40°C ≤ T_C ≤ +85°C, 1 σ		0.05		°/sec
In Run Bas Stability	1 σ		1.8		°/hr
Angular Random Walk	1 σ		0.09		°/√hr
Temperature Coefficient	−40°C ≤ T_C ≤ +85°C, 1 σ		0.0005		°/sec/°C
Linear Acceleration Effect	Any axis, 1 σ (CONFIG[7] = 1)		0.005		°/sec/*g*
	Any axis, 1 σ (CONFIG[7] = 0)		0.015		°/sec/*g*
Vibration Rectification Error			0.0003		°/sec/g^2
Noise					
Output Noise	No filtering		0.05		°/sec rms
Rate Noise Density	f = 10 Hz to 40 Hz, no filtering		0.002		°/sec/√Hz rms
−3 dB Bandwidth			480		Hz
Sensor Resonant Frequency			65		kHz
ACCELEROMETERS[4]	Each axis				
Dynamic Range		±8			*g*
Sensitivity	x_ACCL_OUT and x_ACCL_LOW (32-bit)		7.6294×10^{-9}		*g*/LSB
Repeatability[1]	−40°C ≤ T_C ≤ +85°C		0.05	0.2	%
Sensitivity Temperature Coefficient	−40°C ≤ T_C ≤ +85°C, 1 σ		±16		ppm/°C
Misalignment	Axis to axis		±0.035		Degrees
	Axis to frame (package)		±0.25		Degrees
Nonlinearity	Best fit straight line, ±2 *g*		0.1		% FS
	Best fit straight line, ±4 *g*		0.15		% FS
	Best fit straight line, ±8 *g*		1.6		% FS
Bias					
Repeatability[1, 3]	−40°C ≤ T_C ≤ +85°C, 1 σ		±3.5		m*g*
In Run Stability	1 σ		3.6		µ*g*
Velocity Random Walk	1 σ		0.008		m/sec/√hr
Temperature Coefficient	−40°C ≤ T_C ≤ +85°C, 1 σ		±0.008		m*g*/°C
Repeatability	−40°C ≤ T_C ≤ +85°C, 1 σ		1		m*g*
Noise					
Output Noise	No filtering		0.5		m*g* rms
Noise Density	f = 10 Hz to 40 Hz, no filtering		16		µ*g*/√Hz rms
−3 dB Bandwidth			750		Hz
Sensor Resonant Frequency			2.5		kHz
TEMPERATURE SENSOR					
Scale Factor	Output = 0x0000 at 25°C (±5°C)		0.01429		°C/LSB

Parameter	Test Conditions/Comments	Min	Typ	Max	Unit
LOGIC INPUTS[5]					
Input Voltage					
High, V_{IH}		2.0			V
Low, V_{IL}				0.8	V
$\overline{RST}$ Pulse Width		1			µs
Input Current					
Logic 1, I_{IH}	V_{IH} = 3.3 V			10	µA
Logic 0, I_{IL}	V_{IL} = 0 V				
All Pins Except $\overline{RST}$				10	µA
$\overline{RST}$ Pin			0.33		mA
Input Capacitance, C_{IN}			10		pF
DIGITAL OUTPUTS[5]					
Output Voltage					
High, V_{OH}	I_{SOURCE} = 0.5 mA	2.4			V
Low, V_{OL}	I_{SINK} = 2.0 mA			0.4	V
FLASH MEMORY	Endurance[6]	100,000			Cycles
Data Retention[7]	T_J = 85°C	20			Years
FUNCTIONAL TIMES[8]	Time until data is available				
Power-On Start-Up Time			230		ms
Reset Recovery Time	GLOB_CMD register, Bit 7 = 1 (see Table 142)		190		ms
	$\overline{RST}$ pulled low[9], then restored to high		230		ms
Flash Memory					
Update Time			1237		ms
Self Test Time	GLOB_CMD[1] = 1 (see Table 129)		40		ms
CONVERSION RATE			4.25		kSPS
Initial Clock Accuracy			0.02		%
Temperature Coefficient			40		ppm/°C
Sync Input Clock		3.0		4.5	kHz
POWER SUPPLY, VDD	Operating voltage range	3.0		3.6	V
Power Supply Current[10]	Normal mode, VDD = 3.3 V, µ + σ		89		mA

[1] The repeatability specifications represent a projection for long-term aging, which is derived from the drift behaviors that a sample of units exhibited throughout their 1000-hour, 110°C high temperature operating life (HTOL).
[2] Cross axis sensitivity is the sine of this number.
[3] Bias repeatability describes a long-term behavior over a variety of conditions. Short-term repeatability relates to the in run bias stability and noise density specifications.
[4] All specifications associated with the accelerometers relate to the full-scale range of ±8 *g*.
[5] The digital I/O signals use a 3.3 V system.
[6] Endurance is qualified as per JEDEC Standard 22, Method A117, measured at −40°C, +25°C, +85°C, and +125°C.
[7] The data retention specification assumes a junction temperature (T_J) of 85°C per JEDEC Standard 22, Method A117. Data retention lifetime decreases with T_J.
[8] These times do not include thermal settling and internal filter response times, which may affect overall accuracy.
[9] The $\overline{RST}$ line must be in a low state for at least 10 µs to ensure a proper reset initiation and recovery.
[10] Supply current transients can reach 250 mA during initial startup or reset recovery.

TIMING SPECIFICATIONS

T_C = 25°C, VDD = 3.3 V, unless otherwise noted.

Table 2.

Parameter	Description	Min[1]	Typ	Max[1]	Unit
f_{SCLK}	Serial clock	0.01		15	MHz
t_{STALL}[2]	Stall period between data	5			µs
t_{CLS}	Serial clock low period	31			ns
t_{CHS}	Serial clock high period	31			ns
$t_{\overline{CS}}$	Chip select to clock edge	32			ns
t_{DAV}	DOUT valid after SCLK edge			10	ns
t_{DSU}	DIN setup time before SCLK rising edge	2			ns
t_{DHD}	DIN hold time after SCLK rising edge	2			ns
t_{DR}, t_{DF}	DOUT rise/fall times, ≤100 pF loading		3	8	ns
t_{DSOE}	$\overline{CS}$ assertion to data out active	0		11	ns
t_{HD}	SCLK edge to data out invalid	0			ns
t_{SFS}	Last SCLK edge to $\overline{CS}$ deassertion	32			ns
t_{DSHI}	$\overline{CS}$ deassertion to data out high impedance	0		9	ns
t_{NV}	Data invalid time		11	15	µs
t_1	Input sync pulse width	5			µs
t_2	Input sync to data invalid		233		µs
t_3	Input sync period[3]	222.2			µs

[1] Guaranteed by design and characterization, but not tested in production.
[2] See Table 3 for exceptions to the stall time rating. Note that an insufficient stall time results in reading all 0s for the register attempting to be read.
[3] This measurement represents the inverse of the maximum frequency for the input sample clock: 4500 Hz.

Register Specific Stall Times

Table 3.

Parameter	Description	Min[1]	Typ	Max	Unit
STALL TIME					
FNCTIO_CTRL	Configure DIOx functions	340			µs
FILTR_BNK_0	Enable/select FIR filter banks	65			µs
FILTR_BNK_1	Enable/select FIR filter banks	65			µs
NULL_CNFG	Configure autonull bias function	71			µs
SYNC_SCALE	Configure input clock scale factor	340			µs
DEC_RATE	Configure decimation rate	340			µs
GPIO_CTRL	Configure general-purpose I/O lines	45			µs
CONFIG	Configure miscellaneous functions	45			µs
GLOB_CMD[1]	On demand self test	40			ms
GLOB_CMD[3]	Flash memory update	1.24			sec
GLOB_CMD[6]	Factory calibration restore	350			µs
GLOB_CMD[7]	Software reset	130			ms

[1] Monitoring the data ready signal (see Table 131 for FNCTIO_CTRL configuration) for the return of regular pulsing can help minimize system wait times.

Timing Diagrams

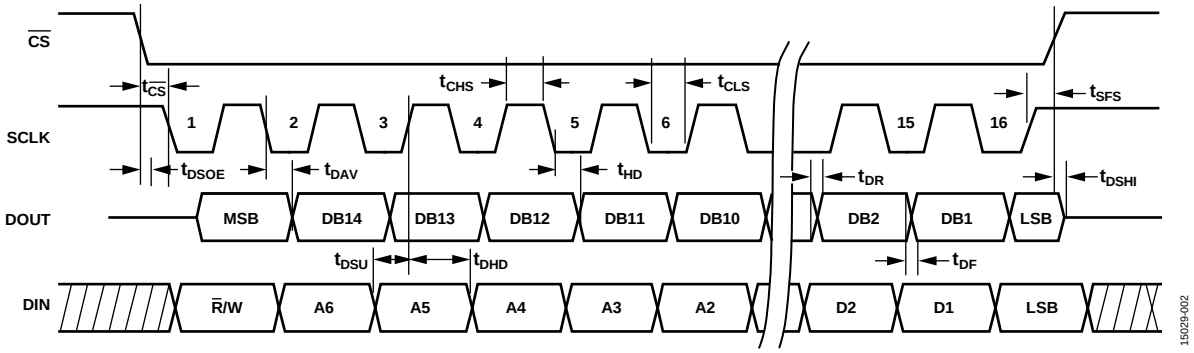


Figure 2. SPI Timing and Sequence

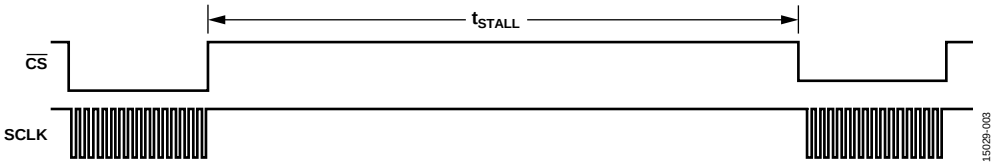


Figure 3. Stall Time and Data Rate

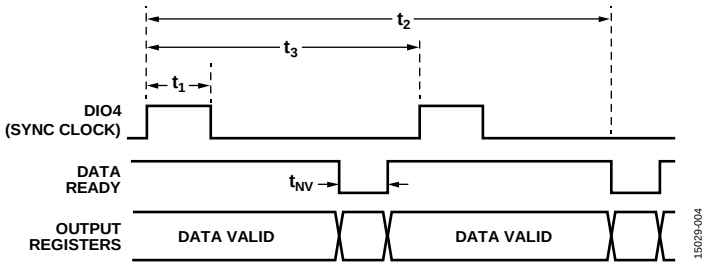


Figure 4. Input Clock Timing Diagram, FNCTIO_CTRL[7:4] = 0xFD

ABSOLUTE MAXIMUM RATINGS

Table 4.

Parameter	Rating
Acceleration	
Any Axis, Unpowered	1500 *g*
Any Axis, Powered	1500 *g*
VDD to GND	−0.3 V to +3.6 V
Digital Input Voltage to GND	−0.3 V to VDD + 0.2 V
Digital Output Voltage to GND	−0.3 V to VDD + 0.2 V
Operating Temperature Range	−40°C to +105°C
Storage Temperature Range[1]	−55°C to +150°C
Barometric Pressure	2 bar

[1] Extended exposure to temperatures that are lower than −40°C or higher than +105°C can adversely affect the accuracy of the factory calibration.

Stresses at or above those listed under Absolute Maximum Ratings may cause permanent damage to the product. This is a stress rating only; functional operation of the product at these or any other conditions above those indicated in the operational section of this specification is not implied. Operation beyond the maximum operating conditions for extended periods may affect product reliability.

THERMAL RESISTANCE

Thermal performance is directly linked to printed circuit board (PCB) design and operating environment. Careful attention to PCB thermal design is required.

θ_{JA} is the natural convection junction to ambient thermal resistance measured in a one cubic foot sealed enclosure.

θ_{JC} is the junction to case thermal resistance.

The ADIS16490 is a multichip module, which includes many active components. The values in Table 5 identify the thermal response of the hottest component inside of the ADIS16490, with respect to the overall power dissipation of the module. This approach enables a simple method for predicting the temperature of the hottest junction, based on either ambient or case temperature.

For example, when the ambient temperature is 70°C, the hottest junction inside of the ADIS16490 is 76.7°C.

$$T_J = \theta_{JA} \times V_{DD} \times I_{DD} + 70°C$$

$$T_J = 22.8°C/W \times 3.3\ V \times 0.089\ A + 70°C$$

$$T_J = 76.7°C$$

Table 5. Package Characteristics

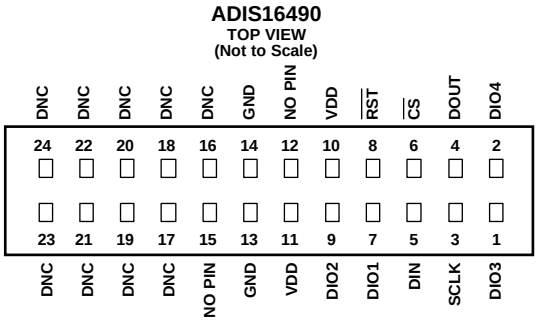
Package Type	θ_{JA}	θ_{JC}	Device Weight
ML-24-9[1]	30.7°C/W	20.9°C/W	42 g

[1] Thermal impedance simulated values come from a case when 4 M2 × 0.4 mm machine screws (torque = 20 inch-ounces) secure the ADIS16490 to the printed circuit board.

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS



NOTES
1. THIS REPRESENTATION DISPLAYS THE TOP VIEW PINOUT FOR THE MATING SOCKET CONNECTOR.
2. THE ACTUAL CONNECTOR PINS ARE NOT VISIBLE FROM THE TOP VIEW.
3. MATING CONNECTOR: SAMTEC CLM-112-02 OR EQUIVALENT.
4. DNC = DO NOT CONNECT.
5. PIN 12 AND PIN 15 ARE NOT PHYSICALLY PRESENT.

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Figure 5. Pin Configuration

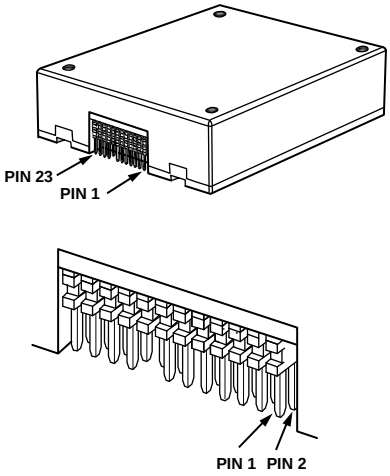

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Figure 6. Axial Orientation (Top Side Facing Up)

Table 6. Pin Function Descriptions

Pin No.	Mnemonic	Type	Description
1	DIO3	Input/output	Configurable Digital Input/Output 3.
2	DIO4	Input/output	Configurable Digital Input/Output 4.
3	SCLK	Input	SPI Serial Clock.
4	DOUT	Output	SPI Data Output. Clocks output on the SCLK falling edge.
5	DIN	Input	SPI Data Input. Clocks input on the SCLK rising edge.
6	$\overline{CS}$	Input	SPI Chip Select.
7	DIO1	Input/output	Configurable Digital Input/Output 1.
8	$\overline{RST}$	Input	Reset.
9	DIO2	Input/output	Configurable Digital Input/Output 2.
10, 11	VDD	Supply	Power Supply.
12, 15	NO PIN	Not applicable	These pins are not physically present.
13, 14	GND	Supply	Power Ground.
16 to 22, 24	DNC	Not applicable	Do Not Connect. Do not connect to these pins.
23	DNC	Not applicable	Do Not Connect. Do not connect to this pin. This pin can tolerate connection to 3.3 V.

TYPICAL PERFORMANCE CHARACTERISTICS

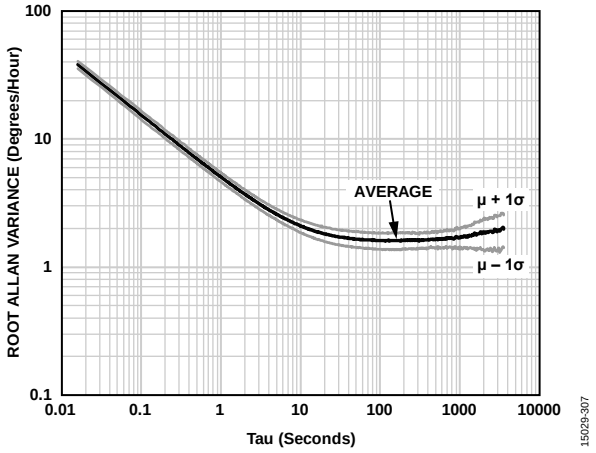

Figure 7. Gyroscope Root Allan Variance

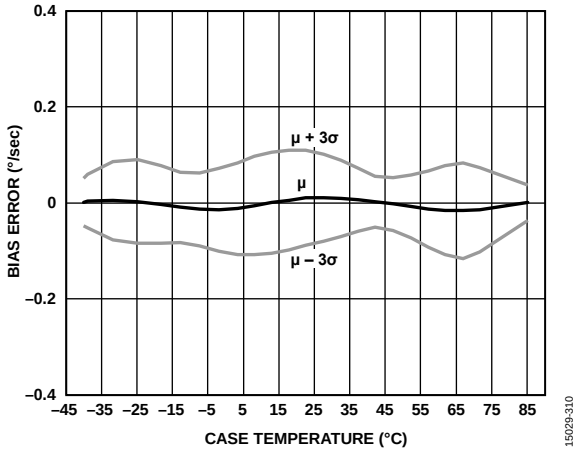

Figure 10. Gyroscope Bias Error, –40°C to +85°C, 1°C/min

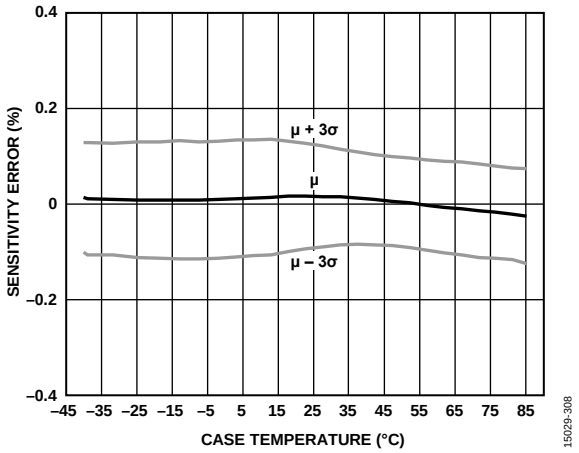

Figure 8. Gyroscope Sensitivity Error, –40°C to +85°C, 1°C/min

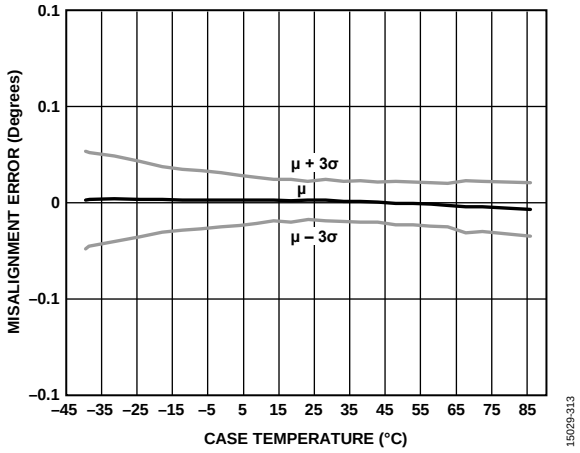

Figure 11. Gyroscope Axis to Axis Misalignment Error, –40°C to +85°C

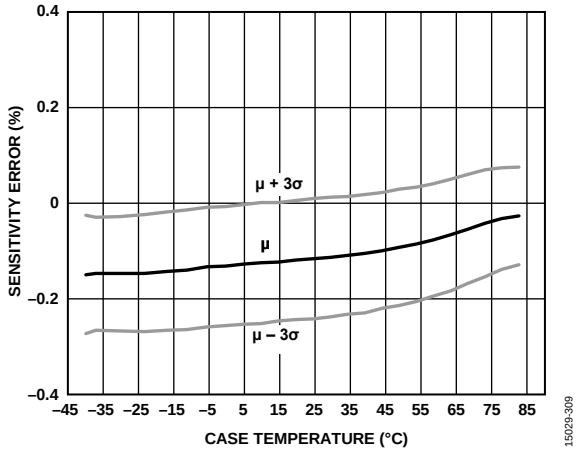

Figure 9. Gyroscope Sensitivity Error, +85°C to –40°C, 1°C/min

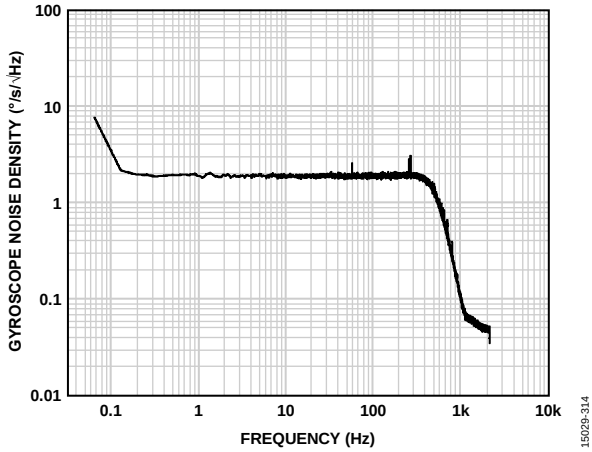

Figure 12. Gyroscope Noise Density, T_C = 25°C

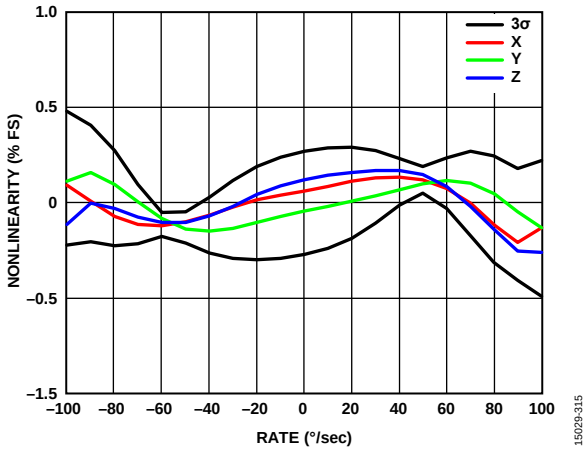

Figure 13. Gyrscope Nonlinearity

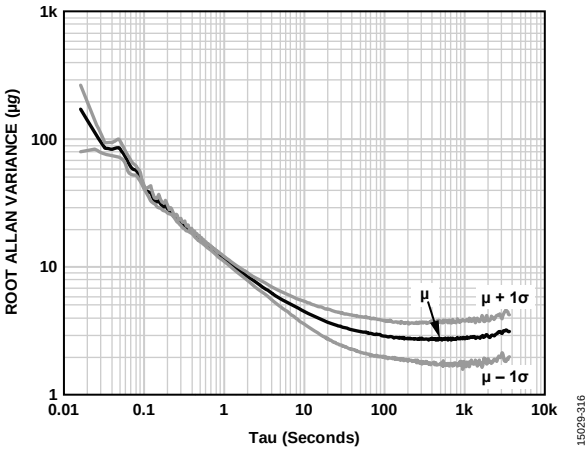

Figure 14. Accelerometer Root Allan Variance, 25°C

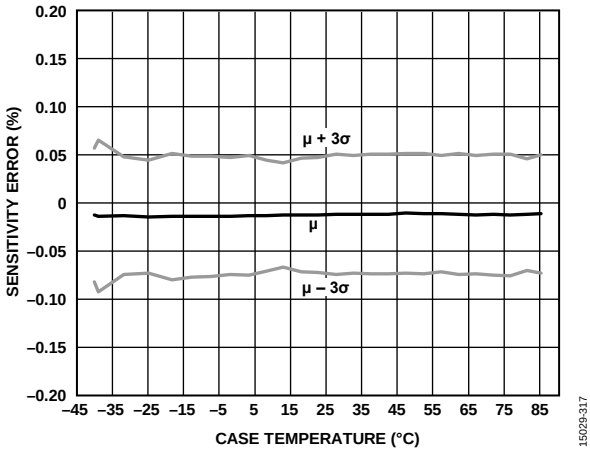

Figure 15. Accelerometer Sensitivity Error, –40°C to +85°C, 1°C/min

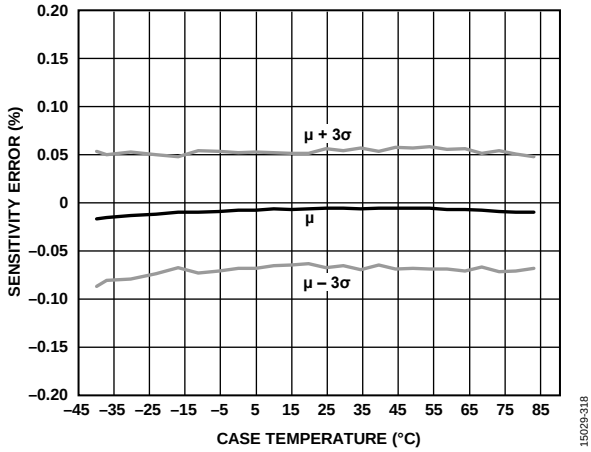

Figure 16. Accelerometer Sensitivity Error, +85°C to –40°C, 1°C/min

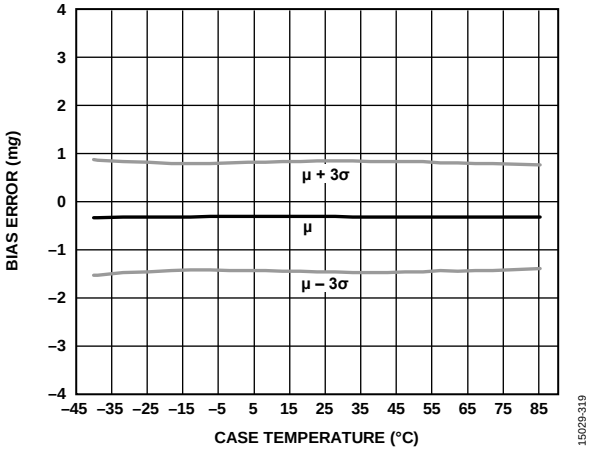

Figure 17. Accelerometer Bias Error, –40°C to +85°C, 1°C/min

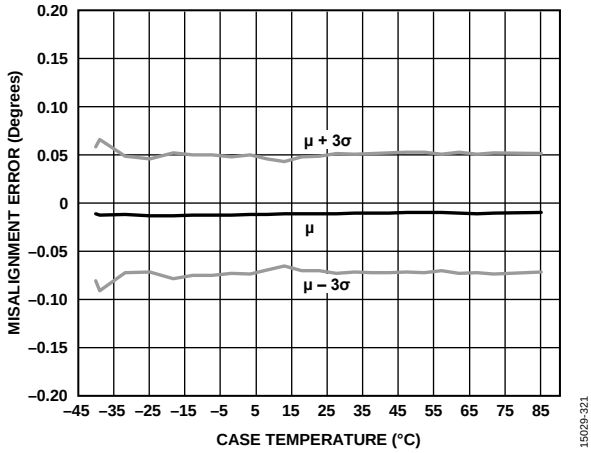

Figure 18. Accelerometer Axis to Axis Misalignment Error, –40°C to +85°C

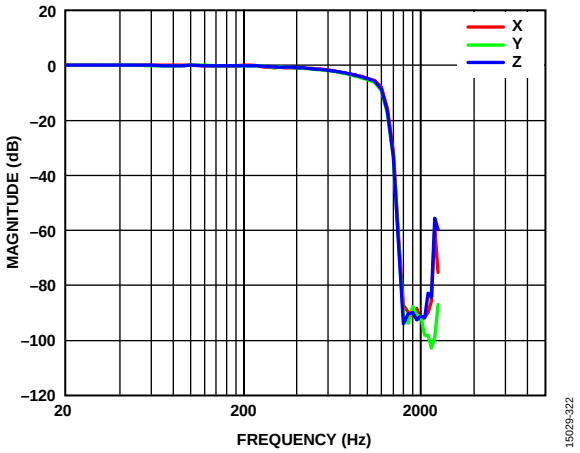

Figure 19. Accelerometer Vibration Response (Swept Sine, 2 g peak)

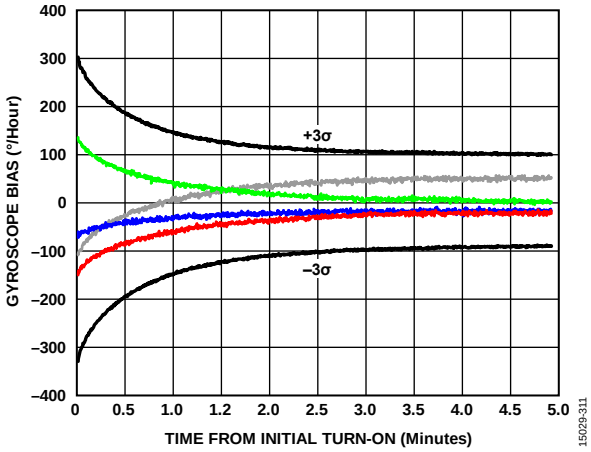

Figure 21. Gyroscope Bias vs. Time from Initial Turn-On

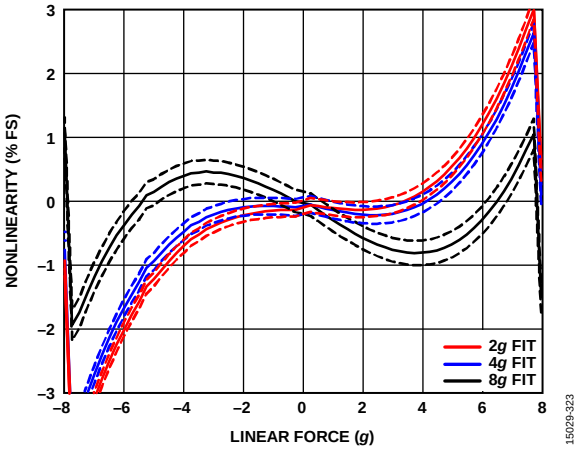

Figure 20. Accelerometer Nonlinearity (FIT Is Curve Fit)

THEORY OF OPERATION

The ADIS16490 is an autonomous sensor system. A power-on self test begins automatically after the voltage on the power supply pins reaches a minimum safe level as defined by Table 1. After the automatic power-on self test, the ADIS16490 begins sampling, processing, and loading calibrated sensor data into the output registers, which are accessible using the SPI port.

INERTIAL SENSOR SIGNAL CHAIN

Figure 22 provides the basic signal chain for the inertial sensors in the ADIS16490, which processes data at a rate of 4250 SPS when using the internal sample clock. Using one of the external clock options in FNCTIO_CTRL[7:4] (see Table 131) can provide flexibility in selecting this rate.

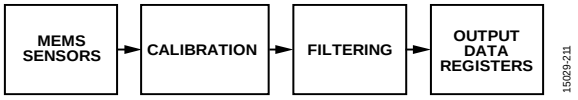

Figure 22. Signal Processing Diagram, Inertial Sensors

Gyroscope Data Sampling

The ADIS16490 produces angular rate measurements around three orthogonal axes (x, y, and z). Figure 23 shows the basic signal flow for the production of x-axis gyroscope data (same as y-axis and z-axis). This signal chain contains two digital MEMS gyroscopes (X_{G1} and X_{G2}), which have their own ADC and sample clocks (f_{SGX1} and f_{SGX2} = 4100 Hz that produce data independently from each other. The sensor to sensor tolerance on this sample rate is ±200 SPS. Processing these data starts with combining (summation and rescale) the most recent sample from each gyroscope together by using an independent sample master frequency (f_{SM}) clock (f_{SM} = 4250 Hz, see Figure 23), which drives the rest of the digital signal processing (calibration, alignment, and filtering) for the gyroscopes and accelerometers.

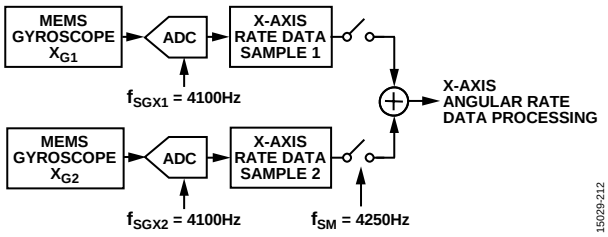

Figure 23. Gyroscope Data Sampling

Accelerometer Data Sampling

The ADIS16490 produces linear acceleration measurements along the same orthogonal axes (x, y, and z) as the gyroscopes, using the same clock (f_{SM}, see Figure 23 and Figure 24) that triggers data acquisition and subsequent processing of the gyroscope data.

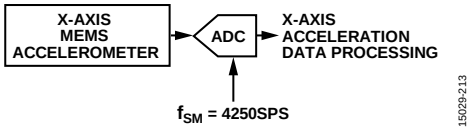

Figure 24. Accelerometer Data Sampling

External Clock Options

The ADIS16490 offers two modes of operation to control data production with an external clock: sync mode and pulse per second (PPS) mode. In sync mode, the external clock directly controls the data sampling and production clock (f_{SM} in Figure 23 and Figure 24). In PPS mode, users can provide a lower input clock rate (1 Hz to 128 Hz) and use a scale factor (SYNC_SCALE register, see Table 141) to establish a data collection and processing rate that is between 3000 Hz and 4250 Hz for best performance.

Inertial Sensor Calibration

The calibration function for the gyroscopes and the accelerometers has two components: factory calibration and user calibration (see Figure 25).

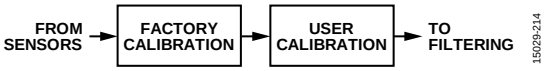

Figure 25. Gyroscope Calibration Processing

Gyroscope Factory Calibration

Gyroscope factory calibration applies the following correction formula to the data of each gyroscope:

$$\begin{bmatrix} \omega_{XC} \\ \omega_{YC} \\ \omega_{ZC} \end{bmatrix} = \begin{bmatrix} m_{11} & m_{12} & m_{13} \\ m_{21} & m_{22} & m_{23} \\ m_{31} & m_{32} & m_{33} \end{bmatrix} \times \left(\begin{bmatrix} \omega_X \\ \omega_Y \\ \omega_Z \end{bmatrix} + \begin{bmatrix} b_X \\ b_Y \\ b_Z \end{bmatrix} + \begin{bmatrix} g_{11} & g_{12} & g_{13} \\ g_{21} & g_{22} & g_{23} \\ g_{31} & g_{32} & g_{33} \end{bmatrix} \times \begin{bmatrix} a'_X \\ a'_Y \\ a'_Z \end{bmatrix} \right) \quad (1)$$

where:

ω_{XC}, ω_{YC}, and ω_{ZC} are the postcalibration gyroscope data.
m_{11}, m_{12}, m_{13}, m_{21}, m_{22}, m_{23}, m_{31}, m_{32}, and m_{33} are the scale and alignment correction factors.
ω_X, ω_Y, and ω_Z are the precalibration gyroscope data.
b_X, b_Y, and b_Z are the bias correction factors.
g_{11}, g_{12}, g_{13}, g_{21}, g_{22}, g_{23}, g_{31}, g_{32}, and g_{33} are the linear g correction factors.
a'_X, a'_Y, and a'_Z are the postcalibration accelerometer data.

All the correction factors in each matrix/array are derived from direct observation of the response of each gyroscope to a variety of rotation rates at multiple temperatures across the calibration temperature range (−40°C ≤ T_C ≤ +85°C). These correction factors are stored in the flash memory bank, but they are not available for observation. CONFIG[7] provides an on/off control for the linear g compensation (see Table 135). See Figure 46 for more details on the user calibration options that are available for the gyroscopes.

Accelerometer Factory Calibration

The accelerometer factory calibration applies the following correction formulas to the data of each accelerometer:

$$\begin{bmatrix} a'_X \\ a'_Y \\ a'_Z \end{bmatrix} = \begin{bmatrix} m_{11} & m_{12} & m_{13} \\ m_{21} & m_{22} & m_{23} \\ m_{31} & m_{32} & m_{33} \end{bmatrix} \times \left(\begin{bmatrix} a_X \\ a_Y \\ a_Z \end{bmatrix} + \begin{bmatrix} b_X \\ b_Y \\ b_Z \end{bmatrix} \right) + \begin{bmatrix} 0 & p_{12} & p_{13} \\ p_{21} & 0 & p_{23} \\ p_{31} & p_{32} & 0 \end{bmatrix} \times \begin{bmatrix} \omega^2_{XC} \\ \omega^2_{YC} \\ \omega^2_{ZC} \end{bmatrix} \quad (2)$$

where:

a_X, a_Y, and a_Z are the precalibration accelerometer data.
a'_X, a'_Y, and a'_Z are the postcalibration accelerometer data.
m_{11}, m_{12}, m_{13}, m_{21}, m_{22}, m_{23}, m_{31}, m_{32}, and m_{33} are the scale and alignment correction factors.
b_X, b_Y, and b_Z are the bias correction factors.
0, p_{12}, p_{13}, p_{21}, 0, p_{23}, p_{31}, p_{32}, and 0 are the point of percussion correction factors
ω^2_{XC}, ω^2_{YC}, and ω^2_{ZC} are the postcalibration gyroscope data (squared).

All the correction factors in each matrix/array are derived from direct observation of the response of each accelerometer to a variety of inertial test conditions at multiple temperatures across the calibration temperature range (−40°C ≤ T_C ≤ +85°C). These correction factors are stored in the flash memory bank, but they are not available for observation. CONFIG[6] provides an on/off control for the point of percussion alignment (see Table 135). See Figure 47 for more details on the user calibration options that are available for the accelerometers.

Filtering

After calibration, the data of each inertial sensor passes through two digital filters, both of which have user configurable attributes: FIR and decimation (see Figure 26).

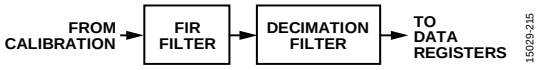

Figure 26. Inertial Sensor Filtering

The FIR filter includes four banks of coefficients that have 120 taps each. FILTR_BNK_0 (see Table 143) and FILTR_BNK_1 (see Table 145) provide the configuration options for the use of the FIR filters of each inertial sensor. Each FIR filter bank includes a preconfigured filter, but users can design their own filters and write over these values using the register of each coefficient. For example, Table 174 provides the details for FIR_COEF_A071, which contains Coefficient 71 in FIR Bank A. Refer to Figure 50 for the frequency response of the factory default filters. These filters do not represent any specific application environment; they are only examples.

The decimation filter averages multiple samples together to produce each register update. In this type of filter structure, the number of samples in the average is equal to the reduction in the update rate for the output data registers. See the DEC_RATE register for the user controls for this filter (see Table 137).

REGISTER STRUCTURE

All communication with the ADIS16490 involves accessing its user registers. The register structure contains both output data and control registers. The output data registers include the latest sensor data, error flags, and identification data. The control registers include sample rate, filtering, input/output, calibration, and diagnostic configuration options. All communication between the ADIS16490 and an external processor involves either reading or writing to one of the user registers.

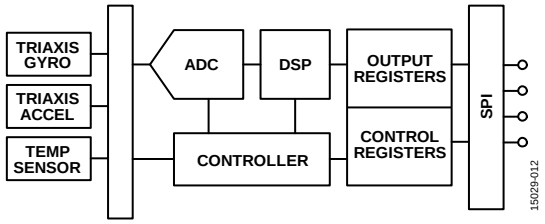

Figure 27. Basic Operation

The register structure uses a paged addressing scheme that contains 13 pages, with each page containing 64 register locations. Each register is 16 bits wide, with each byte having its own unique address within the memory map of that page. The SPI port has access to one page at a time, using the bit sequence in Figure 28. Select the page to activate for SPI access by writing its code to the PAGE_ID register. Read the PAGE_ID register to determine which page is currently active. Table 7 displays the PAGE_ID contents for each page and their basic functions. The PAGE_ID register is located at Address 0x00 on every page.

Table 7. User Register Page Assignments

Page	PAGE_ID	Function
0	0x00	Output data, clock, identification
1	0x01	Reserved
2	0x02	Calibration
3	0x03	Control: sample rate, filtering, I/O
4	0x04	Serial number, CRC values
5	0x05	FIR Filter Bank A, Coefficient 0 to Coefficient 59
6	0x06	FIR Filter Bank A, Coefficient 60 to Coefficient 119
7	0x07	FIR Filter Bank B, Coefficient 0 to Coefficient 59
8	0x08	FIR Filter Bank B, Coefficient 60 to Coefficient 119
9	0x09	FIR Filter Bank C, Coefficient 0 to Coefficient 59
10	0x0A	FIR Filter Bank C, Coefficient 60 to Coefficient 119
11	0x0B	FIR Filter Bank D, Coefficient 0 to Coefficient 59
12	0x0C	FIR Filter Bank D, Coefficient 60 to Coefficient 119

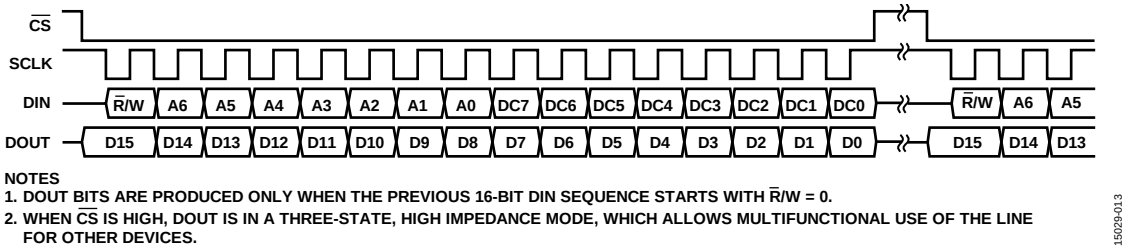

Figure 28. SPI Communication Bit Sequence

SERIAL PERIPHERAL INTERFACE

The serial peripheral interface (SPI) provides access to the user register structures and typically connects to a compatible port on an embedded processor, using the connection diagram shown in Figure 29. The four SPI signals facilitate synchronous, serial data communication.

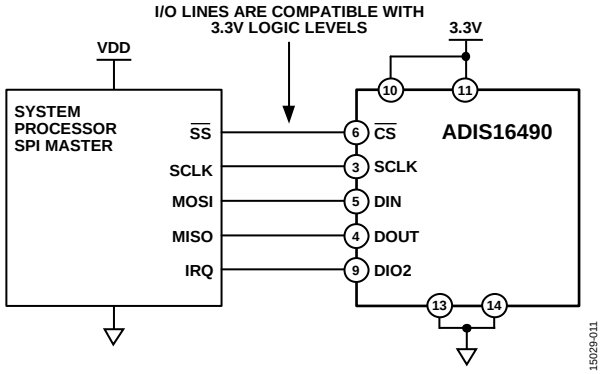

Figure 29. Electrical Connection Diagram

Table 8. Generic Master Processor Pin Names and Functions

Mnemonic	Function
$\overline{SS}$	Slave select
IRQ	Interrupt request
MOSI	Master output, slave input
MISO	Master input, slave output
SCLK	Serial clock

Embedded processors typically use control registers to configure their serial ports for communicating with SPI slave devices such as the ADIS16490. Table 9 provides a list of settings that describe the SPI protocol of the ADIS16490. The initialization routine of the master processor typically establishes these settings using firmware commands to write them into its serial control registers.

Table 9. Generic Master Processor SPI Settings

Processor Setting	Description
Master	ADIS16490 operates as slave
SCLK ≤ 15 MHz	Maximum serial clock rate
SPI Mode 3	CPOL = 1 (polarity), CPHA = 1 (phase)
MSB First Mode	Bit sequence, see Figure 28 for coding
16-Bit Mode	Shift register/data length

DATA READY

The factory default configuration provides users with a data ready (DR) signal on the DIO2 pin, which pulses low when the output data registers are updating (see Figure 30). In this configuration, connect DIO2 to a pin on the embedded processor, which triggers data collection, when this signal pulses high. Register FNCTIO_CTRL[3:0] (see Table 131) provides user configuration options for this function.

Figure 30. Data Ready, When FNCTIO_CTRL[3:0] = 1101 (default)

During the start-up and reset recovery processes, the DR signal can exhibit transient behavior before data production begins. Figure 31 provides an example of the DR behavior during startup, and Figure 32 and Figure 33 provide examples of the DR behavior during recovery from reset commands.

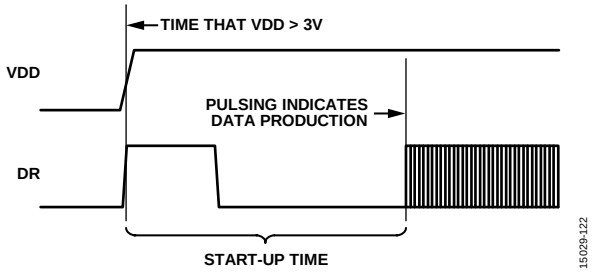

Figure 31. Data Ready Response During Startup

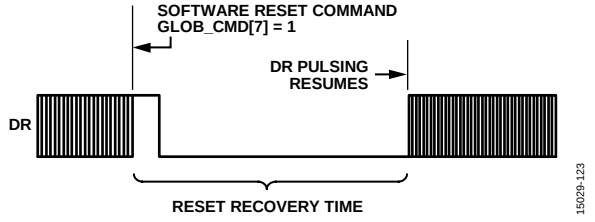

Figure 32. Data Ready Response During Reset (Register GLOB_CMD, Bit 7 = 1) Recovery

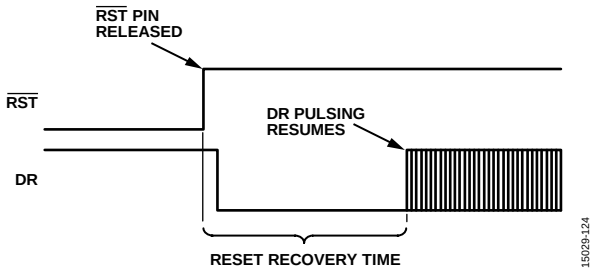

Figure 33. Data Ready Response During Reset ($\overline{RST}$ = 0) Recovery

READING SENSOR DATA

Reading a single register requires two 16-bit cycles on the SPI: one to request the contents of a register and another to receive those contents. The 16-bit command code (see Figure 28) for a read request on the SPI has three parts: the read bit ($\overline{R}/W$ = 0), either address of the register, [A6:A0], and eight don't care bits, [DC7:DC0]. Figure 34 provides an example that includes two register reads in succession. This example starts with DIN = 0x1A00, to request the contents of the Z_GYRO_OUT register, and follows with 0x1800, to request the contents of the Z_GYRO_LOW register (assuming PAGE_ID already equals 0x0000). The sequence in Figure 34 also illustrates full duplex mode of operation, which means that the ADIS16490 can receive requests on DIN while also transmitting data out on DOUT within the same 16-bit SPI cycle.

Figure 34. SPI Read Example

Figure 35 provides an example of the four SPI signals when reading the PROD_ID register (see Table 79) in a repeating pattern. This pattern can be helpful when troubleshooting the SPI interface setup and communications.

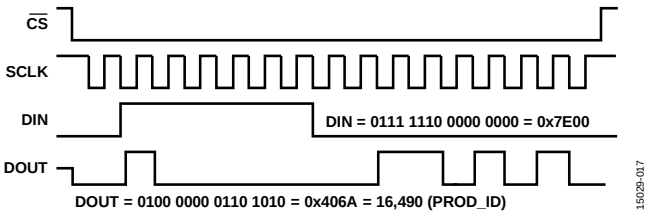

Figure 35. SPI Read Example, Second 16-Bit Sequence

DEVICE CONFIGURATION

Each register contains 16 bits (two bytes). Bits[7:0] contain the low byte and Bits[15:8] contain the high byte of each register. Each byte has its own unique address in the user register map (see Table 10). Updating the contents of a register requires writing to its low byte first and its high byte second. There are three parts to coding a SPI command (see Figure 28), which writes a new byte of data to a register: the write bit ($\overline{R}/W$ = 1), the address of the byte, [A6:A0], and the new data for that location, [DC7:DC0]. Figure 36 provides a coding example for writing 0xFEDC to the XG_BIAS_LOW register (see Table 93), assuming that PAGE_ID already equals 0x0002.

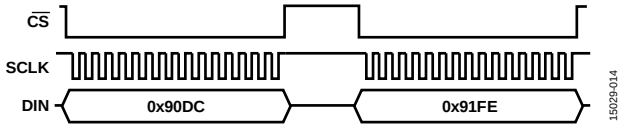

Figure 36. SPI Sequence for Writing 0xFEDC to XG_BIAS_LOW

Dual Memory Structure

The ADIS16490 uses a dual memory structure (see Figure 37), with SRAM supporting real-time operation and flash memory storing operational code, calibration coefficients, and user configurable register settings. The manual flash update command (GLOB_CMD[3], see Table 129) provides a single-command method for storing user configuration settings into flash memory, for automatic recall during the next power-on or reset recovery process. This portion of the flash memory bank has two independent banks that operate in a ping pong manner, alternating with every flash update. During power-on or reset recovery, the ADIS16490 performs a cyclic redundancy check (CRC) on the SRAM and compares it to a CRC computation from the same memory locations in flash memory. If this fails, the ADIS16490 resets and boots up from the other flash memory location. SYS_E_FLAG[2] (see Table 16) provides an error flag for detecting when the back-up flash memory supported the last power-on or reset recovery. Table 10 provides a memory map for the user registers in the ADIS16490, which includes flash backup support (indicated by yes or no in the flash column).

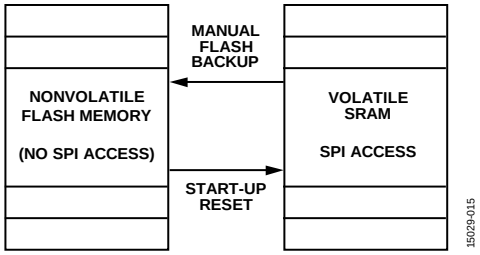

Figure 37. SRAM and Flash Memory Diagram

USER REGISTER MEMORY MAP

Table 10. User Register Memory Map (N/A Means Not Applicable)

Name	R/W	Flash Backup	PAGE_ID	Address	Default	Register Description
PAGE_ID	R/W	No	0x00	0x00, 0x01	0x0000	Page identifier
Reserved	N/A	N/A	0x00	0x02, 0x03	N/A	Reserved
DATA_CNT	R	No	0x00	0x04, 0x05	N/A	Data counter
Reserved	N/A	N/A	0x00	0x06, 0x07	N/A	Reserved
SYS_E_FLAG	R	No	0x00	0x08, 0x09	N/A	Output, system error flags (0x0000 if no errors)
DIAG_STS	R	No	0x00	0x0A, 0x0B	N/A	Output, self test error flags (0x0000 if no errors)
Reserved	N/A	N/A	0x00	0x0C, 0x0D	N/A	Reserved
TEMP_OUT	R	No	0x00	0x0E, 0x0F	N/A	Output, temperature
X_GYRO_LOW	R	No	0x00	0x10, 0x11	N/A	Output, x-axis gyroscope, low word
X_GYRO_OUT	R	No	0x00	0x12, 0x13	N/A	Output, x-axis gyroscope, high word
Y_GYRO_LOW	R	No	0x00	0x14, 0x15	N/A	Output, y-axis gyroscope, low word
Y_GYRO_OUT	R	No	0x00	0x16, 0x17	N/A	Output, y-axis gyroscope, high word
Z_GYRO_LOW	R	No	0x00	0x18, 0x19	N/A	Output, z-axis gyroscope, low word
Z_GYRO_OUT	R	No	0x00	0x1A, 0x1B	N/A	Output, z-axis gyroscope, high word
X_ACCL_LOW	R	No	0x00	0x1C, 0x1D	N/A	Output, x-axis accelerometer, low word
X_ACCL_OUT	R	No	0x00	0x1E, 0x1F	N/A	Output, x-axis accelerometer, high word
Y_ACCL_LOW	R	No	0x00	0x20, 0x21	N/A	Output, y-axis accelerometer, low word
Y_ACCL_OUT	R	No	0x00	0x22, 0x23	N/A	Output, y-axis accelerometer, high word
Z_ACCL_LOW	R	No	0x00	0x24, 0x25	N/A	Output, z-axis accelerometer, low word
Z_ACCL_OUT	R	No	0x00	0x26, 0x27	N/A	Output, z-axis accelerometer, high word
TIME_STAMP	R	No	0x00	0x28, 0x29	N/A	Output, time stamp
Reserved	N/A	N/A	0x00	0x2A to 0x3F	N/A	Reserved
X_DELTANG_LOW	R	No	0x00	0x40, 0x41	N/A	Output, x-axis delta angle, low word
X_DELTANG_OUT	R	No	0x00	0x42, 0x43	N/A	Output, x-axis delta angle, high word
Y_DELTANG_LOW	R	No	0x00	0x44, 0x45	N/A	Output, y-axis delta angle, low word
Y_DELTANG_OUT	R	No	0x00	0x46, 0x47	N/A	Output, y-axis delta angle, high word
Z_DELTANG_LOW	R	No	0x00	0x48, 0x49	N/A	Output, z-axis delta angle, low word
Z_DELTANG_OUT	R	No	0x00	0x4A, 0x4B	N/A	Output, z-axis delta angle, high word
X_DELTVEL_LOW	R	No	0x00	0x4C, 0x4D	N/A	Output, x-axis delta velocity, low word
X_DELTVEL_OUT	R	No	0x00	0x4E, 0x4F	N/A	Output, x-axis delta velocity, high word
Y_DELTVEL_LOW	R	No	0x00	0x50, 0x51	N/A	Output, y-axis delta velocity, low word
Y_DELTVEL_OUT	R	No	0x00	0x52, 0x53	N/A	Output, y-axis delta velocity, high word
Z_DELTVEL_LOW	R	No	0x00	0x54, 0x55	N/A	Output, z-axis delta velocity, low word
Z_DELTVEL_OUT	R	No	0x00	0x56, 0x57	N/A	Output, z-axis delta velocity, high word
Reserved	N/A	N/A	0x00	0x58 to 0x7D	N/A	Reserved
PROD_ID	R	Yes	0x00	0x7E, 0x7F	0x406A	Output, product identification (16490d)
Reserved	N/A	N/A	0x01	0x00 to 0x7F	N/A	Reserved
PAGE_ID	R/W	No	0x02	0x00, 0x01	0x0000	Page identifier
Reserved	N/A	N/A	0x02	0x02, 0x03	N/A	Reserved
X_GYRO_SCALE	R/W	Yes	0x02	0x04, 0x05	0x0000	Calibration, scale, x-axis gyroscope
Y_GYRO_SCALE	R/W	Yes	0x02	0x06, 0x07	0x0000	Calibration, scale, y-axis gyroscope
Z_GYRO_SCALE	R/W	Yes	0x02	0x08, 0x09	0x0000	Calibration, scale, z-axis gyroscope
X_ACCL_SCALE	R/W	Yes	0x02	0x0A, 0x0B	0x0000	Calibration, scale, x-axis accelerometer
Y_ACCL_SCALE	R/W	Yes	0x02	0x0C, 0x0D	0x0000	Calibration, scale, y-axis accelerometer
Z_ACCL_SCALE	R/W	Yes	0x02	0x0E, 0x0F	0x0000	Calibration, scale, z-axis accelerometer
XG_BIAS_LOW	R/W	Yes	0x02	0x10, 0x11	0x0000	Calibration, bias, gyroscope, x-axis, low word
XG_BIAS_HIGH	R/W	Yes	0x02	0x12, 0x13	0x0000	Calibration, bias, gyroscope, x-axis, high word
YG_BIAS_LOW	R/W	Yes	0x02	0x14, 0x15	0x0000	Calibration, bias, gyroscope, y-axis, low word
YG_BIAS_HIGH	R/W	Yes	0x02	0x16, 0x17	0x0000	Calibration, bias, gyroscope, y-axis, high word
ZG_BIAS_LOW	R/W	Yes	0x02	0x18, 0x19	0x0000	Calibration, bias, gyroscope, z-axis, low word

Name	R/W	Flash Backup	PAGE_ID	Address	Default	Register Description
ZG_BIAS_HIGH	R/W	Yes	0x02	0x1A, 0x1B	0x0000	Calibration, bias, gyroscope, z-axis, high word
XA_BIAS_LOW	R/W	Yes	0x02	0x1C, 0x1D	0x0000	Calibration, bias, accelerometer, x-axis, low word
XA_BIAS_HIGH	R/W	Yes	0x02	0x1E, 0x1F	0x0000	Calibration, bias, accelerometer, x-axis, high word
YA_BIAS_LOW	R/W	Yes	0x02	0x20, 0x21	0x0000	Calibration, bias, accelerometer, y-axis, low word
YA_BIAS_HIGH	R/W	Yes	0x02	0x22, 0x23	0x0000	Calibration, bias, accelerometer, y-axis, high word
ZA_BIAS_LOW	R/W	Yes	0x02	0x24, 0x25	0x0000	Calibration, bias, accelerometer, z-axis, low word
ZA_BIAS_HIGH	R/W	Yes	0x02	0x26, 0x27	0x0000	Calibration, bias, accelerometer, z-axis, high word
Reserved	N/A	N/A	0x02	0x28 to 0x73	0x0000	Reserved
USER_SCR_1	R/W	Yes	0x02	0x74, 0x75	0x0000	User Scratch Register 1
USER_SCR_2	R/W	Yes	0x02	0x76, 0x77	0x0000	User Scratch Register 2
USER_SCR_3	R/W	Yes	0x02	0x78, 0x79	0x0000	User Scratch Register 3
USER_SCR_4	R/W	Yes	0x02	0x7A, 0x7B	0x0000	User Scratch Register 4
FLSHCNT_LOW	R	Yes	0x02	0x7C, 0x7D	N/A	Diagnostic, flash memory count, low word
FLSHCNT_HIGH	R	Yes	0x02	0x7E, 07F	N/A	Diagnostic, flash memory count, high word
PAGE_ID	R/W	No	0x03	0x00, 0x01	0x0000	Page identifier
GLOB_CMD	W	No	0x03	0x02, 0x03	N/A	Control, global commands
Reserved	N/A	N/A	0x03	0x04, 0x05	N/A	Reserved
FNCTIO_CTRL	R/W	Yes	0x03	0x06, 0x07	0x000D	Control, I/O pins, functional definitions
GPIO_CTRL	R/W	Yes	0x03	0x08, 0x09	0x00X0[1]	Control, I/O pins, general purpose
CONFIG	R/W	Yes	0x03	0x0A, 0x0B	0x00C0	Control, clock, and miscellaneous correction
DEC_RATE	R/W	Yes	0x03	0x0C, 0x0D	0x0000	Control, output sample rate decimation
NULL_CNFG	R/W	Yes	0x03	0x0E, 0x0F	0x070A	Control, automatic bias correction configuration
SYNC_SCALE	R/W	Yes	0x03	0x10, 0x11	0x109A	Input clock scaling (PPS mode)
Reserved	N/A	N/A	0x03	0x12 to 0x15	N/A	Reserved
FILTR_BNK_0	R/W	Yes	0x03	0x16, 0x17	0x0000	Filter selection
FILTR_BNK_1	R/W	Yes	0x03	0x18, 0x19	0x0000	Filter selection
Reserved	N/A	N/A	0x03	0x1A to 0x77	N/A	Reserved
FIRM_REV	R	Yes	0x03	0x78, 0x79	N/A	Firmware revision
FIRM_DM	R	Yes	0x03	0x7A, 0x7B	N/A	Firmware programming date: day/month
FIRM_Y	R	Yes	0x03	0x7C, 0x7D	N/A	Firmware programming date: year
BOOT_REV	R	Yes	0x03	0x7E, 0x7F	N/A	Boot loader revision
PAGE_ID	R/W	No	0x04	0x00, 0x01	0x0000	Page identifier
Reserved	N/A	N/A	0x04	0x02, 0x03	N/A	Reserved
CAL_SIGTR_LWR	R	Yes	0x04	0x04, 0x05	N/A	Signature CRC, calibration coefficients, low word
CAL_SIGTR_UPR	R	Yes	0x04	0x06, 0x07	N/A	Signature CRC, calibration coefficients, high word
CAL_DRVTN_LWR	R	No	0x04	0x08, 0x09	N/A	Real-time CRC, calibration coefficients, low word
CAL_DRVTN_UPR	R	No	0x04	0x0A, 0x0B	N/A	Real-time CRC, calibration coefficients, high word
CODE_SIGTR_LWR	R	Yes	0x04	0x0C, 0x0D	N/A	Signature CRC, program code, low word
CODE_SIGTR_UPR	R	Yes	0x04	0x0E, 0x0F	N/A	Signature CRC, program code, high word
CODE_DRVTN_LWR	R	No	0x04	0x10, 0x11	N/A	Real-time CRC, program code, low word
CODE_DRVTN_UPR	R	No	0x04	0x12, 0x13	N/A	Real-time CRC, program code, high word
Reserved	N/A	N/A	0x04	0x1C to 0x1F	N/A	Reserved
SERIAL_NUM	R	Yes	0x04	0x20, 0x21	N/A	Serial number
Reserved	N/A	N/A	0x04	0x22 to 0x7F	N/A	Reserved
PAGE_ID	R/W	No	0x05	0x00, 0x01	0x0000	Page identifier
Reserved	N/A	N/A	0x05	0x02 to 0x07	N/A	Reserved
FIR_COEF_Axxx[2]	R/W	Yes	0x05	0x08 to 0x7F	N/A	FIR Filter Bank A: Coefficient 0 through Coefficient 59
PAGE_ID	R/W	No	0x06	0x00	0x0000	Page identifier
Reserved	N/A	N/A	0x06	0x02 to 0x07	N/A	Reserved
FIR_COEF_Axxx[2]	R/W	Yes	0x06	0x08 to 0x7F	N/A	FIR Filter Bank A: Coefficient 60 through Coefficient 119
PAGE_ID	R/W	No	0x07	0x00, 0x01	0x0000	Page identifier
Reserved	N/A	N/A	0x07	0x02 to 0x07	N/A	Reserved
FIR_COEF_Bxxx[3]	R/W	Yes	0x07	0x08 to 0x7F	N/A	FIR Filter Bank B: Coefficient 0 through Coefficient 59

Name	R/W	Flash Backup	PAGE_ID	Address	Default	Register Description
PAGE_ID	R/W	No	0x08	0x00, 0x01	0x0000	Page identifier
Reserved	N/A	N/A	0x08	0x02 to 0x07	N/A	Reserved
FIR_COEF_Bxxx[3]	R/W	Yes	0x08	0x08 to 0x7F	N/A	FIR Filter Bank B: Coefficient 60 through Coefficient 119
PAGE_ID	R/W	No	0x09	0x00, 0x01	0x0000	Page identifier
Reserved	N/A	N/A	0x09	0x02 to 0x07	N/A	Reserved
FIR_COEF_Cxxx[4]	R/W	Yes	0x09	0x08 to 0x7F	N/A	FIR Filter Bank C: Coefficient 0 through Coefficient 59
PAGE_ID	R/W	No	0x0A	0x00, 0x01	0x0000	Page identifier
Reserved	N/A	N/A	0x0A	0x02 to 0x07	N/A	Reserved
FIR_COEF_Cxxx[4]	R/W	Yes	0x0A	0x08 to 0x7F	N/A	FIR Filter Bank C: Coefficient 60 through Coefficient 119
PAGE_ID	R/W	No	0x0B	0x00, 0x01	0x0000	Page identifier
Reserved	N/A	N/A	0x0B	0x02 to 0x07	N/A	Reserved
FIR_COEF_Dxxx[5]	R/W	Yes	0x0B	0x08 to 0x7F	N/A	FIR Filter Bank D: Coefficient 0 through Coefficient 59
PAGE_ID	R/W	No	0x0C	0x00, 0x01	0x0000	Page identifier
Reserved	N/A	N/A	0x0C	0x02 to 0x07	N/A	Reserved
FIR_COEF_Dxxx[5]	R/W	Yes	0x0C	0x08 to 0x7F	N/A	FIR Filter Bank D: Coefficient 60 through Coefficient 119

[1] The GPIO_CTRL[7:4] bits reflect the logic levels on the DIOx lines and do not have a default setting.
[2] See the FIR Filter Bank A, FIR_COEF_A000 to FIR_COEF_A119 section for additional information.
[3] See the FIR Filter Bank B, FIR_COEF_B000 to FIR_COEF_B119 section for additional information.
[4] See the FIR Filter Bank C, FIR_COEF_C000 to FIR_COEF_C119 section for additional information.
[5] See the FIR Filter Bank D, FIR_COEF_D000 to FIR_COEF_D119 section for additional information.

USER REGISTER DEFINTIONS

Page Number (PAGE_ID)

Table 11. PAGE_ID Register Definition

Page	Addresses	Default	Access	Flash Backup
0x00	0x00, 0x01	0x0000	R/W	No

Table 12. PAGE_ID Bit Assignments

Bits	Description
[15:0]	Page number, binary numerical format

The contents in the PAGE_ID register (see Table 11 and Table 12) contain the current page setting, and provide a control for selecting another page for SPI access. For example, set DIN = 0x8002 to select Page 2 for SPI-based user access. See Table 10 for the page assignments associated with each user accessible register.

Data/Sample Counter (DATA_CNT)

Table 13. DATA_CNT Register Definition

Page	Addresses	Default	Access	Flash Backup
0x00	0x04, 0x05	Not applicable	R	No

Table 14. DATA_CNT Bit Assignments

Bits	Description
[15:0]	Data counter, binary format.

The DATA_CNT register (see Table 13 and Table 14) is a continuous, real-time, sample counter. It starts at 0x0000, increments every time that the output data registers update, and wraps around from 0xFFFF (65,535 decimal) to 0x0000 (0 decimal).

Status/Error Flag Indicators (SYS_E_FLAG)

Table 15. SYS_E_FLAG Register Definition

Page	Addresses	Default	Access	Flash Backup
0x00	0x08, 0x09	0x0000	R	No

Table 16. SYS_E_FLAG Bit Assignments

Bits	Description
15	Watch dog timer flag. A 1 indicates that the ADIS16490 automatically resets itself to clear an issue.
[14:9]	Not used.
8	Sync error. A 1 indicates that the sample timing is not scaling correctly, when operating in PPS mode (FNCTIO_CTRL[8] = 1, see Table 131). When this error occurs, verify that the input sync frequency is correct and that SYNC_SCALE (see Table 141) has the correct value.
7	Processing overrun. A 1 indicates occurrence of a processing overrun. Initiate a reset to recover. Replace the ADIS16490 if this error persists.
6	Flash memory update failure. A 1 indicates that the most recent flash memory update failed (GLOB_CMD[3], see Table 129). Repeat the test and replace the ADIS16490 if this error persists.
5	Sensor failure. A 1 indicates failure of the self test processes (GLOB_CMD[1], see Table 129), when the device is not in motion. Replace the ADIS16490 if the error persists.
4	Not used.
3	SPI communication error. A 1 indicates that the total number of SCLK cycles is not equal to an integer multiple of 16. Repeat the previous communication sequence to recover. Persistence in this error may indicate a weakness in the SPI service from the master processor.
2	SRAM error condition. A 1 indicates a failure in the CRC (period = 20 ms) between the SRAM and flash memory. Initiate a reset to recover and replace the ADIS16490 if this error persists.
1	Boot memory failure. A 1 indicates that the CRC on the primary flash memory bank did not match the reference CRC value and that the device automatically rebooted using the backup memory bank in flash. Replace the ADIS16490 if this error persists.
0	Not used.

The SYS_E_FLAG register (see Table 15 and Table 16) provides various error flags. Reading this register causes all of its bits to return to 0, with the exception of Bit 7. If an error condition persists, its flag (bit) automatically returns to an alarm value of 1.

Self Test Error Flags (DIAG_STS)

Table 17. DIAG_STS Register Definition

Page	Addresses	Default	Access	Flash Backup
0x00	0x0A, 0x0B	0x0000	R	No

Table 18. DIAG_STS Bit Definitions

Bits	Description (Default = 0x0000)
[15:6]	Not used
5	Self test failure, z-axis accelerometer (1 = failure)
4	Self test failure, y-axis accelerometer (1 = failure)
3	Self test failure, x-axis accelerometer (1 = failure)
2	Self test failure, z-axis gyroscope (1 = failure)
1	Self test failure, y-axis gyroscope (1 = failure)
0	Self test failure, x-axis gyroscope (1 = failure)

SYS_E_FLAG[5] (see Table 16) contains the pass/fail result (0 = pass) for the on demand self test (ODST) operations, whereas the DIAG_STS register (see Table 17 and Table 18) contains pass/fail flags (0 = pass) for each inertial sensor. Reading the DIAG_STS register causes all of its bits to restore to 0. The bits in DIAG_STS return to 1 if the error conditions persists.

Internal Temperature (TEMP_OUT)

Table 19. TEMP_OUT Register Definition

Page	Addresses	Default	Access	Flash Backup
0x00	0x0E, 0x0F	Not applicable	R	No

Table 20. TEMP_OUT Bit Definitions

Bits	Description
[15:0]	Temperature data; twos complement, 1°C per 70 LSB, 25°C = 0x0000

The TEMP_OUT register (see Table 19 and Table 20) provides a coarse measurement of the temperature inside of the ADIS16490 and is useful for monitoring relative changes in the thermal environment.

Table 21. TEMP_OUT Data Format Examples

Temperature (°C)	Decimal	Hex	Binary
+85	+4200	0x1068	0001 0000 0110 1000
+25 + 2/70	+2	0x0002	0000 0000 0000 0010
+25 + 1/70	+1	0x0001	0000 0000 0000 0001
+25	0	0x0000	0000 0000 0000 0000
+25 – 1/70	−1	0xFFFF	1111 1111 1111 1111
+25 – 2/70	−2	0xFFFE	1111 1111 1111 1110
−40	−4550	0xEE3A	1110 1110 0011 1010

GYROSCOPE DATA

The gyroscopes in the ADIS16490 measure the angular rate of rotation around three orthogonal axes (x, y, and z). Figure 38 illustrates the orientation of each gyroscope axis, along with the direction of rotation that produces a positive response in each of their measurements.

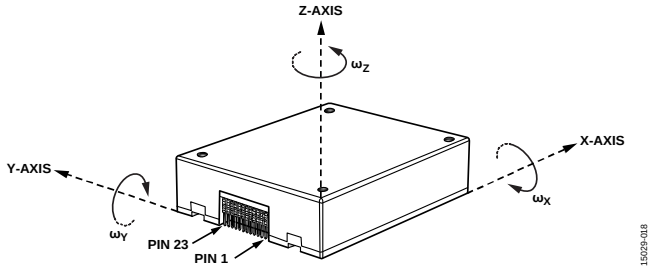

Figure 38. Gyroscope Axis and Polarity Assignments

Each gyroscope has two output data registers. Figure 39 illustrates how these two registers combine to support a 32-bit, twos complement data format for the x-axis gyroscope measurements. This format also applies to the y-axis and z-axis as well.

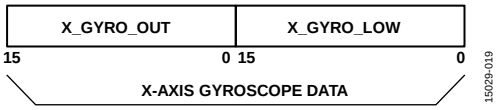

Figure 39. Gyroscope Output Data Structure

X-Axis Gyroscope (X_GYRO_LOW, X_GYRO_OUT)

Table 22. X_GYRO_LOW Register Definition

Page	Addresses	Default	Access	Flash Backup
0x00	0x10, 0x11	Not applicable	R	No

Table 23. X_GYRO_LOW Bit Definitions

Bits	Description
[15:0]	X-axis gyroscope data; low word

Table 24. X_GYRO_OUT Register Definition

Page	Addresses	Default	Access	Flash Backup
0x00	0x12, 0x13	Not applicable	R	No

Table 25. X_GYRO_OUT Bit Definitions

Bits	Description
[15:0]	X-axis gyroscope data; high word; twos complement, ±100°/sec range; 0°/sec = 0x0000, 1 LSB = 0.005°/sec

The X_GYRO_LOW (see Table 22 and Table 23) and X_GYRO_OUT (see Table 24 and Table 25) registers contain the gyroscope data for the x-axis.

Y-Axis Gyroscope (Y_GYRO_LOW, Y_GYRO_OUT)

Table 26. Y_GYRO_LOW Register Definition

Page	Addresses	Default	Access	Flash Backup
0x00	0x14, 0x15	Not applicable	R	No

Table 27. Y_GYRO_LOW Bit Definitions

Bits	Description
[15:0]	Y-axis gyroscope data; low word

Table 28. Y_GYRO_OUT Register Definition

Page	Addresses	Default	Access	Flash Backup
0x00	0x16, 0x17	Not applicable	R	No

Table 29. Y_GYRO_OUT Bit Definitions

Bits	Description
[15:0]	Y-axis gyroscope data; high word; twos complement, ±100°/sec range; 0°/sec = 0x0000, 1 LSB = 0.005°/sec

The Y_GYRO_LOW (see Table 26 and Table 27) and Y_GYRO_OUT (see Table 28 and Table 29) registers contain the gyroscope data for the y-axis.

Z-Axis Gyroscope (Z_GYRO_LOW, Z_GYRO_OUT)

Table 30. Z_GYRO_LOW Register Definition

Page	Addresses	Default	Access	Flash Backup
0x00	0x18, 0x19	Not applicable	R	No

Table 31. Z_GYRO_LOW Bit Definitions

Bits	Description
[15:0]	Z-axis gyroscope data; additional resolution bits

Table 32. Z_GYRO_OUT Register Definition

Page	Addresses	Default	Access	Flash Backup
0x00	0x1A, 0x1B	Not applicable	R	No

Table 33. Z_GYRO_OUT Bit Definitions

Bits	Description
[15:0]	Z-axis gyroscope data; high word; twos complement, ±100°/sec range; 0°/sec = 0x0000, 1 LSB = 0.005°/sec

The Z_GYRO_LOW (see Table 30 and Table 31) and Z_GYRO_OUT (see Table 32 and Table 33) registers contain the gyroscope data for the z-axis.

Gyroscope Resolution

Table 34 and Table 35 offer various numerical examples that demonstrate the format of the angular rate (gyroscopes) data in both 16-bit and 32-bit formats.

Table 34. 16-Bit Gyroscope Data Format Examples

Rotation Rate (°/sec)	Decimal	Hex	Binary
+100	+20,000	0x4E20	0100 1110 0010 0000
+0.01	+2	0x0002	0000 0000 0000 0010
+0.005	+1	0x0001	0000 0000 0000 0001
0	0	0x0000	0000 0000 0000 0000
−0.005	−1	0xFFFF	1111 1111 1111 1111
−0.01	−2	0xFFFE	1111 1111 1111 1110
−100	−20,000	0xB1E0	1011 0001 1110 0000

Table 35. 32-Bit Gyroscope Data Format Examples

Rotation Rate (°/sec)	Decimal	Hex
+100	+1,310,720,000	0x4E200000
$+0.005/2^{15}$	+2	0x00000002
$+0.005/2^{16}$	+1	0x00000001
0	0	0x0000000
$-0.005/2^{16}$	−1	0xFFFFFFFF
$-0.005/2^{15}$	−2	0xFFFFFFFE
−100	−1,310,720,000	0xB1E00000

ACCELERATION DATA

The accelerometers in the ADIS16490 measure both dynamic and static (response to gravity) acceleration along three orthogonal axes (x, y, and z). Figure 40 illustrates the orientation of each accelerometer axis, along with the direction of acceleration that produces a positive response in each of their measurements.

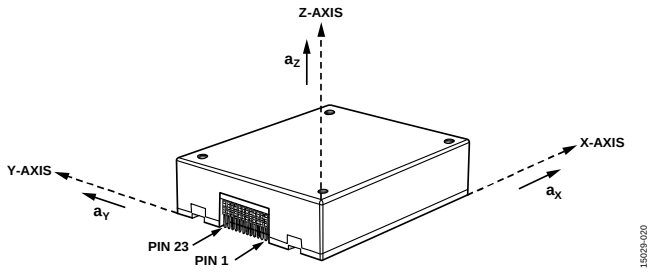

Figure 40. Accelerometer Axis and Polarity Assignments

Each accelerometer has two output data registers. Figure 41 illustrates how these two registers combine to support a 32-bit, twos complement data format for the x-axis accelerometer measurements. This format also applies to the y- and z-axes.

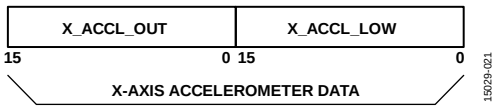

Figure 41. Accelerometer Output Data Structure

X-Axis Accelerometer (X_ACCL_LOW, X_ACCL_OUT)

Table 36. X_ACCL_LOW Register Definition

Page	Addresses	Default	Access	Flash Backup
0x00	0x1C, 0x1D	Not applicable	R	No

Table 37. X_ACCL_LOW Bit Definitions

Bits	Description
[15:0]	X-axis accelerometer data; low word

Table 38. X_ACCL_OUT Register Definition

Page	Addresses	Default	Access	Flash Backup
0x00	0x1E, 0x1F	Not applicable	R	No

Table 39. X_ACCL_OUT Definitions

Bits	Description
[15:0]	X-axis accelerometer data, high word; twos complement, ±8 *g* range; 0 *g* = 0x0000, 1 LSB = 0.5 m*g*

The X_ACCL_LOW (see Table 36 and Table 37) and X_ACCL_OUT (see Table 38 and Table 39) registers contain the accelerometer data for the x-axis.

Y-Axis Accelerometer (Y_ACCL_LOW, Y_ACCL_OUT)

Table 40. Y_ACCL_LOW Register Definition

Page	Addresses	Default	Access	Flash Backup
0x00	0x20, 0x21	Not applicable	R	No

Table 41. Y_ACCL_LOW Bit Definitions

Bits	Description
[15:0]	Y-axis accelerometer data; low word

Table 42. Y_ACCL_OUT Register Definition

Page	Addresses	Default	Access	Flash Backup
0x00	0x22, 0x23	Not applicable	R	No

Table 43. Y_ACCL_OUT Bit Definitions

Bits	Description
[15:0]	Y-axis accelerometer data, high word; twos complement, ±8 *g* range, 0 *g* = 0x0000, 1 LSB = 0.5 m*g*

The Y_ACCL_LOW (see Table 40 and Table 41) and Y_ACCL_OUT (see Table 42 and Table 43) registers contain the accelerometer data for the y-axis.

Z-Axis Accelerometer (Z_ACCL_LOW, Z_ACCL_OUT)

Table 44. Z_ACCL_LOW Register Definition

Page	Addresses	Default	Access	Flash Backup
0x00	0x24, 0x25	Not applicable	R	No

Table 45. Z_ACCL_LOW Bit Definitions

Bits	Description
[15:0]	Z-axis accelerometer data; low word

Table 46. Z_ACCL_OUT Register Definition

Page	Addresses	Default	Access	Flash Backup
0x00	0x26, 0x27	Not applicable	R	No

Table 47. Z_ACCL_OUT Bit Definitions

Bits	Description
[15:0]	Z-axis accelerometer data, high word; twos complement, ±8 *g* range; 0 *g* = 0x0000, 1 LSB = 0.5 m*g*

The Z_ACCL_LOW (see Table 44 and Table 45) and Z_ACCL_OUT (see Table 46 and Table 47) registers contain the accelerometer data for the z-axis.

Accelerometer Resolution

Table 48 and Table 49 offer various numerical examples that demonstrate the format of the linear acceleration data in both 16-bit and 32-bit formats.

Table 48. 16-Bit Accelerometer Data Format Examples

Acceleration	Decimal	Hex	Binary
+8 *g*	+16,000	0x3E80	0011 1110 1000 0000
+1.0 m*g*	+2	0x0002	0000 0000 0000 0010
+0.5 m*g*	+1	0x0001	0000 0000 0000 0001
0 m*g*	0	0x0000	0000 0000 0000 0000
−0.5 m*g*	−1	0xFFFF	1111 1111 1111 1111
−1.0 m*g*	−2	0xFFFE	1111 1111 1111 1110
−8 *g*	−16,000	0xC180	1100 0001 1000 0000

Table 49. 32-Bit Accelerometer Data Format Examples

Acceleration	Decimal	Hex
+8 *g*	+1,048,576,000	0x3E800000
+0.1/2^{15} m*g*	+2	0x00000002
+0.5/2^{16} m*g*	+1	0x00000001
0 m*g*	0	0x00000000
−0.5/2^{16} m*g*	−1	0xFFFFFFFF
−0.1/2^{15} m*g*	−2	0xFFFFFFFE
−8 *g*	−1,048,576,000	0xC1800000

DELTA ANGLES

In addition to the angular rate of rotation (gyroscope) measurements around each axis (x, y, and z), the ADIS16490 also provides delta angle measurements that represent a computation of angular displacement between each sample update.

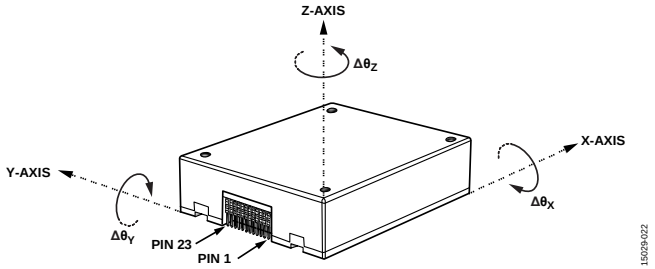

Figure 42. Delta Angle Axis and Polarity Assignments

The delta angle outputs represent an integration of the gyroscope measurements and use the following formula for all three axes (x-axis displayed):

$$\Delta\theta_{x,nD} = \frac{1}{2f_S} \times \sum_{d=0}^{D-1} \left(\omega_{x,nD+d} + \omega_{x,nD+d-1} \right)$$

where:
D is the decimation rate = DEC_RATE + 1 (see Table 137).
f_S is the sample rate.
d is the incremental variable in the summation formula.
ω_x is the x-axis rate of rotation (gyroscope).
n is the sample time, prior to the decimation filter.

When using the internal sample clock, f_S is equal to 4250 SPS. When using the external clock option, f_S is equal to the frequency of the external clock. The range in the delta angle registers accommodates the maximum rate of rotation (100°/sec), the nominal sample rate (4250 SPS) and an update rate of 1 Hz (DEC_RATE = 0x1099; divide by 4249 plus 1, see Table 137), all at the same time. When using an external clock that is higher than 4250 SPS, reduce the DEC_RATE setting to avoid overranging the delta angle registers.

Each axis of the delta angle measurements has two output data registers. Figure 43 illustrates how these two registers combine to support a 32-bit, twos complement data format for the x-axis delta angle measurements. This format also applies to the y- and z-axes.

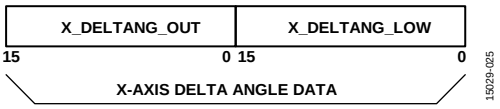

Figure 43. Delta Angle Output Data Structure

X-Axis Delta Angle (X_DELTANG_LOW, X_DELTANG_OUT)

The X_DELTANG_LOW (see Table 50 and Table 51) and X_DELTANG_OUT (see Table 52 and Table 53) registers contain the delta angle data for the x-axis.

Table 50. X_DELTANG_LOW Register Definitions

Page	Addresses	Default	Access	Flash Backup
0x00	0x40, 0x41	Not applicable	R	No

Table 51. X_DELTANG_LOW Bit Definitions

Bits	Description
[15:0]	X-axis delta angle data; low word

Table 52. X_DELTANG_OUT Register Definitions

Page	Addresses	Default	Access	Flash Backup
0x00	0x42, 0x43	Not applicable	R	No

Table 53. X_DELTANG_OUT Bit Definitions

Bits	Description
[15:0]	X-axis delta angle data, high word; twos complement, ±720° range, 0° = 0x0000, 1 LSB = 720°/2^{15} = ~0.022°

Y-Axis Delta Angle (Y_DELTANG_LOW, Y_DELTANG_OUT)

The Y_DELTANG_LOW (see Table 54 and Table 55) and Y_DELTANG_OUT (see Table 56 and Table 57) registers contain the delta angle data for the y-axis.

Table 54. Y_DELTANG_LOW Register Definitions

Page	Addresses	Default	Access	Flash Backup
0x00	0x44, 0x45	Not applicable	R	No

Table 55. Y_DELTANG_LOW Bit Definitions

Bits	Description
[15:0]	Y-axis delta angle data; low word

Table 56. Y_DELTANG_OUT Register Definitions

Page	Addresses	Default	Access	Flash Backup
0x00	0x46, 0x47	Not applicable	R	No

Table 57. Y_DELTANG_OUT Bit Definitions

Bits	Description
[15:0]	Y-axis delta angle data, high word; twos complement, ±720° range, 0° = 0x0000, 1 LSB = 720°/2^{15} = ~0.022°

Z-Axis Delta Angle (Z_DELTANG_LOW, Z_DELTANG_OUT)

The Z_DELTANG_LOW (see Table 58 and Table 59) and Z_DELTANG_OUT (see Table 60 and Table 61) registers contain the delta angle data for the z-axis.

Table 58. Z_DELTANG_LOW Register Definitions

Page	Addresses	Default	Access	Flash Backup
0x00	0x48, 0x49	Not applicable	R	No

Table 59. Z_DELTANG_LOW Bit Definitions

Bits	Description
[15:0]	Z-axis delta angle data; low word

Table 60. Z_DELTANG_OUT Register Definitions

Page	Addresses	Default	Access	Flash Backup
0x00	0x4A, 0x4B	Not applicable	R	No

Table 61. Z_DELTANG_OUT Bit Definitions

Bits	Description
[15:0]	Z-axis delta angle data, high word; twos complement, ±720° range, 0° = 0x0000, 1 LSB = 720°/2^{15} = ~0.022°

Delta Angle Resolution

Table 62 and Table 63 offer various numerical examples that demonstrate the format of the delta angle data in both 16-bit and 32-bit formats.

Table 62. 16-Bit Delta Angle Data Format Examples

Delta Angle (°)	Decimal	Hex	Binary
+720 × (2^{15} − 1)/2^{15}	+32,767	0x7FFF	0111 1111 1110 1111
+720/2^{14}	+2	0x0002	0000 0000 0000 0010
+720/2^{15}	+1	0x0001	0000 0000 0000 0001
0	0	0x0000	0000 0000 0000 0000
−720/2^{15}	−1	0xFFFF	1111 1111 1111 1111
−720/2^{14}	−2	0xFFFE	1111 1111 1111 1110
−720	−32,768	0x8000	1000 0000 0000 0000

Table 63. 32-Bit Delta Angle Data Format Examples

Delta Angle (°)	Decimal	Hex
+720 × (2^{31} − 1)/2^{31}	+2,147,483,647	0x7FFFFFFF
+720/2^{30}	+2	0x00000002
+720/2^{31}	+1	0x00000001
0	0	0x00000000
−720/2^{31}	−1	0xFFFFFFFF
−720/2^{30}	−2	0xFFFFFFFE
−720	−2,147,483,647	0x80000000

DELTA VELOCITY

In addition to the linear acceleration measurements along each axis (x, y, and z), the ADIS16490 also provides delta velocity measurements that represent a computation of linear velocity change between each sample update.

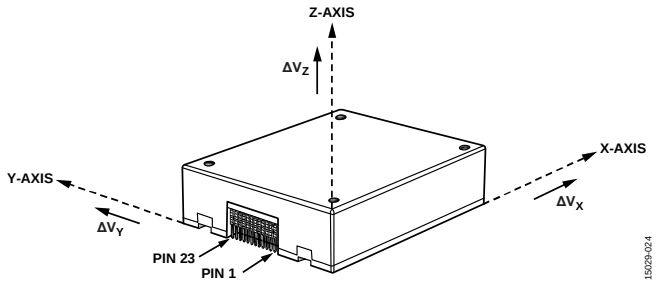

Figure 44. Delta Velocity Axis and Polarity Assignments

The delta velocity outputs represent an integration of the acceleration measurements and use the following formula for all three axes (x-axis displayed):

$$\Delta V_{x,nD} = \frac{1}{2f_S} \times \sum_{d=0}^{D-1} \left(a_{x,nD+d} + a_{x,nD+d-1} \right)$$

where:
D is the decimation rate = DEC_RATE + 1 (see Table 137).
f_S is the sample rate.
d is the incremental variable in the summation formula.
a_x is the x-axis rate of acceleration (accelerometer).
n is the sample time, prior to the decimation filter.

When using the internal sample clock, f_S is equal to 4250 SPS. When using the external clock option, f_S is equal to the frequency of the external clock. The range in the delta velocity registers accommodates the maximum linear acceleration (8 *g*), the nominal sample rate (4250 SPS) and an update rate of 1 Hz (DEC_RATE = 0x1099; divide by 4249 plus 1, see Table 137), all at the same time. When using an external clock that is higher than 4250 SPS, reduce the DEC_RATE setting to avoid overranging the delta velocity registers.

Each axis of the delta velocity measurements has two output data registers. Figure 45 illustrates how these two registers combine to support 32-bit, twos complement data format for the delta velocity measurements along the x-axis. This format also applies to the y- and x-axes.

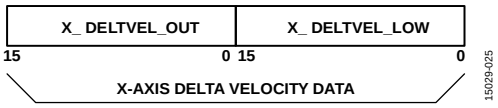

Figure 45. Delta Angle Output Data Structure

X-Axis Delta Velocity (X_DELTVEL_LOW, X_DELTVEL_OUT)

Table 64. X_DELTVEL_LOW Register Definitions

Page	Addresses	Default	Access	Flash Backup
0x00	0x4C, 0x4D	Not applicable	R	No

Table 65. X_DELTVEL_LOW Bit Definitions

Bits	Description
[15:0]	X-axis delta angle data; low word

Table 66. X_DELTVEL_OUT Register Definitions

Page	Addresses	Default	Access	Flash Backup
0x00	0x4E, 0x4F	Not applicable	R	No

Table 67. X_DELTVEL_OUT Bit Definitions

Bits	Description
[15:0]	X-axis delta velocity data; twos complement, ±200 m/sec range, 0 m/sec = 0x0000; 1 LSB = 200 m/sec ÷ 2^{15} = ~6.104 mm/sec

The X_DELTVEL_LOW (see Table 64 and Table 65) and X_DELTVEL_OUT (see Table 66 and Table 67) registers contain the delta velocity data for the x-axis.

Y-Axis Delta Velocity (Y_DELTVEL_LOW, Y_DELTVEL_OUT)

Table 68. Y_DELTVEL_LOW Register Definitions

Page	Addresses	Default	Access	Flash Backup
0x00	0x50, 0x51	Not applicable	R	No

Table 69. Y_DELTVEL_LOW Bit Definitions

Bits	Description
[15:0]	Y-axis delta angle data; low word

Table 70. Y_DELTVEL_OUT Register Definitions

Page	Addresses	Default	Access	Flash Backup
0x00	0x52, 0x53	Not applicable	R	No

Table 71. Y_DELTVEL_OUT Bit Definitions

Bits	Description
[15:0]	Y-axis delta velocity data, high word; twos complement, ±200 m/sec range, 0 m/sec = 0x0000; 1 LSB = 200 m/sec ÷ 2^{15} = ~6.104 mm/sec

The Y_DELTVEL_LOW (see Table 68 and Table 69) and Y_DELTVEL_OUT (see Table 70 and Table 71) registers contain the delta velocity data for the y-axis.

Z-Axis Delta Velocity (Z_DELTVEL_LOW, Z_DELTVEL_OUT)

Table 72. Z_DELTVEL_LOW Register Definitions

Page	Addresses	Default	Access	Flash Backup
0x00	0x54, 0x55	Not applicable	R	No

Table 73. Z_DELTVEL_LOW Bit Definitions

Bits	Description
[15:0]	Z-axis delta angle data; low word

Table 74. Z_DELTVEL_OUT Register Definitions

Page	Addresses	Default	Access	Flash Backup
0x00	0x56, 0x57	Not applicable	R	No

Table 75. Z_DELTVEL_OUT Bit Definitions

Bits	Description
[15:0]	Z-axis delta velocity data, high word; twos complement, ±200 m/sec range, 0 m/sec = 0x0000; 1 LSB = 200 m/sec ÷ 2^{15} = ~6.104 mm/sec

The Z_DELTVEL_LOW (see Table 72 and Table 73) and Z_DELTVEL_OUT (see Table 74 and Table 75) registers contain the delta velocity data for the z-axis.

Delta Velocity Resolution

Table 76 and Table 77 offer various numerical examples that demonstrate the format of the delta angle data in both 16-bit and 32-bit formats.

Table 76. 16-Bit Delta Velocity Data Format Examples

Velocity (m/sec)	Decimal	Hex	Binary
+200 × (2^{15} – 1)/2^{15}	+32,767	0x7FFF	0111 1111 1110 1111
+200/2^{14}	+2	0x0002	0000 0000 0000 0010
+200/2^{15}	+1	0x0001	0000 0000 0000 0001
0	0	0x0000	0000 0000 0000 0000

Velocity (m/sec)	Decimal	Hex	Binary
$-200/2^{15}$	−1	0xFFFF	1111 1111 1111 1111
$-200/2^{14}$	−2	0xFFFE	1111 1111 1111 1110
−200	−32,768	0x8000	1000 0000 0000 0000

Table 77. 32-Bit Delta Angle Data Format Examples

Velocity (m/sec)	Decimal	Hex
$+200 \times (2^{31} - 1)/2^{31}$	+2,147,483,647	0x7FFFFFFF
$+200/2^{30}$	+2	0x00000002
$+200/2^{31}$	+1	0x00000001
0	0	0x00000000
$-200/2^{31}$	−1	0xFFFFFFFF
$-200/2^{30}$	−2	0xFFFFFFFE
−200	−2,147,483,648	0x80000000

Product Identification, PROD_ID

Table 78. PROD_ID Register Definitions

Page	Addresses	Default	Access	Flash Backup
0x00	0x7E, 0x7F	0x406A	R	Yes

Table 79. PROD_ID Bit Definitions

Bits	Description
[15:0]	Product identification = 0x406A

The PROD_ID register (see Table 78 and Table 79) contains the numerical portion of the part number (16490). See Figure 35 for an example of how to use a looping read of this register to validate the integrity of the communication.

CALIBRATION

The signal chain of each inertial sensor (accelerometers, gyroscopes) includes application of unique correction formulas that come from extensive characterization of bias, sensitivity, alignment, and response to linear acceleration (gyroscopes) over a temperature range of −40°C to +85°C for the ADIS16490. These correction formulas are not accessible, but users do have the opportunity to adjust the bias and the scale factor, for each sensor individually, through user accessible registers. These correction factors follow immediately after the factory derived correction formulas in the signal chain, which processes at a rate of 4250 Hz when using the internal sample clock (see f_{SM} in Figure 23 and Figure 24).

Calibration, Gyroscope Scale, X_GYRO_SCALE

Table 80. X_GYRO_SCALE Register Definitions

Page	Addresses	Default	Access	Flash Backup
0x02	0x04, 0x05	0x0000	R/W	Yes

Table 81. X_GYRO_SCALE Bit Definitions

Bits	Description
[15:0]	X-axis gyroscope scale correction; twos complement, 0x0000 = unity gain, 1 LSB = $1 \div 2^{15}$ = ~0.003052%

The X_GYRO_SCALE register (see Table 80 and Table 81) provides users with the opportunity to adjust the scale factor for the x-axis gyroscopes. See Figure 46 for an illustration of how this scale factor influences the x-axis gyroscope data.

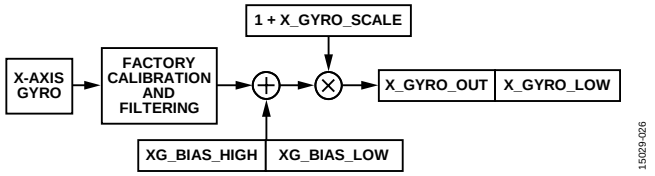

Figure 46. User Calibration Signal Path, Gyroscopes

Calibration, Gyroscope Scale, Y_GYRO_SCALE

Table 82. Y_GYRO_SCALE Register Definitions

Page	Addresses	Default	Access	Flash Backup
0x02	0x06, 0x07	0x0000	R/W	Yes

Table 83. Y_GYRO_SCALE Bit Definitions

Bits	Description
[15:0]	Y-axis gyroscope scale correction; twos complement, 0x0000 = unity gain, 1 LSB = $1 \div 2^{15}$ = ~0.003052%

The Y_GYRO_SCALE register (see Table 82 and Table 83) allows users to adjust the scale factor for the y-axis gyroscopes. This register influences the y-axis gyroscope measurements in the same manner that X_GYRO_SCALE influences the x-axis gyroscope measurements (see Figure 46).

Calibration, Gyroscope Scale, Z_GYRO_SCALE

Table 84. Z_GYRO_SCALE Register Definitions

Page	Addresses	Default	Access	Flash Backup
0x02	0x08, 0x09	0x0000	R/W	Yes

Table 85. Z_GYRO_SCALE Bit Definitions

Bits	Description
[15:0]	Z-axis gyroscope scale correction; twos complement, 0x0000 = unity gain, 1 LSB = $1 \div 2^{15}$ = ~0.003052%

The Z_GYRO_SCALE register (see Table 84 and Table 85) allows users to adjust the scale factor for the z-axis gyroscopes. This register influences the z-axis gyroscope measurements in the same manner that X_GYRO_SCALE influences the x-axis gyroscope measurements (see Figure 46).

Calibration, Accelerometer Scale, X_ACCL_SCALE

Table 86. X_ACCL_SCALE Register Definitions

Page	Addresses	Default	Access	Flash Backup
0x02	0x0A, 0x0B	0x0000	R/W	Yes

Table 87. X_ACCL_SCALE Bit Definitions

Bits	Description
[15:0]	X-axis accelerometer scale correction; twos complement, 0x0000 = unity gain, 1 LSB = $1 \div 2^{15}$ = ~0.003052%

The X_ACCL_SCALE register (see Table 86 and Table 87) allows users to adjust the scale factor for the x-axis accelerometers. See Figure 47 for an illustration of how this scale factor influences the x-axis accelerometer data.

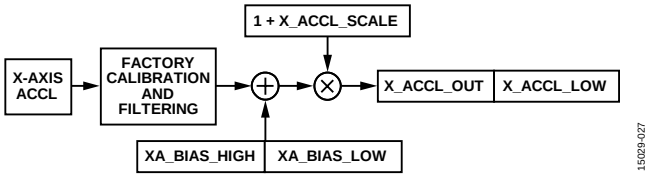

Figure 47. User Calibration Signal Path, Accelerometers

Calibration, Accelerometer Scale, Y_ACCL_SCALE

Table 88. Y_ACCL_SCALE Register Definitions

Page	Addresses	Default	Access	Flash Backup
0x02	0x0C, 0x0D	0x0000	R/W	Yes

Table 89. Y_ACCL_SCALE Bit Definitions

Bits	Description
[15:0]	Y-axis accelerometer scale correction; twos complement, 0x0000 = unity gain, 1 LSB = $1 \div 2^{15}$ = ~0.003052%

The Y_ACCL_SCALE register (see Table 88 and Table 89) allows users to adjust the scale factor for the y-axis accelerometers. This register influences the y-axis accelerometer measurements in the same manner that X_ACCL_SCALE influences the x-axis accelerometer measurements (see Figure 47).

Calibration, Accelerometer Scale, Z_ACCL_SCALE

Table 90. Z_ACCL_SCALE Register Definitions

Page	Addresses	Default	Access	Flash Backup
0x02	0x0E, 0x0F	0x0000	R/W	Yes

Table 91. Z_ACCL_SCALE Bit Definitions

Bits	Description
[15:0]	Z-axis accelerometer scale correction; twos complement, 0x0000 = unity gain, 1 LSB = $1 \div 2^{15}$ = ~0.003052%

The Z_ACCL_SCALE register (see Table 90 and Table 91) allows users to adjust the scale factor for the z-axis accelerometers. This register influences the z-axis accelerometer measurements in the same manner that X_ACCL_SCALE influences the x-axis accelerometer measurements (see Figure 47).

Calibration, Gyroscope Bias, XG_BIAS_LOW, XG_BIAS_HIGH

Table 92. XG_BIAS_LOW Register Definitions

Page	Addresses	Default	Access	Flash Backup
0x02	0x10, 0x11	0x0000	R/W	Yes

Table 93. XG_BIAS_LOW Bit Definitions

Bits	Description
[15:0]	X-axis gyroscope offset correction, low word; twos complement, 0°/sec = 0x0000, 1 LSB = 0.005°/sec $\div 2^{16}$

Table 94. XG_BIAS_HIGH Register Definitions

Page	Addresses	Default	Access	Flash Backup
0x02	0x12, 0x13	0x0000	R/W	Yes

Table 95. XG_BIAS_HIGH Bit Definitions

Bits	Description
[15:0]	X-axis gyroscope offset correction, high word; twos complement, 0°/sec = 0x0000, 1 LSB = 0.005°/sec

The XG_BIAS_LOW (see Table 92 and Table 93) and XG_BIAS_HIGH (see Table 94 and Table 95) registers combine to allow users to adjust the bias of the x-axis gyroscopes. The digital format examples in Table 34 also apply to the XG_BIAS_HIGH register, and the digital format examples in Table 35 apply to the number that comes from combining the XG_BIAS_LOW and XG_BIAS_HIGH registers. See Figure 46 for an illustration of how these two registers combine and influence the x-axis gyroscope measurements.

Calibration, Gyroscope Bias, YG_BIAS_LOW, YG_BIAS_HIGH

Table 96. YG_BIAS_LOW Register Definitions

Page	Addresses	Default	Access	Flash Backup
0x02	0x14, 0x15	0x0000	R/W	Yes

Table 97. YG_BIAS_LOW Bit Definitions

Bits	Description
[15:0]	Y-axis gyroscope offset correction, low word; twos complement, 0°/sec = 0x0000, 1 LSB = 0.005°/sec $\div 2^{16}$

Table 98. YG_BIAS_HIGH Register Definitions

Page	Addresses	Default	Access	Flash Backup
0x02	0x16, 0x17	0x0000	R/W	Yes

Table 99. YG_BIAS_HIGH Bit Definitions

Bits	Description
[15:0]	Y-axis gyroscope offset correction, high word; twos complement, 0°/sec = 0x0000, 1 LSB = 0.005°/sec

The YG_BIAS_LOW (see Table 96 and Table 97) and YG_BIAS_HIGH (see Table 98 and Table 99) registers combine to allow users to adjust the bias of the y-axis gyroscopes. The digital format examples in Table 34 also apply to the YG_BIAS_HIGH register, and the digital format examples in Table 35 apply to the number that comes from combining the YG_BIAS_LOW and YG_BIAS_HIGH registers. These registers influences the y-axis gyroscope measurements in the same manner that the XG_BIAS_LOW and XG_BIAS_HIGH registers influence the x-axis gyroscope measurements (see Figure 46).

Calibration, Gyroscope Bias, ZG_BIAS_LOW, ZG_BIAS_HIGH

Table 100. ZG_BIAS_LOW Register Definitions

Page	Addresses	Default	Access	Flash Backup
0x02	0x18, 0x19	0x0000	R/W	Yes

Table 101. ZG_BIAS_LOW Bit Definitions

Bits	Description
[15:0]	Z-axis gyroscope offset correction, low word; twos complement, 0°/sec = 0x0000, 1 LSB = 0.005°/sec $\div 2^{16}$

Table 102. ZG_BIAS_HIGH Register Definitions

Page	Addresses	Default	Access	Flash Backup
0x02	0x1A, 0x1B	0x0000	R/W	Yes

Table 103. ZG_BIAS_HIGH Bit Definitions

Bits	Description
[15:0]	Z-axis gyroscope offset correction, high word twos complement, 0°/sec = 0x0000, 1 LSB = 0.005°/sec

The ZG_BIAS_LOW (see Table 100 and Table 101) and ZG_BIAS_HIGH (see Table 102 and Table 103) registers combine to allow users to adjust the bias of the z-axis gyroscopes. The digital format examples in Table 34 also apply to the ZG_BIAS_HIGH register, and the digital format examples in Table 35 apply to the number that comes from combining the ZG_BIAS_LOW and ZG_BIAS_HIGH registers. These registers influence the z-axis gyroscope measurements in the same manner that the XG_BIAS_LOW and XG_BIAS_HIGH registers influence the x-axis gyroscope measurements (see Figure 46).

Calibration, Accelerometer Bias, XA_BIAS_LOW, XA_BIAS_HIGH

Table 104. XA_BIAS_LOW Register Definitions

Page	Addresses	Default	Access	Flash Backup
0x02	0x1C, 0x1D	0x0000	R/W	Yes

Table 105. XA_BIAS_LOW Bit Definitions

Bits	Description
[15:0]	X-axis accelerometer offset correction, low word, twos complement, 0 *g* = 0x0000, 1 LSB = 0.5 m*g* ÷ 2^{16}

Table 106. XA_BIAS_HIGH Register Definitions

Page	Addresses	Default	Access	Flash Backup
0x02	0x1E, 0x1F	0x0000	R/W	Yes

Table 107. XA_BIAS_HIGH Bit Definitions

Bits	Description
[15:0]	X-axis accelerometer offset correction, high word, twos complement, 0 *g* = 0x0000, 1 LSB = 0.5 m*g*

The XA_BIAS_LOW (see Table 104 and Table 105) and XA_BIAS_HIGH (see Table 106 and Table 107) registers combine to allow users to adjust the bias of the x-axis accelerometers. The digital format examples in Table 48 also apply to the XA_BIAS_HIGH register and the digital format examples in Table 49 apply to the number that comes from combining the XA_BIAS_LOW and XA_BIAS_HIGH registers. See Figure 47 for an illustration of how these two registers combine and influence the x-axis gyroscope measurements.

Calibration, Accelerometer Bias, YA_BIAS_LOW, YA_BIAS_HIGH

Table 108. YA_BIAS_LOW Register Definitions

Page	Addresses	Default	Access	Flash Backup
0x02	0x20, 0x21	0x0000	R/W	Yes

Table 109. YA_BIAS_LOW Bit Definitions

Bits	Description
[15:0]	Y-axis accelerometer offset correction, low word, twos complement, 0 *g* = 0x0000, 1 LSB = 0.5 m*g* ÷ 2^{16}

Table 110. YA_BIAS_HIGH Register Definitions

Page	Addresses	Default	Access	Flash Backup
0x02	0x22, 0x23	0x0000	R/W	Yes

Table 111. YA_BIAS_HIGH Bit Definitions

Bits	Description
[15:0]	Y-axis accelerometer offset correction, high word, twos complement, 0 *g* = 0x0000, 1 LSB = 0.5 m*g*

The YA_BIAS_LOW (see Table 108 and Table 109) and YA_BIAS_HIGH (see Table 110 and Table 111) registers combine to allow users to adjust the bias of the y-axis accelerometers. The digital format examples in Table 48 also apply to the YA_BIAS_HIGH register, and the digital format examples in Table 49 apply to the number that comes from combining the YA_BIAS_LOW and YA_BIAS_HIGH registers. These registers influence the y-axis accelerometer measurements in the same manner that the XA_BIAS_LOW and XA_BIAS_HIGH registers influence the x-axis accelerometer measurements (see Figure 47).

Calibration, Accelerometer Bias, ZA_BIAS_LOW, ZA_BIAS_HIGH

Table 112. ZA_BIAS_LOW Register Definitions

Page	Addresses	Default	Access	Flash Backup
0x02	0x24, 0x25	0x0000	R/W	Yes

Table 113. ZA_BIAS_LOW Bit Definitions

Bits	Description
[15:0]	Z-axis accelerometer offset correction, low word, twos complement, 0 *g* = 0x0000, 1 LSB = 0.5 m*g* ÷ 2^{16}

Table 114. ZA_BIAS_HIGH Register Definitions

Page	Addresses	Default	Access	Flash Backup
0x02	0x26, 0x27	0x0000	R/W	Yes

Table 115. ZA_BIAS_HIGH Bit Definitions

Bits	Description
[15:0]	Z-axis accelerometer offset correction, high word, twos complement, 0 *g* = 0x0000, 1 LSB = 0.5 m*g*

The ZA_BIAS_LOW (see Table 112 and Table 113) and ZA_BIAS_HIGH (see Table 114 and Table 115) registers combine to allow users to adjust the bias of the z-axis accelerometers. The digital format examples in Table 48 also apply to the ZA_BIAS_ HIGH register and the digital format examples in Table 49 apply to the number that comes from combining the ZA_BIAS_LOW and ZA_BIAS_HIGH registers. These registers influence the z-axis accelerometer measurements in the same manner that the XA_BIAS_LOW and XA_BIAS_HIGH registers influence the x-axis accelerometer measurements (see Figure 47).

Scratch Registers, USER_SCR_x

Table 116. USER_SCR_1 Register Definitions

Page	Addresses	Default	Access	Flash Backup
0x02	0x74, 0x75	0x0000	R/W	Yes

Table 117. USER_SCR_1 Bit Definitions

Bits	Description
[15:0]	User defined

Table 118. USER_SCR_2 Register Definitions

Page	Addresses	Default	Access	Flash Backup
0x02	0x76, 0x77	0x0000	R/W	Yes

Table 119. USER_SCR_2 Bit Definitions

Bits	Description
[15:0]	User defined

Table 120. USER_SCR_3 Register Definitions

Page	Addresses	Default	Access	Flash Backup
0x02	0x78, 0x79	0x0000	R/W	Yes

Table 121. USER_SCR_3 Bit Definitions

Bits	Description
[15:0]	User defined

Table 122. USER_SCR_4 Register Definitions

Page	Addresses	Default	Access	Flash Backup
0x02	0x7A, 0x7B	0x0000	R/W	Yes

Table 123. USER_SCR_4 Bit Definitions

Bits	Description
[15:0]	User defined

The USER_SCR_1 (see Table 116 and Table 117), USER_SCR_2 (see Table 118 and Table 119), USER_SCR_3 (see Table 120 and Table 121), USER_SCR_4 (see Table 122 and Table 123) registers provide four locations for users to store information.

Flash Memory Endurance Counter, FLSHCNT_LOW, FLSHCNT_HIGH

Table 124. FLSHCNT_LOW Register Definitions

Page	Addresses	Default	Access	Flash Backup
0x02	0x7C, 0x7D	Not applicable	R	Yes

Table 125. FLSHCNT_LOW Bit Definitions

Bits	Description
[15:0]	Flash memory write counter, low word

Table 126. FLSHCNT_HIGH Register Definitions

Page	Addresses	Default	Access	Flash Backup
0x02	0x7E, 0x7F	Not applicable	R	Yes

Table 127. FLSHCNT_HIGH Bit Definitions

Bits	Description
[15:0]	Flash memory write counter, high word

The FLSHCNT_LOW (see Table 124 and Table 125) and FLSHCNT_HIGH (see Table 126 and Table 127) registers combine to provide a 32-bit, binary counter that tracks the number of flash memory write cycles. In addition to the number of write cycles, the flash memory has a finite service lifetime, which depends on the junction temperature. Figure 48 provides guidance for estimating the retention life for the flash memory at specific junction temperatures. The junction temperature is approximately 7°C above the case temperature.

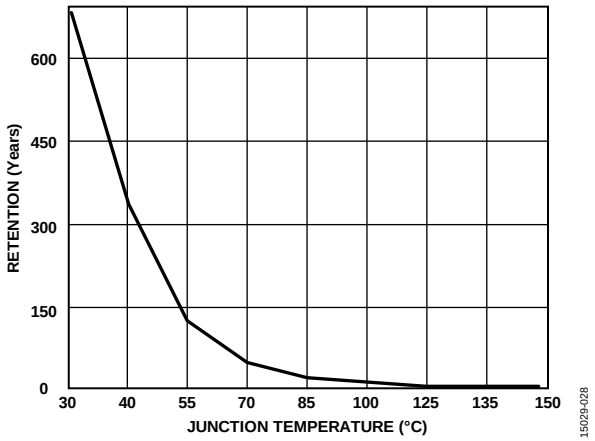

Figure 48. Flash Memory Retention

Global Commands, GLOB_CMD

Table 128. GLOB_CMD Register Definitions

Page	Addresses	Default	Access	Flash Backup
0x03	0x02, 0x03	Not applicable	W	No

Table 129. GLOB_CMD Bit Definitions

Bits	Description
[15:8]	Not used
7	Software reset
6	Factory calibration restore
[5:4]	Not used
3	Flash memory update
2	Not used
1	Self test
0	Bias correction update

The GLOB_CMD register (see Table 128 and Table 129) provides trigger bits for several operations. Write a 1 to the appropriate bit in GLOB_CMD to start a particular function.

Software Reset

Select Page 3 (DIN = 0x8003) and then set GLOB_CMD[7] = 1 (DIN = 0x8280, DIN = 0x8300) to initiate a reset in the operation of the ADIS16490. This reset removes all data, initializes all registers from their flash settings, and restarts data sampling and processing. This function provides a firmware alternative to providing a low pulse on the $\overline{\text{RST}}$ pin (see Table 6, Pin 8).

Factory Calibration Restore

Select Page 3 (DIN = 0x8003) and then set GLOB_CMD[6] = 1 (DIN = 0x8240, DIN = 0x8300) to initiate restoration of the factory calibration. This restoration writes 0x0000 to the following registers: X_GYRO_SCALE, Y_GYRO_SCALE, Z_GYRO_SCALE, X_ACCL_SCALE, Y_ACCL_SCALE, Z_ACCL_SCALE, XG_BIAS_LOW, XG_BIAS_HIGH, YG_BIAS_LOW, YG_BIAS_HIGH, ZG_BIAS_LOW, ZG_BIAS_HIGH, XA_BIAS_LOW, XA_BIAS_HIGH, YA_BIAS_LOW, YA_BIAS_HIGH, ZA_BIAS_LOW, and ZA_BIAS_HIGH.

Flash Memory Update

Select Page 3 (DIN = 0x8003) and then set GLOB_CMD[3] = 1 (DIN = 0x8208, DIN = 0x8300) to initiate a manual flash update. SYS_E_FLAG[6] (see Table 16) identifies success (0) or failure (1) in completing this process.

Note that the user must not poll the status registers while waiting for the update to complete because the serial port is disabled. Rather, the user must either wait the prescribed amount of time found in Table 3 or wait for the data ready indicator pin to begin toggling.

On Demand Self Test (ODST)

Select Page 3 (DIN = 0x8003) and then set GLOB_CMD[1] = 1 (DIN = 0x8202, then DIN = 0x8300) to run the ODST routine, which executes the following steps:

1. Measure the output on each sensor.
2. Activate an internal force on the mechanical elements of each sensor, which simulates the force associated with actual inertial motion.
3. Measure the output response on each sensor.
4. Deactivate the internal force on each sensor.
5. Calculate the difference between the force on and normal operating conditions (force off).
6. Compare the difference with internal pass/fail criteria.
7. Report the pass/fail results for each sensor in DIAG_STS (see Table 18) and the overall pass/fail flag in SYS_E_FLAG[5] (see Table 16).

False positive results are possible when executing the ODST while the device is in motion. Note that the user must not poll the status registers while waiting for the test to complete. Rather, the user must either wait the prescribed amount of time found in Table 3 or wait for the data ready indicator pin to begin toggling.

Bias Correction Update

Select Page 3 (DIN = 0x8003) and set GLOB_CMD[0] = 1 (DIN = 0x8201, then DIN = 0x8300) to update the user offset registers with the correction factors of the CBE (see Table 139). Ensure that the inertial platform is stable during the entire average time for optimal bias estimates.

Auxiliary I/O Line Configuration, FNCTIO_CTRL

Table 130. FNCTIO_CTRL Register Definitions

Page	Addresses	Default	Access	Flash Backup
0x03	0x06, 0x07	0x000D	R/W	Yes

Table 131. FNCTIO_CTRL Bit Definitions

Bits	Description
[15:9]	Not used
8	Sync clock mode: 1 = PPS, 0 = sync
7	Sync clock input enable: 1 = enabled, 0 = disabled
6	Sync clock input polarity: 1 = rising edge, 0 = falling edge
[5:4]	Sync clock input line selection: 00 = DIO1, 01 = DIO2, 10 = DIO3, 11 = DIO4
3	Data ready enable: 1 = enabled, 0 = disabled
2	Data ready polarity: 1 = positive, 0 = negative
[1:0]	Data ready line selection: 00 = DIO1, 01 = DIO2, 10 = DIO3, 11 = DIO4

The FNCTIO_CTRL register (see Table 130 and Table 131) provides configuration control for each I/O pin (DIO1, DIO2, DIO3, and DIO4). Each DIOx pin supports only one function at a time. When a single pin has two assignments, the enable bit for the lower priority function automatically resets to zero (disabling the lower priority function). The order of priority is as follows, from highest priority to lowest priority: data ready, sync clock input, and general-purpose. The ADIS16490 can take up to 20 ms to execute a write command to the FNCTIO_CTRL register. During this time, the operational state and the contents of the register remain unchanged, but the SPI interface supports normal communication (for accessing other registers).

Data Ready Indicator

The FNCTIO_CTRL[3:0] bits provide three configuration options for the data ready function: on/off, polarity, and DIOx line. The primary purpose this signal is to drive the interrupt control line of an embedded processor, which can help synchronize data collection and minimize latency. The data ready indicator is useful to determine if the controller inside the ADIS16490 is busy with a task (for example, a flash memory update) because data ready stops togging while these tasks are performed and resumes on completion. The factory default assigns DIO2 as a positive polarity, data ready signal, which means that the data in the output registers is valid when the DIO2 line is high (see Figure 30). This configuration works well when DIO2 drives an interrupt service pin that activates on a low to high pulse. Use the following sequence to change this assignment to DIO3 with negative polarity:

1. Select Page 3 (DIN = 0x8003).
2. Set FNCTIO_CTRL[3:0] = 1000 (DIN = 0x860A, then DIN = 0x8700).

The timing jitter on the data ready signal is typically within ±1.4 µs. When using DIO1 to support the data ready function, this signal can experience premature data ready pulses during the ADIS16490 start-up. However, these pulses do not indicate

that data production has started. If it is necessary to use DIO1 for this function, use it in conjunction with a delay or other control mechanism to prevent premature data acquisition activity during the start-up process.

Input Sync/Clock Control

The FNCTIO_CTRL[8:4] bits provide several configuration options for using one of the DIOx lines as an external clock signal and for controlling inertial sensor data collection and processing. For example, use the following sequence to establish DIO4 as a positive polarity, input clock pin that operates in sync mode and preserves the factory default setting for the data ready function:

1. Select Page 3 (DIN = 0x8003).
2. Set FNCTIO_CTRL[7:0] = 0xFD (DIN = 0x86FD).
3. Set FNCTIO_CTRL[15:8] = 0x00 (DIN = 0x8700).

In sync mode, the ADIS16490 disables its internal sample clock, and the frequency of the external clock signal establishes the rate of data collection and processing (f_{SM} in Figure 23 and Figure 24). When using the PPS mode (FNCTIO_CTRL[8] = 1) the rate of data collection and production (f_{SM}) is equal to the product of the external clock frequency and scale factor (K_{ECSF}) in the SYNC_SCALE register (see Table 141).

General-Purpose I/O Control, GPIO_CTRL

Table 132. GPIO_CTRL Register Definitions[1]

Page	Addresses	Default	Access	Flash Backup
0x03	0x08, 0x09	0x00X0	R/W	Yes

[1] The GPIO_CTRL[7:4] bits reflect the logic levels on the DIOx lines and do not have a default setting.

Table 133. GPIO_CTRL Bit Definitions[1]

Bits	Description
[15:8]	Don't care
7	General-Purpose I/O Line 4 (DIO4) data level
6	General-Purpose I/O Line 3 (DIO3) data level
5	General-Purpose I/O Line 2 (DIO2) data level
4	General-Purpose I/O Line 1 (DIO1) data level
3	General-Purpose I/O Line 4 (DIO4) direction control (1 = output, 0 = input)
2	General-Purpose I/O Line 3 (DIO3) direction control (1 = output, 0 = input)
1	General-Purpose I/O Line 2 (DIO2) direction control (1 = output, 0 = input)
0	General-Purpose I/O Line 1 (DIO1) direction control (1 = output, 0 = input)

[1] The GPIO_CTRL[7:4] bits reflect the logic levels on the DIOx lines and do not have a default setting.

When FNCTIO_CTRL does not configure a DIOx pin, the GPIO_CTRL register (see Table 132 and Table 133) provides user controls for general-purpose use of the DIOx pins. GPIO_CTRL[3:0] provide input/output assignment controls for each line. When the DIOx lines are inputs, monitor their level by reading GPIO_CTRL[7:4]. When the DIOx lines are used as outputs, set their level by writing to GPIO_CTRL[7:4]. For example, use the following sequence to set DIO1 and DIO3 as high and low output lines, respectively, and set DIO2 and DIO4 as input lines. Select Page 3 (DIN = 0x8003) and set GPIO_ CTRL[7:0] = 0x15 (DIN = 0x8815, then DIN = 0x8900).

Miscellaneous Configuration, CONFIG

Table 134. CONFIG Register Definitions

Page	Addresses	Default	Access	Flash Backup
0x03	0x0A, 0x0B	0x00C0	R/W	Yes

Table 135. CONFIG Bit Definitions

Bits	Description
[15:8]	Not used
7	Linear *g* compensation for gyroscopes (1 = enabled)
6	Point of percussion alignment (1 = enabled)
[5:0]	Not used

The CONFIG register (see Table 134 and Table 135) provides configuration options for the linear *g* compensation in the gyroscopes (on/off) and the point of percussion alignment for the accelerometers (on/off).

Point of Percussion

CONFIG[6] offers a point of percussion alignment function that maps the accelerometer sensors to the corner of the package identified in Figure 49. To activate this feature, select Page 3 (DIN = 0x8003), then set CONFIG[6] = 1 (DIN = 0x8A40, DIN = 0x8B00).

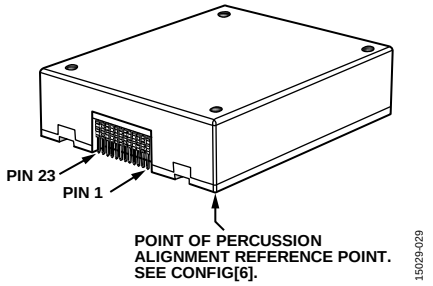

Figure 49. Point of Percussion Reference Point

Linear Acceleration on Effect on Gyroscope Bias

The ADIS16490 includes first-order compensation for the linear *g* effect in the gyroscopes, which uses the following model:

$$\begin{bmatrix} \omega_{XC} \\ \omega_{YC} \\ \omega_{ZC} \end{bmatrix} = \begin{bmatrix} LG_{11} & LG_{12} & LG_{13} \\ LG_{21} & LG_{22} & LG_{23} \\ LG_{31} & LG_{32} & LG_{33} \end{bmatrix} \times \begin{bmatrix} A_X \\ A_Y \\ A_Z \end{bmatrix} + \begin{bmatrix} \omega_{XPC} \\ \omega_{YPC} \\ \omega_{ZPC} \end{bmatrix}$$

The linear *g* correction factors, LG_{XY}, apply correction for linear acceleration in all three directions to the data path of each gyroscope (ω_{XPC}, ω_{YPC}, and ω_{ZPC}) at the rate of the data samples (4250 SPS when using the internal clock). CONFIG[7] provides an on/off control for this compensation. The factory default value for this bit activates this compensation. To turn it off, select Page 3 (DIN = 0x8003) and set CONFIG[7] = 0 (DIN = 0x8A40, DIN =

0x8B00). Note that this command sequence also preserves the default setting for the point of percussion alignment function (on).

Decimation Filter, DEC_RATE

Table 136. DEC_RATE Register Definitions

Page	Addresses	Default	Access	Flash Backup
0x03	0x0C, 0x0D	0x0000	R/W	Yes

Table 137. DEC_RATE Bit Definitions

Bits	Description
[15:0]	Decimation rate, binary format, maximum = 4249

The DEC_RATE register (see Table 136 and Table 137) provides user control for the final filter stage (see Figure 26), which averages and decimates the accelerometers and gyroscopes data, while also extending the time that the delta angle and delta velocity track between each update. The output sample rate is equal to 4250/(DEC_RATE + 1). For example, select Page 3 (DIN = 0x8003), and set DEC_RATE = 0x2A (DIN = 0x8C2A, then DIN = 0x8D00) to reduce the output sample rate to ~98.8 SPS (4250 ÷ 43).

Data Update Rate in External Sync Modes

When using the input sync option, in direct mode (FNCTIO_CTRL[8:7] = 01, see Table 131), replace the 4250 number in this relationship with the input clock frequency. When using the input sync option, in PPS mode (FNCTIO_CTRL[8:7] = 11, see Table 131), replace the 4250 number in this relationship with the product of the input sync frequency and the scale value in the SYNC_SCALE register (see Table 141).

Continuous Bias Estimation (CBE), NULL_CNFG

Table 138. NULL_CNFG Register Definitions

Page	Addresses	Default	Access	Flash Backup
0x03	0x0E, 0x0F	0x070A	R/W	Yes

Table 139. NULL_CNFG Bit Definitions

Bits	Description
[15:14]	Not used
13	Z-axis acceleration bias correction enable (1 = enabled)
12	Y-axis acceleration bias correction enable (1 = enabled)
11	X-axis acceleration bias correction enable (1 = enabled)
10	Z-axis gyroscope bias correction enable (1 = enabled)
9	Y-axis gyroscope bias correction enable (1 = enabled)
8	X-axis gyroscope bias correction enable (1 = enabled)
[7:4]	Not used
[3:0]	Time base control (TBC), range: 0 to 13 (default = 10); $t_B = 2^{TBC}/4250$, time base; $t_A = 64 \times t_B$, average time

The NULL_CNFG register (see Table 138 and Table 139) provides the configuration controls for the continuous bias estimator (CBE), which associates with the bias correction update command in GLOB_CMD[0] (see Table 129). NULL_CNFG[3:0] establishes the total average time (tA) for the bias estimates and NULL_CNFG[13:8] provide on/off controls for each sensor. The factory default configuration for NULL_CNFG enables the bias null command for the gyroscopes, disables the bias null command for the accelerometers, and sets the average time to ~15.42 seconds.

$$t_B = 2^{TBC}/4250 = 2^{10}/4250 = \sim 0.241 \text{ seconds}$$

$$t_A = 64 \times t_B = 64 \times 0.241 = 15.42 \text{ seconds}$$

where:
t_B is the time base.
t_A is the averaging time.

When a sensor bit in NULL_CNFG is active (equal to 1), setting GLOB_CMD[0] = 1 (DIN sequence: 0x8003, 0x8201, 0x8300) causes its bias correction register to automatically update with a value that corrects for its present bias error (from the CBE). For example, setting NULL_CNFG[8] equal to 1 causes an update in the XG_BIAS_LOW (see Table 93) and XG_BIAS_HIGH (see Table 95) registers.

Scaling the Input Clock (PPS Mode), SYNC_SCALE

Table 140. SYNC_SCALE Register Definitions

Page	Addresses	Default	Access	Flash Backup
0x03	0x10, 0x11	0x109A	R/W	Yes

Table 141. SYNC_SCALE Bit Definitions

Bits	Description
[15:0]	External clock scale factor (K_{ECSF}), binary format

The PPS mode (FNCTIO_CTRL[8] = 1, see Table 131) supports the use of an input sync frequency that is slower than the data sample rates of the inertial sensors. This mode supports a frequency range of 1 Hz to 128 Hz for the input sync mode. In this mode, the data sample rate is equal to the product of the value in the SYNC_SCALE register (see Table 140 and Table 141) and the input sync frequency. For example, the following command sequence sets the data collection and processing rate (f_{SM} in Figure 23 and Figure 24) to 4000 Hz (SYNC_SCALE = 0x0FA0) when using a 1 Hz signal on the DIO3 line as the external clock input, while also preserving the factory default configuration for the data ready signal:

1. Select Page 3 (DIN = 0x8003).
2. Set SYNC_SCALE[7:0] = 0xA0 (DIN = 0x90A0).
3. Set SYNC_SCALE[15:8] = 0x0F (DIN = 0x910F).
4. Set FNCTIO_CTRL[7:0] = 0xFD (DIN = 0x86ED).
5. Set FNCTIO_CTRL[15:8] = 0x00 (DIN = 0x8701).

Note that the data ready indicator pin does not begin to toggle until at least two external clock edges (with valid time period between them) are detected by the ADIS16495.

FIR Filter Control, FILTR_BNK_0, FILTR_BNK_1

Table 142. FILTR_BNK_0 Register Definitions

Page	Addresses	Default	Access	Flash Backup
0x03	0x16, 0x17	0x0000	R/W	Yes

Table 143. FILTR_BNK_0 Bit Definitions

Bits	Description (Default = 0x0000)
15	Don't care
14	Y-axis accelerometer filter enable (1 = enabled)
[13:12]	Y-axis accelerometer filter bank selection: 00 = Bank A, 01 = Bank B, 10 = Bank C, 11 = Bank D
11	X-axis accelerometer filter enable (1 = enabled)
[10:9]	X-axis accelerometer filter bank selection: 00 = Bank A, 01 = Bank B, 10 = Bank C, 11 = Bank D
8	Z-axis gyroscope filter enable (1 = enabled)
[7:6]	Z-axis gyroscope filter bank selection:
	00 = Bank A, 01 = Bank B, 10 = Bank C, 11 = Bank D
5	Y-axis gyroscope filter enable (1 = enabled)
[4:3]	Y-axis gyroscope filter bank selection: 00 = Bank A, 01 = Bank B, 10 = Bank C, 11 = Bank D
2	X-axis gyroscope filter enable (1 = enabled)
[1:0]	X-axis gyroscope filter bank selection: 00 = Bank A, 01 = Bank B, 10 = Bank C, 11 = Bank D

Table 144. FILTR_BNK_1 Register Definitions

Page	Addresses	Default	Access	Flash Backup
0x03	0x18, 0x19	0x0000	R/W	Yes

Table 145. FILTR_BNK_1 Bit Definitions

Bits	Description
[15:3]	Don't care
2	Z-axis accelerometer filter enable (1 = enabled)
[1:0]	Z-axis accelerometer filter bank selection:
	00 = Bank A, 01 = Bank B, 10 = Bank C, 11 = Bank D

The FILTR_BNK_0 (see Table 142 and Table 143) and FILTR_BNK_1 (see Table 144 and Table 145) registers provide the configuration controls for the FIR filter bank in the signal chain of each sensor (see Figure 26). These registers provide on/off control for the FIR bank for each inertial sensor, along with the FIR bank (A, B, C, or D) that each sensor uses.

Firmware Revision, FIRM_REV

Table 146. FIRM_REV Register Definitions

Page	Addresses	Default	Access	Flash Backup
0x03	0x78, 0x79	Not applicable	R	Yes

Table 147. FIRM_REV Bit Definitions

Bits	Description
[15:12]	Firmware revision binary coded decimal (BCD) code, tens digit, numerical format = 4-bit binary, range = 0 to 9
[11:8]	Firmware revision BCD code, ones digit, numerical format = 4-bit binary, range = 0 to 9
[7:4]	Firmware revision BCD code, tenths digit, numerical format = 4-bit binary, range = 0 to 9
[3:0]	Firmware revision BCD code, hundredths digit, numerical format = 4-bit binary, range = 0 to 9

The FIRM_REV register (see Table 146 and Table 147) provides the firmware revision for the internal firmware. This register uses a BCD format, where each nibble represents a digit. For example, if FIRM_REV = 0x1234, the firmware revision is 12.34.

Firmware Revision Day and Month, FIRM_DM

Table 148. FIRM_DM Register Definitions

Page	Addresses	Default	Access	Flash Backup
0x03	0x7A, 0x7B	Not applicable	R	Yes

Table 149. FIRM_DM Bit Definitions

Bits	Description
[15:12]	Factory configuration month BCD code, tens digit, numerical format = 4-bit binary, range = 0 to 2
[11:8]	Factory configuration month BCD code, ones digit, numerical format = 4-bit binary, range = 0 to 9
[7:4]	Factory configuration day BCD code, tens digit, numerical format = 4-bit binary, range = 0 to 3
[3:0]	Factory configuration day BCD code, ones digit, numerical format = 4-bit binary, range = 0 to 9

The FIRM_DM register (see Table 148 and Table 149) contains the month and day of the factory configuration date. FIRM_DM[15:12] and FIRM_DM[11:8] contain digits that represent the month of the factory configuration in a BCD format. For example, November is the 11th month in a year and is represented by FIRM_DM[15:8] = 0x11. FIRM_DM[7:4] and FIRM_DM[3:0] contain digits that represent the day of factory configuration in a BCD format. For example, the 27th day of the month is represented by FIRM_DM[7:0] = 0x27.

Firmware Revision Year, FIRM_Y

Table 150. FIRM_Y Register Definitions

Page	Addresses	Default	Access	Flash Backup
0x03	0x7C, 0x7D	Not applicable	R	Yes

Table 151. FIRM_Y Bit Definitions

Bits	Description
[15:12]	Factory configuration year BCD code, thousands digit, numerical format = 4-bit binary, range = 0 to 9
[11:8]	Factory configuration year BCD code, hundreds digit, numerical format = 4-bit binary, range = 0 to 9
[7:4]	Factory configuration year BCD code, tens digit, numerical format = 4-bit binary, range = 0 to 3
[3:0]	Factory configuration year BCD code, ones digit, numerical format = 4-bit binary, range = 0 to 9

The FIRM_Y register (see Table 150 and Table 151) contains the year of the factory configuration date. For example, the year 2013 is represented by FIRM_Y = 0x2013.

Boot Revision Number, BOOT_REV

Table 152. BOOT_REV Register Definitions

Page	Addresses	Default	Access	Flash Backup
0x03	0x7E, 0x7F	Not applicable	R	Yes

Table 153. BOOT_REV Bit Definitions

Bits	Description
[15:8]	Binary, major revision number
[7:0]	Binary, minor revision number

Continuous SRAM Testing

This device employs a CRC function on the SRAM memory blocks that contain the program code (CODE_SIGTR_xxx) and the calibration coefficients (CAL_DRVTN_xxx). This process operates in the background and generates real-time, 32-bit CRC values for the program code and calibration coefficients, respectively. At the conclusion of each cycle, the processor writes these calculated values in the CAL_DRVTN_xxx and CODE_DRVTN_xxx registers (see Table 159, Table 161, Table 167, and Table 169) and compares them with the signature values, which reflect the state of these memory locations at the time of factory configuration. When the calculation results do not match the signature values, SYS_E_ FLAG[2] increases to a 1. The respective signature values are available for user access through the CAL_SIGTR_xxx and CODE_SIGTR_xxx registers (see Table 155, Table 157, Table 163, and Table 165). The following conditions must be met for SYS_E_FLAG[2] to remain at the zero level:

- CAL_SIGTR_LWR = CAL_DRVTN_LWR
- CAL_SIGTR_UPR = CAL_DRVTN_UPR
- CODE_SIGTR_LWR = CODE_DRVTN_LWR
- CODE_SIGTR_UPR = CODE_DRVTN_UPR

Signature CRC, Calibration Values, CAL_SIGTR_LWR

Table 154. CAL_SIGTR_LWR Register Definitions

Page	Addresses	Default	Access	Flash Backup
0x04	0x04, 0x05	Not applicable	R	Yes

Table 155. CAL_SIGTR_LWR Bit Definitions

Bits	Description
[15:0]	Factory programmed CRC value for the program code, low word

Signature CRC, Calibration Values, CAL_SIGTR_UPR

Table 156. CAL_SIGTR_UPR Register Definitions

Page	Addresses	Default	Access	Flash Backup
0x04	0x06, 0x07	Not applicable	R	Yes

Table 157. CAL_SIGTR_UPR Bit Definitions

Bits	Description
[15:0]	Factory programmed CRC value for the program code, high word

Derived CRC, Calibration Values, CAL_DRVTN_LWR

Table 158. CAL_DRVTN_LWR Register Definitions

Page	Addresses	Default	Access	Flash Backup
0x04	0x08, 0x09	Not applicable	R	No

Table 159. CAL_DRVTN_LWR Bit Definitions

Bits	Description
[15:0]	Calculated CRC value for the program code, low word

Derived CRC, Calibration Values, CAL_DRVTN_UPR

Table 160. CAL_DRVTN_UPR Register Definitions

Page	Addresses	Default	Access	Flash Backup
0x04	0x0A, 0x0B	Not applicable	R	No

Table 161. CAL_DRVTN_UPR Bit Definitions

Bits	Description
[15:0]	Calculated CRC value for the program code, high word

Signature CRC, Program Code, CODE_SIGTR_LWR

Table 162. CODE_SIGTR_LWR Register Definitions

Page	Addresses	Default	Access	Flash Backup
0x04	0x0C, 0x0D	Not applicable	R	Yes

Table 163. CODE_SIGTR_LWR Bit Definitions

Bits	Description
[15:0]	Factory programmed CRC value for the calibration coefficients, low word

Signature CRC, Program Code, CODE_SIGTR_UPR

Table 164. CODE_SIGTR_UPR Register Definitions

Page	Addresses	Default	Access	Flash Backup
0x04	0x0E, 0x0F	Not applicable	R	Yes

Table 165. CODE_SIGTR_UPR Bit Definitions

Bits	Description
[15:0]	Factory programmed CRC value for the calibration coefficients, high word

Derived CRC, Program Code, CODE_DRVTN_LWR

Table 166. CODE_DRVTN_LWR Register Definitions

Page	Addresses	Default	Access	Flash Backup
0x04	0x10, 0x11	Not applicable	R	No

Table 167. CODE_DRVTN_LWR Bit Definitions

Bits	Description
[15:0]	Calculated CRC value for the calibration coefficients, low word

Derived CRC, Program Code, CODE_DRVTN_UPR

Table 168. CODE_DRVTN_LWR Register Definitions

Page	Addresses	Default	Access	Flash Backup
0x04	0x12, 0x13	Not applicable	R	No

Table 169. CODE_DRVTN_UPR Bit Definitions

Bits	Description
[15:0]	Calculated CRC value for the calibration coefficients, high word

Lot Specific Serial Number, SERIAL_NUM

Table 170. SERIAL_NUM Register Definitions

Page	Addresses	Default	Access	Flash Backup
0x04	0x20, 0x21	Not applicable	R	Yes

Table 171. SERIAL_NUM Bit Definitions

Bits	Description
[15:0]	Lot specific serial number

FIR FILTERS

The ADIS16490 provides four FIR filter banks to configure and select for each individual inertial sensor using the FILTR_BNK_0 (see Table 143) and FILTR_BNK_1 (see Table 145) registers. Each FIR filter bank (A, B, C, and D) has 120 taps that consume two pages of memory. The coefficient associated with each tap, in each filter bank, has its own dedicated register that uses a 16-bit, twos complement format. The FIR filter has unity gain when the sum of all of the coefficients is equal to 32,768. For filter designs that require less than 120 taps, write 0x0000 to all unused registers to eliminate the latency associated with that particular tap.

FIR Filter Bank A, FIR_COEF_A000 to FIR_COEF_A119

Table 172. FIR Filter Bank A Memory Map

Page	PAGE_ID	Addresses	Register
5	0x05	0x00, 0x01	PAGE_ID
5	0x05	0x02 to 0x07	Not used
5	0x05	0x08, 0x09	FIR_COEF_A000
5	0x05	0x0A, 0x0B	FIR_COEF_A001
5	0x05	0x0C to 0x7D	FIR_COEF_A002 to FIR_COEF_A058
5	0x05	0x7E, 0x07F	FIR_COEF_A059
6	0x06	0x00, 0x01	PAGE_ID
6	0x06	0x02 to 0x07	Not used
6	0x06	0x08, 0x09	FIR_COEF_A060
6	0x06	0x0A, 0x0B	FIR_COEF_A061
6	0x06	0x0C to 0x7D	FIR_COEF_A062 to FIR_COEF_A118
6	0x06	0x7E, 0x7F	FIR_COEF_A119

Table 173 and Table 174 provide detailed register and bit definitions for one of the FIR coefficient registers in Bank A, FIR_COEF_A071. Table 175 provides a configuration example, which sets this register to a decimal value of −169 (0xFF57).

Table 173. FIR_COEF_A071 Register Definitions

Page	Addresses	Default	Access	Flash Backup
0x06	0x1E, 0x1F	Not applicable	R/W	Yes

Table 174. FIR_COEF_A071 Bit Definitions

Bits	Description
[15:0]	FIR Bank A, Coefficient 71, twos complement

Table 175. Configuration Example, FIR Coefficient

DIN	Description
0x8006	Select Page 6
0x9E57	FIR_COEF_A071[7:0] = 0x57
0x9FFF	FIR_COEF_A071[15:8] = 0xFF

FIR Filter Bank B, FIR_COEF_B000 to FIR_COEF_B119

Table 176. Filter Bank B Memory Map

Page	PAGE_ID	Addresses	Register
7	0x07	0x00, 0x01	PAGE_ID
7	0x07	0x02 to 0x07	Not used
7	0x07	0x08, 0x09	FIR_COEF_B000
7	0x07	0x0A, 0x0B	FIR_COEF_B001
7	0x07	0x0C to 0x7D	FIR_COEF_B002 to FIR_COEF_B058
7	0x07	0x7E, 0x07F	FIR_COEF_B059
8	0x08	0x00, 0x01	PAGE_ID
8	0x08	0x02 to 0x07	Not used
8	0x08	0x08, 0x09	FIR_COEF_B060
8	0x08	0x0A, 0x0B	FIR_COEF_B061
8	0x08	0x0C to 0x7D	FIR_COEF_B062 to FIR_COEF_B118
8	0x08	0x7E, 0x7F	FIR_COEF_B119

FIR Filter Bank C, FIR_COEF_C000 to FIR_COEF_C119

Table 177. Filter Bank C Memory Map

Page	PAGE_ID	Addresses	Register
9	0x09	0x00, 0x01	PAGE_ID
9	0x09	0x02 to 0x07	Not used
9	0x09	0x08, 0x09	FIR_COEF_C000
9	0x09	0x0A, 0x0B	FIR_COEF_C001
9	0x09	0x0C to 0x7D	FIR_COEF_C002 to FIR_COEF_C058
9	0x09	0x7E, 0x07F	FIR_COEF_C059
10	0x0A	0x00, 0x01	PAGE_ID
10	0x0A	0x02 to 0x07	Not used
10	0x0A	0x08, 0x09	FIR_COEF_C060
10	0x0A	0x0A, 0x0B	FIR_COEF_C061
10	0x0A	0x0C to 0x7D	FIR_COEF_C062 to FIR_COEF_C118
10	0x0A	0x7E, 0x7F	FIR_COEF_C119

FIR Filter Bank D, FIR_COEF_D000 to FIR_COEF_D119

Table 178. Filter Bank D Memory Map

Page	PAGE_ID	Addresses	Register
11	0x0B	0x00, 0x01	PAGE_ID
11	0x0B	0x02 to 0x07	Not used
11	0x0B	0x08, 0x09	FIR_COEF_D000
11	0x0B	0x0A, 0x0B	FIR_COEF_D001
11	0x0B	0x0C to 0x7D	FIR_COEF_D002 to FIR_COEF_D058
11	0x0B	0x7E, 0x07F	FIR_COEF_D059
12	0x0C	0x00, 0x01	PAGE_ID
12	0x0C	0x02 to 0x07	Not used
12	0x0C	0x08, 0x09	FIR_COEF_D060
12	0x0C	0x0A, 0x0B	FIR_COEF_D061
12	0x0C	0x0C to 0x7D	FIR_COEF_D062 to FIR_COEF_D118
12	0x0C	0x7E, 0x7F	FIR_COEF_D119

Default Filter Performance

The FIR filter banks have factory programmed filter designs. They are all low-pass filters that have unity dc gain. Table 179 provides a summary of each filter design, and Figure 50 shows the frequency response characteristics. The phase delay is equal to ½ of the total number of taps.

Table 179. FIR Filter Descriptions, Default Configuration

FIR Filter Bank	Taps	−3 dB Frequency (Hz)
A	120	300
B	120	100
C	32	300
D	32	100

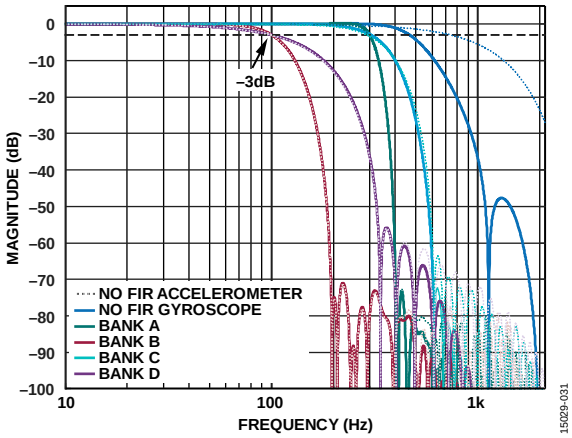

Figure 50. FIR Filter Frequency Response Curves

APPLICATIONS INFORMATION

MOUNTING BEST PRACTICES

For the best performance, follow these simple rules when installing the ADIS16490 into a system:

- Eliminate opportunity for translational force (x- and y-axis direction, per Figure 40) application on the electrical connector.
- Use uniform mounting forces on all four corners. The suggested torque setting is 40 inch ounces (0.285 Nm).
- When the IMU rests on the PCB, which contains the mating connector (see Figure 51), use a diameter of at least 2.85 mm for the passthrough holes.

These rules help prevent irregular force profiles, which can warp the package and introduce bias errors in the sensors. Figure 51 and Figure 52 provide details for mounting hole and connector alignment pin drill locations.

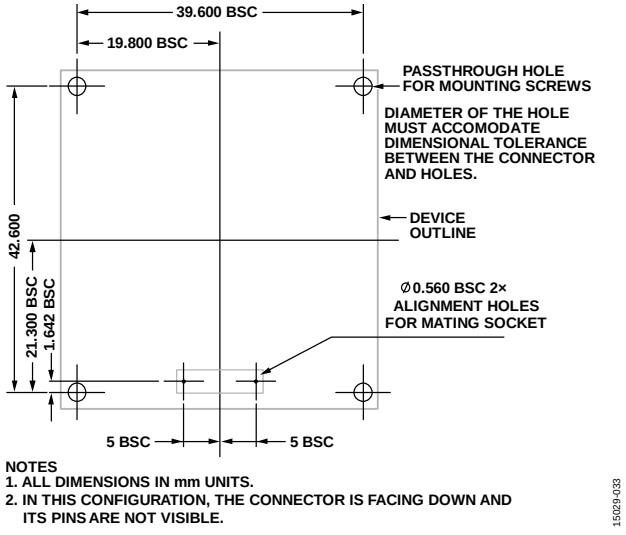

Figure 51. Suggested PCB Layout Pattern, Connector Down

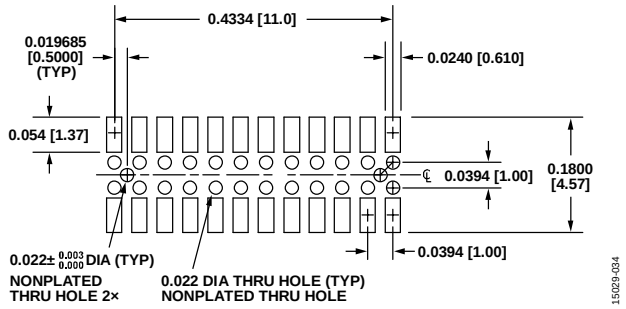

Figure 52. Suggested Layout and Mechanical Design When Using Samtec CLM-112-02-G-D-A for the Mating Connector

PREVENTING MISINSERTION

The ADIS16490 connector uses the same pattern as the ADIS16485, but with Pin 12 and Pin 15 missing. This pin configuration enables a mating connector to plug these holes, which makes inserting the ADIS16490 incorrectly very difficult. Samtec has a custom part number that provides this type of mating socket: ASP-193371-04.

EVALUATION TOOLS

Breakout Board, ADIS16IMU1/PCBZ

The ADIS16IMU1/PCBZ (sold separately) provides a breakout board function for the ADIS16490, which means that it provides access to the ADIS16490 through larger connectors that support standard 1 mm ribbon cabling. It also provides four mounting holes for attachment of the ADIS16490 to the breakout board.

PC-Based Evaluation, EVAL-ADIS2

Use the EVAL-ADIS2 and ADIS16IMU1/PCBZ to evaluate the ADIS16490 on a PC-based platform.

POWER SUPPLY CONSIDERATIONS

The VDD power supply must charge 46 µF of capacitance (inside of the ADIS16490, across the VDD and GND pins) during its initial ramp and settling process. When VDD reaches 2.85 V, the ADIS16490 begins its internal start-up process, which generates additional transient current demand. See Figure 53 for a typical current profile during the start-up process. The first peak in Figure 53 relates to charging the 46 µF capacitor bank, whereas the other transient activity relates to numerous functions turning on during the initialization process of the ADIS16490.

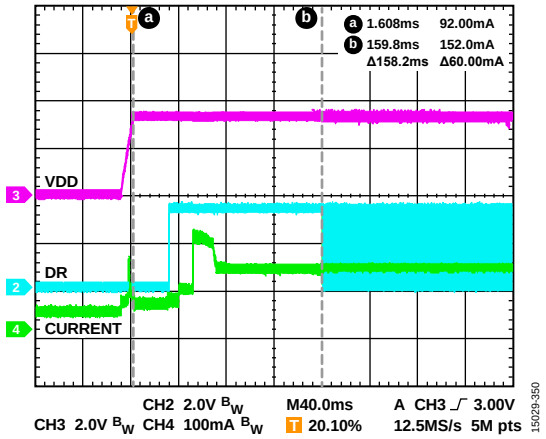

Figure 53. Transient Current Demand, Startup (DR Means Data Ready)

PACKAGING AND ORDERING INFORMATION

OUTLINE DIMENSIONS

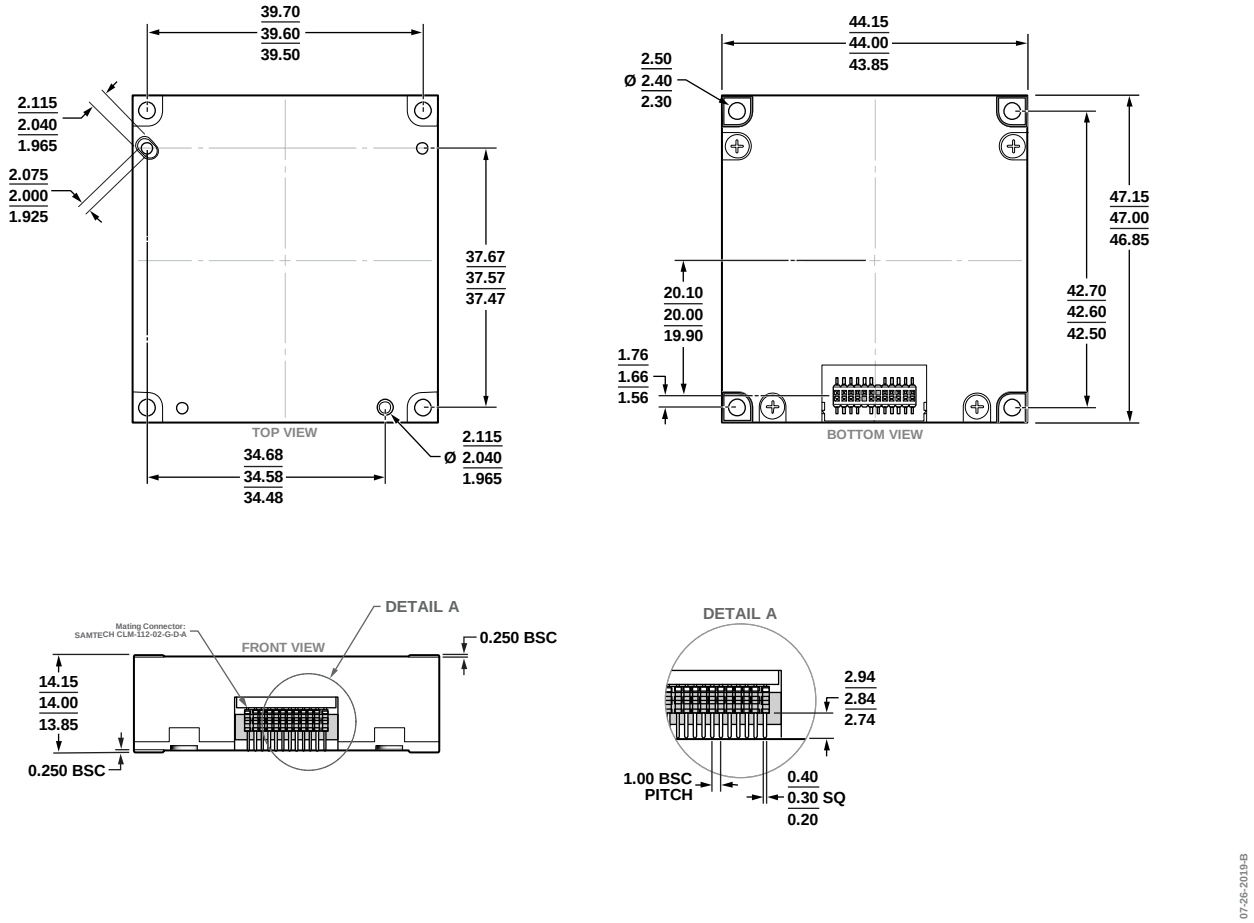

Figure 54. 24-Lead Module with Connector Interface [MODULE]
(ML-24-9)
Dimensions shown in millimeters

ORDERING GUIDE

Model[1]	Temperature Range	Description	Package Option
ADIS16490BMLZ	−40°C to +105°C	24-Lead Module with Connector Interface [MODULE]	ML-24-9

[1] Z = RoHS Compliant Part.