D2900, JANUARY 1986—REVISED MARCH 1988

- **Provides Control for 16K, 64K, 256K, and 1M Dynamic RAMs**
- **Highest-Order Two-Address Bits Select One of Four Banks of RAMs**
- **Supports Scrubbing Operations and Nibble-Mode Access**
- **Separate Output Enable for Multi-Channel Access to Memory**
- **52-Pin Dual-In-Line Package**

description

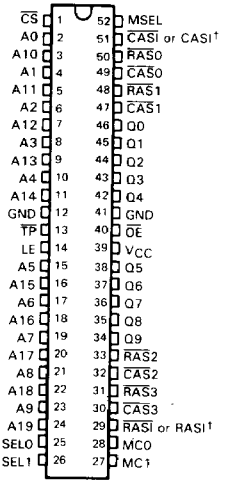
The 'ALS6301 and 'ALS6302 dynamic memory controllers (DMCs) are designed for use in today's high-performance memory systems. The DMC acts as the address controller between any processor and dynamic memory array.

Two versions are provided that help simplify interfacing to the system dynamic timing controller. The 'ALS6301 offers active-low Row Address Strobe Input ($\overline{RASI}$) and Column Address Strobe Input ($\overline{CASI}$), while the 'ALS6302 offers active-high Row Address Strobe Input (RASI) and Column Address Strobe Input (CASI) inputs.

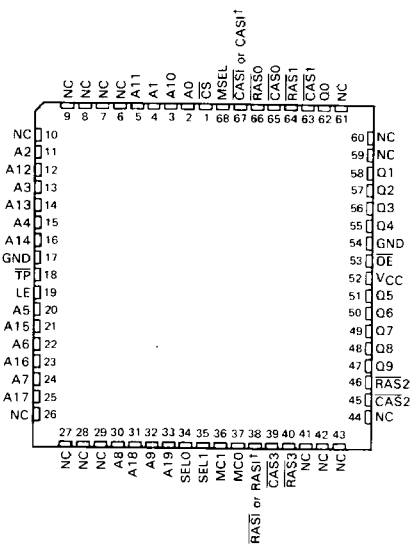
Using two 10-bit address latches, the DMC will hold the row and column addresses for any DRAM up to 1M. These latches and the two row/column refresh address counters feed into a 10-bit, 4-input MUX for output to the dynamic RAM address lines. A 2-bit bank select latch is provided to select one of the four $\overline{RAS}$ and $\overline{CAS}$ outputs. The two bits are normally obtained from the two highest-order address bits.

The 'ALS6301 and 'ALS6302 have two basic modes of operation, read/write and refresh. During normal read/write operations, the row and column addresses are multiplexed to the dynamic RAM, with the corresponding $\overline{RAS}$ and $\overline{CAS}$ signals activated to strobe the addresses into the RAM. In the refresh mode, the two counters cycle through the refresh addresses. If memory scrubbing is not being implemented, only the row counter is used. When memory scrubbing is being performed, both the row and column counters are used to perform read-modify-write cycles. In this mode all $\overline{RAS}$ outputs will be active (low) while only one $\overline{CAS}$ output is active at a time.

SN74ALS6301, SN74ALS6302 . . . JD OR N PACKAGE
(TOP VIEW)



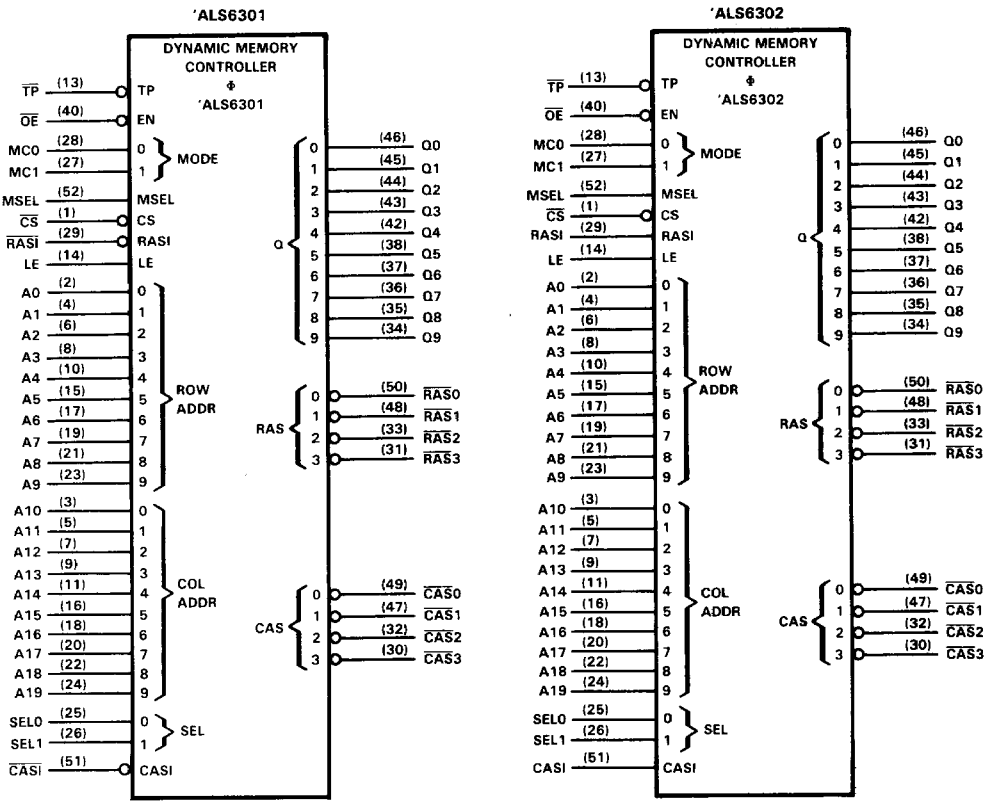
SN74ALS6301, SN74ALS6302 . . . FN PACKAGE
(TOP VIEW)



† 'ALS6301 has active-low inputs $\overline{CASI}$ and $\overline{RASI}$; 'ALS6302 has active-high inputs CASI and RASI.

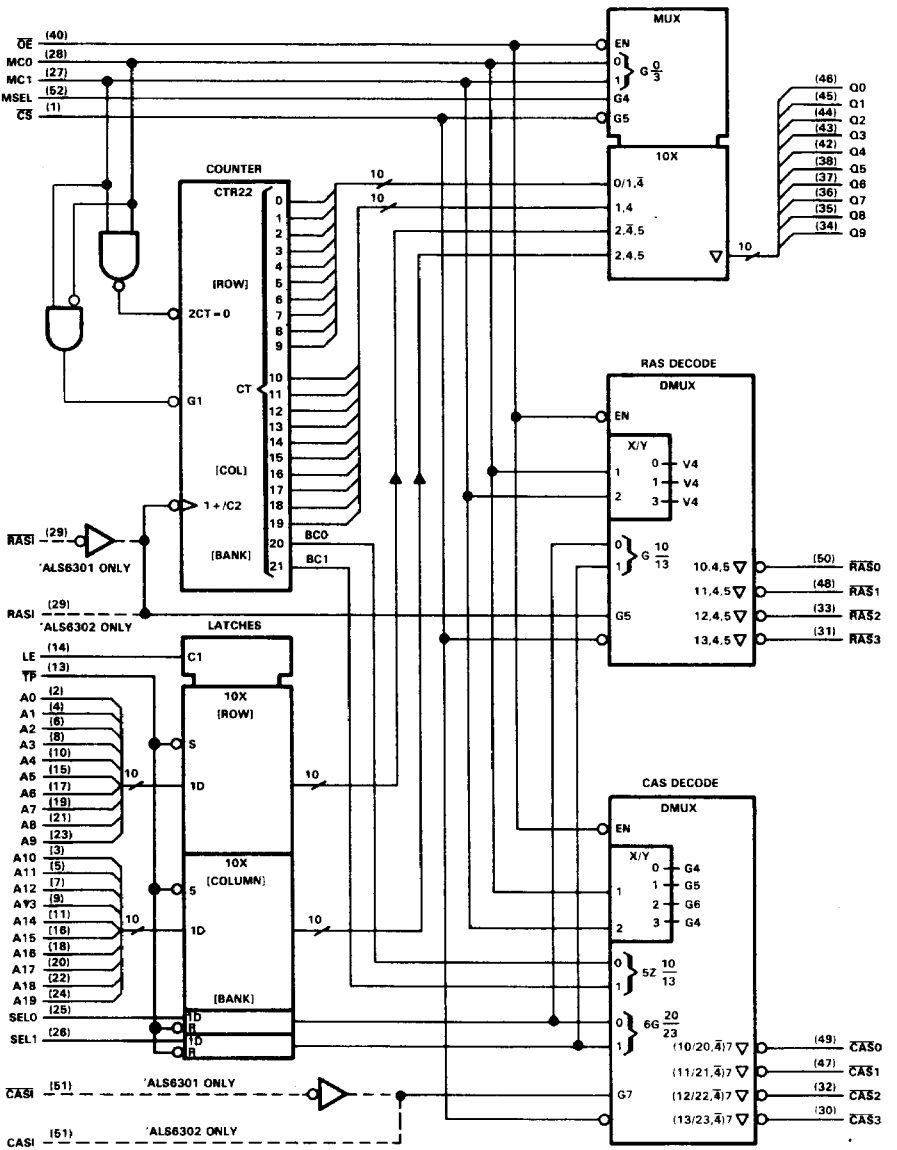
The SN74ALS6301 and SN74ALS6302 are characterized for operation from 0°C to 70°C.

logic symbols†



†These symbols are in accordance with ANSI/IEEE Std-91-1984 and IEC Publication 617-12.
Pin numbers shown are for JD and N packages.

logic diagram (positive logic)



Pin numbers shown are for JD and N packages.

TERMINAL FUNCTIONS

PIN NAME	DESCRIPTION
A0-A19	Address Inputs. A0-A9 are latched in as the nine-bit row address for the DRAM. These inputs drive Q0-Q9 when the DMC is in the read/write mode and MSEL is low. A10-A19 are latched in as the column address, and will drive Q0-Q9 when MSEL is high and the DMC is in the read/write mode. The addresses are latched when the Latch Enable (LE) input signal is low.
$\overline{\text{CASI}}$ or CASI	Column Address Strobe Input. This input going active causes the selected $\overline{\text{CAS}}$ output to be forced low. The $\overline{\text{CASI}}$ input on the 'ALS6301 is active low input while on the 'ALS6302, CASI is active high input. (For more details see timing diagrams.)
$\overline{\text{CAS0}}$-$\overline{\text{CAS3}}$	Column Address Strobe. During normal Read/Write cycles the two selected bits (SEL0, SEL1) determine which $\overline{\text{CAS}}$ output will go active following $\overline{\text{CASI}}$ ('ALS6301) or CASI ('ALS6302) going active. When memory scrubbing is being performed, only the $\overline{\text{CAS}}$n signal selected will be active. For non-scrubbing cycles, all four $\overline{\text{CAS}}$ outputs will remain high.
$\overline{\text{CS}}$	Chip Select. This active-low input is used to enable the DMC. When $\overline{\text{CS}}$ is active, the DMC operates normally in all four modes. When $\overline{\text{CS}}$ goes high, the device will not enter the read/write mode. This allows other devices to access the same memory that the DMC is controlling.
LE	Latch Enable. This active-high input causes the row, column, and bank select latches to become transparent, allowing the latches to accept new input data. A low input on LE latches the input data.
MC0, MC1	Mode Controls. These inputs determine in which of the four modes the DMC operates. The description of each of the four operating modes is given in Table 2.
MSEL	Multiplexer Select. This input determines whether the row or column address will be sent to the memory address inputs. When MSEL is high, the column address is selected, while the row address is selected when MSEL is low. The address may come from either the address latch or refresh address counter depending on MC0 and MC1 (see Mode Control Function Table).
$\overline{\text{OE}}$	Output Enable. This active-low input enables/disables the output signals. When $\overline{\text{OE}}$ is high, the outputs of the DMC enter the high-impedance state.
Q0-Q9	Address Outputs. These address outputs feed the DRAM address inputs and provide drive for memory systems having capacitance of up to 500 picofarads.
$\overline{\text{RASI}}$ or RASI	Row Address Strobe Input. During the normal memory cycles, the decoded $\overline{\text{RAS}}$n output ($\overline{\text{RAS0}}$, $\overline{\text{RAS1}}$, $\overline{\text{RAS2}}$, or $\overline{\text{RAS3}}$) is forced low after receipt of an active Row Address Strobe Input signal. In either Refresh mode, all four $\overline{\text{RAS}}$ outputs will be low while the Row Address Strobe Input signal is active. The $\overline{\text{RASI}}$ on the 'ALS6301 is an active-low input while on the 'ALS6302, RASI is an active-high input. (For more details see timing diagrams).
$\overline{\text{RAS0}}$-$\overline{\text{RAS3}}$	Row Address Strobe. Each of the Row Address Strobe outputs provides a $\overline{\text{RAS}}$ signal to one of the four banks of dynamic memory. Each $\overline{\text{RAS}}$n output will go low when selected by SEL0 and SEL1 after $\overline{\text{RASI}}$ ('ALS6301) or RASI ('ALS6302) goes active. All four go low in response to $\overline{\text{RASI}}$ ('ALS6301) or RASI ('ALS6302) while in the refresh mode.
SEL0, SEL1	Bank Select. These two inputs are normally the two highest-order address bits and are used in the read/write mode to select which bank of memory will be receiving the $\overline{\text{RAS}}$ and $\overline{\text{CAS}}$ signals after $\overline{\text{RASI}}$ ('ALS6301) or RASI ('ALS6302) and $\overline{\text{CASI}}$ ('ALS6301) or CASI ('ALS6302) go active.
$\overline{\text{TP}}$	This active-low test input asynchronously sets the row and column input latches high, while forcing the two bank select latches low. In normal operation, $\overline{\text{TP}}$ is tied high.

FUNCTION TABLES

MODE-CONTROL

MC1	MC0	OPERATING MODE
L	L	Refresh Mode without Scrubbing. Refresh cycles are performed with only the row counter being used to generate the addresses. In this mode, all four $\overline{RAS}$ outputs are active while the four $\overline{CAS}$ outputs remain high.
L	H	Refresh with Scrubbing/Initialize. During this mode, refresh cycles are done with both the row and column counters generating the addresses. MSEL is used to select either the row or the column counter. All four $\overline{RAS}$ outputs go low in response to $\overline{RASI}$ ('ALS6301) or RASI ('ALS6302), while only one $\overline{CAS}$n output goes low in response to $\overline{CASI}$ ('ALS6301) or CASI ('ALS6302). The bank counter keeps track of which $\overline{CAS}$ output goes active. This mode can also be used during system power-up so that the memory can be written with a known data pattern.
H	L	Read/Write. This mode is used to perform read/write cycles. Both the Row and Column addresses are multiplexed to the address output lines using MSEL. SEL0 and SEL1 are decoded to determine which $\overline{RAS}$n and $\overline{CAS}$n outputs will be active. The refresh counter is disabled while in this mode.
H	H	Clear Refresh Counters. This mode clears the three refresh counters (row, column, and bank) on the inactive transition of $\overline{RASI}$ ('ALS6301) or RASI ('ALS6302), putting them at start of the refresh sequence (see timing diagrams for more detail). In this mode, all four $\overline{RAS}$ outputs are driven low after the active edge of $\overline{RASI}$ ('ALS6301) or RASI ('ALS6302) so that DRAM wake-up cycles may also be performed.

FUNCTION TABLES (continued)

ADDRESS OUTPUT FUNCTIONS

MODE	INPUTS				OUTPUTS Q0-Q9
	MC1	MC0	MSEL	$\overline{CS}$	
Refresh without scrubbing	L	L	X	X	Row counter address
Refresh with scrubbing	L	H	L	X	Row counter address
			H	X	Column counter address
Read/write	H	L	L	L	Row address†
			H	L	Column address†
			X	H	All L
Clear refresh counter‡	H	H	X	X	All L

RAS OUTPUT FUNCTIONS

INPUTS							OUTPUTS			
'ALS6301 $\overline{RASI}$	'ALS6302 RASI	MC1	MC0	SEL1†	SEL0†	$\overline{CS}$	$\overline{RAS0}$	$\overline{RAS1}$	$\overline{RAS2}$	$\overline{RAS3}$
L	H	L	L	X	X	X	L	L	L	L
L	H	L	H	X	X	X	L	L	L	L
L	H	H	L	L	L	L	L	H	H	H
				L	H	L	H	L	H	H
				H	L	L	H	H	L	H
				H	H	L	H	H	H	L
				X	X	H	H	H	H	H
L	H	H	H	X	X	X	L	L	L	L
H	L	X	X	X	X	X	H	H	H	H

CAS OUTPUT FUNCTIONS

INPUTS									OUTPUTS			
'ALS6301 $\overline{CASI}$	'ALS6302 CASI	MC1	MC0	SEL1†	SEL0†	INTERNAL BC1	INTERNAL BC0	$\overline{CS}$	$\overline{CAS0}$	$\overline{CAS1}$	$\overline{CAS2}$	$\overline{CAS3}$
L	H	L	L	X	X	X	X	X	H	H	H	H
L	H	L	H	X	X	L	L	X	L	H	H	H
						L	H	X	H	L	H	H
						H	L	X	H	H	L	H
						H	H	X	H	H	H	L
L	H	H	L	L	L	X	X	L	L	H	H	H
				L	H	X	X	L	H	L	H	H
				H	L	X	X	L	H	H	L	H
				H	H	X	X	L	H	H	H	L
				X	X	X	X	H	H	H	H	H
L	H	H	H	X	X	X	X	X	H	H	H	H
H	L	X	X	X	X	X	X	X	H	H	H	H

† If $\overline{TP}$ is low, the row and column address latch will be high. If $\overline{TP}$ is high, the row and column address latch will be at the levels entered when LE was last high.

‡ For 'ALS6301, clearing occurs on the low-to-high transition of $\overline{RASI}$; for 'ALS6302, clearing occurs on the high-to-low transition of RASI.

read/write operation details

During normal read/write operations, the row and column addresses are multiplexed to the dynamic RAM controlled by the MSEL input. The corresponding $\overline{RAS}$n and $\overline{CAS}$n output signals strobe the addresses into memory. The block diagram in Figure 1 shows a typical system interface for a four-megaword dynamic memory. The DMC is used to control the four banks of 1M memory.

For systems where addresses and data are multiplexed onto a single bus, the DMC uses latches (row, column, and bank) to hold the address information. Figure 5 shows a typical timing diagram using the input latches. The twenty-two input latches are transparent when latch enable (LE) is high, and latch the input data whenever LE is taken low. For systems in which the processor has separate address and data buses, LE may be permanently high (see timing diagram in Figure 4).

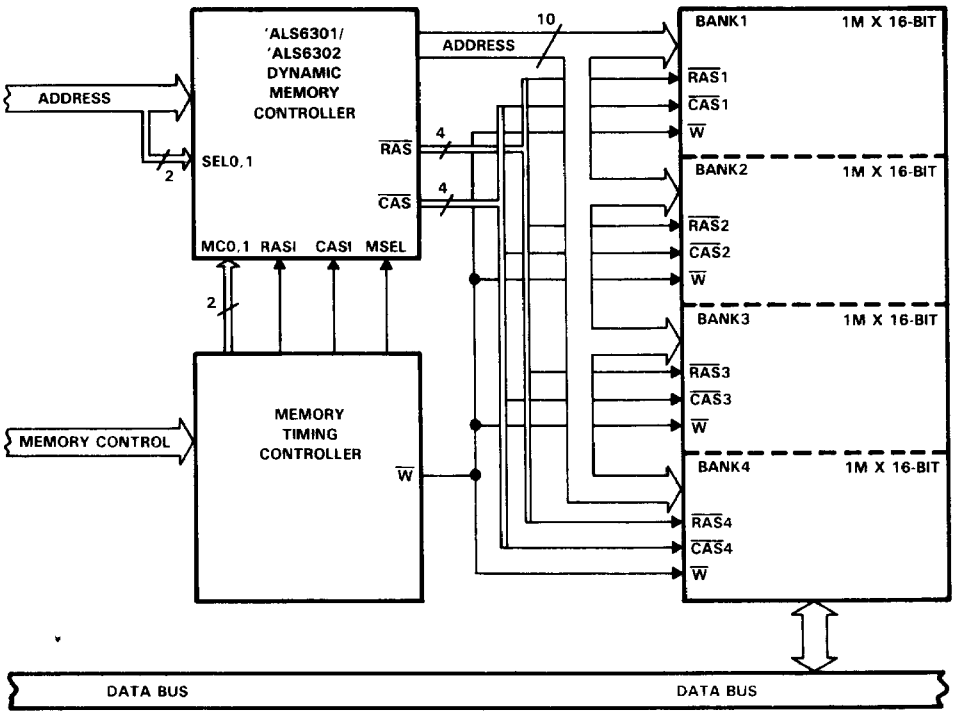


FIGURE 1. 4-MEGAWORD X 16-BIT DYNAMIC MEMORY

read/write operations (continued)

The DMC is designed with heavy-duty outputs that are capable of driving four banks of 16-bit words, including six checkbits used for error detection and correction.

In addition to heavy-duty output drivers, the outputs are designed with balanced output impedances (25 Ω both high and low). This feature optimizes the drive low characteristics, based on safe undershoot, while providing symmetrical drive high characteristics. It also eliminates the external resistors required to pull the outputs up to the MOS V_{OH} level (V_{CC} – 1.5 V).

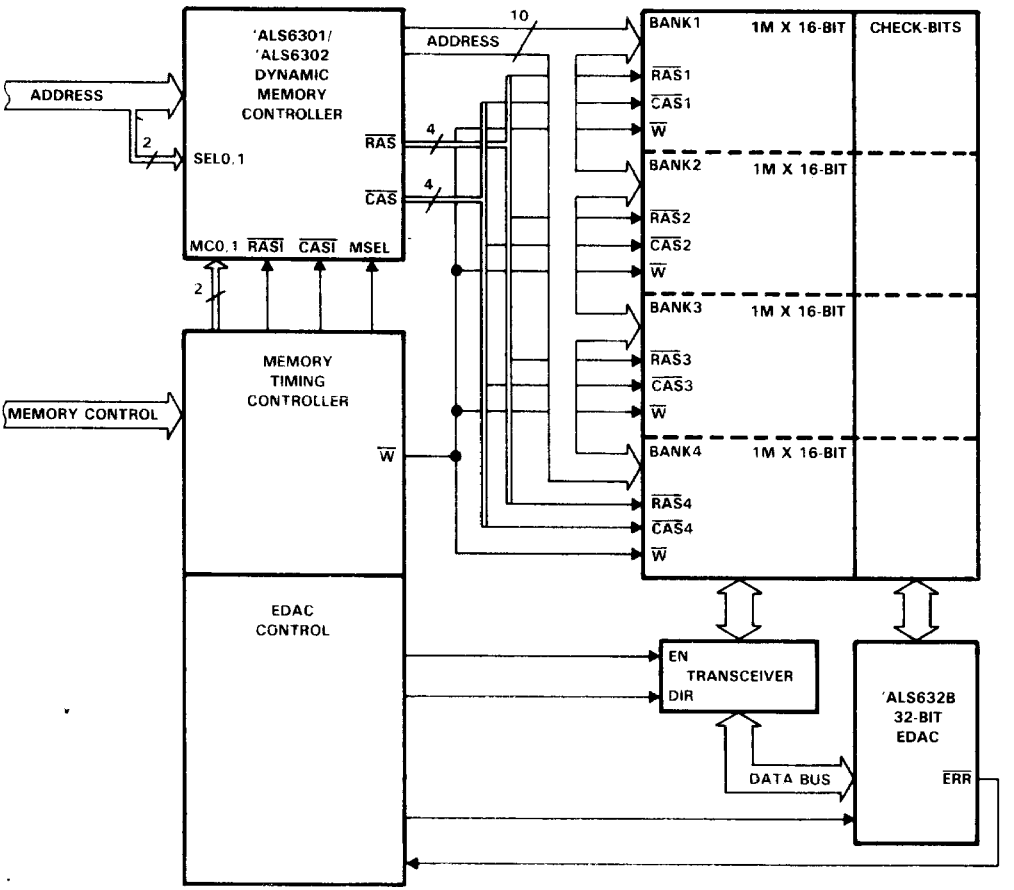


FIGURE 2. 4-MEGAWORD X 16-BIT DYNAMIC MEMORY WITH ERROR DETECTION AND CORRECTION

memory expansion

With a 10-bit address path, the DMC can control up to four megaword when using 1M dynamic RAMs. If a larger memory size is desired, the DMC's chip select ($\overline{CS}$) makes it easy to expand the memory size by using additional DMCs. A sixteen-megaword memory system is shown in Figure 3.

To maintain maximum performance in 32-bit applications, it is recommended that individual bus drivers be used for each bank.

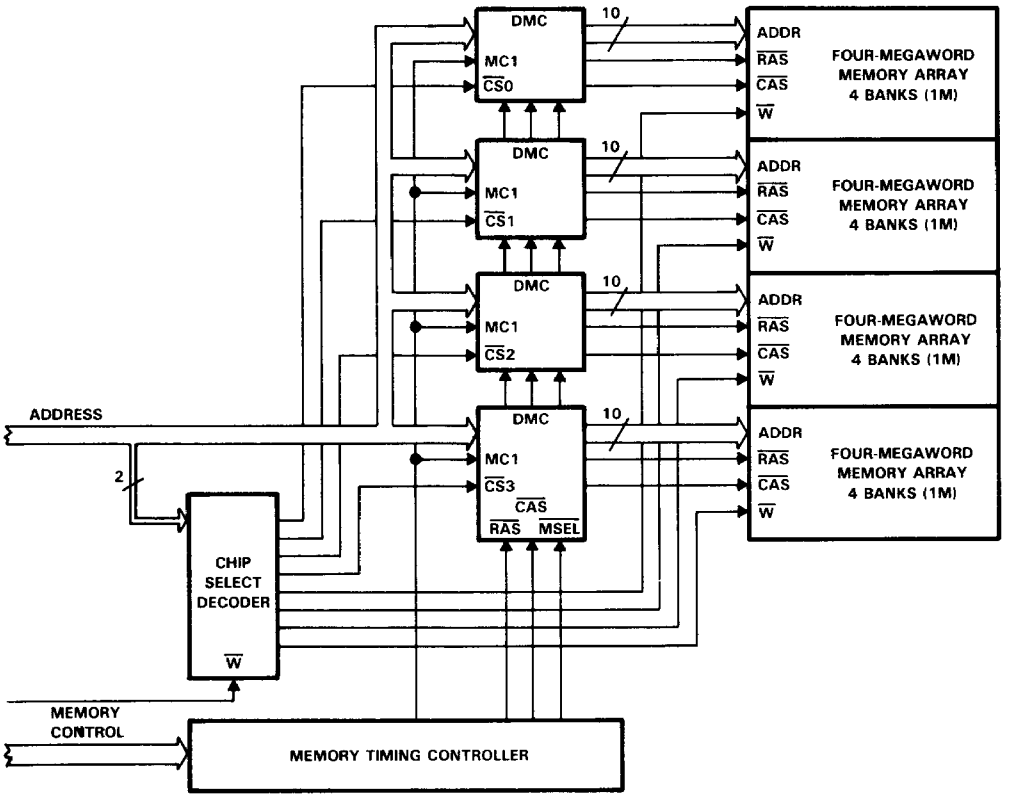


FIGURE 3. 16-MEGAWORD X 16-BIT DYNAMIC MEMORY

refresh operations

The two 10-bit counters in the 'ALS6301 and 'ALS6302 support 128-, 256-, 512-, and 1024-line refresh operations. Transparent, burst, synchronous, or asynchronous refresh modes are all possible. The refresh counters are advanced on the low-to-high transition of $\overline{\text{RASI}}$ on the 'ALS6301, and on the high-to-low transition of RASI on the 'ALS6302. The refresh counters are reset to zero on the low-to-high transition of $\overline{\text{RASI}}$ on the 'ALS6301, and on the high-to-low transition of RASI on the 'ALS6302, if MC1 and MC0 are at a high logic level. See Figure 8 for additional timing details.

When performing refresh cycles without memory scrubbing (MC1 and MC0 both low), all four $\overline{\text{RAS}}$ outputs go low, while all $\overline{\text{CAS}}$ outputs are driven high. Typical timing for this mode of operation is shown in Figure 6.

decoupling

Due to the high switching speed and high drive capability of the 'ALS6301 and 'ALS6302, it is necessary to decouple the device for proper operation. Multilayer ceramic 0.1-μF to 1-μF capacitors are recommended for decoupling. It is important to mount the capacitors as close as possible to the power pins (V_{CC} and GND) to minimize lead inductance and noise. A ground plane is recommended.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage, V_{CC} (see Note 1) . . . . . 7 V
Input voltage . . . . . 7 V
Voltage applied to disabled 3-state output . . . . . 5.5 V
Operating free-air temperature range . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C

†Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions beyond those indicated in the "recommended operating conditions" section of this specification is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: All voltage values are with respect to the GND pins.

recommended operating conditions

			MIN	NOM	MAX	UNIT
V_{CC}	Supply voltage		4.5	5	5.5	V
V_{IH}	High-level input voltage		2			V
V_{IL}	Low-level input voltage				0.8	V
I_{OH}	High-level output current				−2.6	mA
I_{OL}	Low-level output current				12	mA
t_w	Pulse duration	(23) $\overline{RASI}$ low or RASI high	10			ns
		(24) $\overline{RASI}$ high or RASI low	10			
		(25) LE high	10			
t_{su}	Setup time	(26) An before LE↓	5			ns
		(27) SELn before LE↓	5			
		(28) MC0,1 high before $\overline{RASI}$↑ or RASI↓	10			
		(29) SELn before $\overline{RASI}$↓ or RASI↑	5			
t_h	Hold time	(30) An after LE↓	5			ns
		(31) SELn after LE↓	5			
T_A	Operating free-air temperature		0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS		MIN	TYP‡	MAX	UNIT
V_{IK}	V_{CC} = 4.5 V,	I_I = −18 mA			−1.2	V
V_{OH}	V_{CC} = 4.5 V,	I_{OH} = −2.6 mA	2.4	3.2		V
V_{OL}	V_{CC} = 4.5 V,	I_{OL} = 1 mA		0.15	0.5	V
	V_{CC} = 4.5 V,	I_{OL} = 12 mA		0.35	0.8	
I_{OL}	V_{CC} = 4.5 V,	V_O = 2 V	30			mA
I_{OZH}	V_{CC} = 5.5 V,	V_O = 2.7 V			20	μA
I_{OZL}	V_{CC} = 5.5 V,	V_O = 0.4 V			−20	μA
I_I	V_{CC} = 5.5 V,	V_I = 7 V			0.1	mA
I_{IH}	V_{CC} = 5.5 V,	V_I = 2.7 V			20	μA
I_{IL}	V_{CC} = 5.5 V,	V_I = 0.4 V			−0.1	mA
I_O§	V_{CC} = 5.5 V,	V_O = 2.25 V	−30		−112	mA
I_{CC}	V_{CC} = 5.5 V			136	220	mA

‡All typical values are at V_{CC} = 5 V, T_A = 25°C.

§The output conditions have been chosen to produce a current that closely approximates one half the true short-circuit output current, I_{OS}.

'ALS6301 switching characteristics, C_L = 50 pF

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS†	MIN	TYP‡	MAX	UNIT
$t_{pd(1)}$	$\overline{RASI}$	Any Q	V_{CC} = 4.5 V to 5.5 V, T_A = 0°C to 70°C	5	16	30	ns
$t_{pd(2)}$	$\overline{RASI}$	$\overline{RAS}n$		2	10	14	ns
$t_{pd(3)}$	$\overline{CASI}$	$\overline{CAS}n$		2	7	14	ns
$t_{pd(4)}$	Any A	Any Q		3	9	17	ns
$t_{pd(5)}$	MSEL	Any Q		5	13	22	ns
$t_{pd(6)}$	LE↑	Any Q			13	22	ns
$t_{pd(7)}$	LE↑	Any $\overline{RAS}$			13	22	ns
$t_{pd(8)}$	LE↑	Any $\overline{CAS}$			13	22	ns
$t_{pd(9)}$	MC0 or MC1	Any Q		6	14	24	ns
$t_{pd(10)}$	MC0 or MC1	Any $\overline{RAS}$		2	10	15	ns
$t_{pd(11)}$	MC0 or MC1	Any $\overline{CAS}$		2	10	15	ns
$t_{pd(12)}$	$\overline{CS}$	Any Q			13	24	ns
$t_{pd(13)}$	$\overline{CS}$	Any $\overline{RAS}$			7	13	ns
$t_{pd(14)}$	$\overline{CS}$	Any $\overline{CAS}$			9	13	ns
$t_{pd(15)}$	SEL0 or SEL1	Any $\overline{RAS}$			9	15	ns
$t_{pd(16)}$	SEL0 or SEL1	Any $\overline{CAS}$			9	15	ns
$t_{en(17)}$	$\overline{OE}$↓	Any Q			10	18	ns
$t_{en(18)}$	$\overline{OE}$↓	Any $\overline{RAS}$			10	18	ns
$t_{en(19)}$	$\overline{OE}$↓	Any $\overline{CAS}$			10	18	ns
$t_{dis(20)}$	$\overline{OE}$↑	Any Q			12	20	ns
$t_{dis(21)}$	$\overline{OE}$↑	Any $\overline{RAS}$			12	20	ns
$t_{dis(22)}$	$\overline{OE}$↑	Any $\overline{CAS}$			12	20	ns

'ALS6301 switching characteristics, C_L = 150 pF

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS†	MIN	TYP‡	MAX	UNIT
$t_{pd(1)}$	$\overline{RASI}$	Any Q	V_{CC} = 4.5 V to 5.5 V, T_A = 0°C to 70°C	10	20	35	ns
$t_{pd(2)}$	$\overline{RASI}$	$\overline{RAS}n$		3	9	18	ns
$t_{pd(3)}$	$\overline{CASI}$	$\overline{CAS}n$		2	7	18	ns
$t_{pd(4)}$	Any A	Any Q		5	11	18	ns
$t_{pd(5)}$	MSEL	Any Q		5	15	24	ns
$t_{pd(6)}$	LE↑	Any Q			13	24	ns
$t_{pd(7)}$	LE↑	Any $\overline{RAS}$			13	24	ns
$t_{pd(8)}$	LE↑	Any $\overline{CAS}$			13	24	ns
$t_{pd(9)}$	MC0 or MC1	Any Q		8	15	25	ns
$t_{pd(10)}$	MC0 or MC1	Any $\overline{RAS}$		5	10	16	ns
$t_{pd(11)}$	MC0 or MC1	Any $\overline{CAS}$		5	10	16	ns
$t_{pd(12)}$	$\overline{CS}$	Any Q			16	25	ns
$t_{pd(13)}$	$\overline{CS}$	Any $\overline{RAS}$			9	15	ns
$t_{pd(14)}$	$\overline{CS}$	Any $\overline{CAS}$			9	15	ns
$t_{pd(15)}$	SEL0 or SEL1	Any $\overline{RAS}$			10	17	ns
$t_{pd(16)}$	SEL0 or SEL1	Any $\overline{CAS}$			10	17	ns

†See Parameter Measurement Information for load circuit and voltage waveforms.
‡All typical values are at V_{CC} = 5 V, T_A = 25°C.

'ALS6302 switching characteristics, C_L = 50 pF

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS†	MIN	TYP‡	MAX	UNIT
$t_{pd(1)}$	RASI	Any Q	V_{CC} = 4.5 V to 5.5 V, T_A = 0°C to 70°C	5	16	30	ns
$t_{pd(2)}$	RASI	$\overline{RAS}n$		2	10	14	ns
$t_{pd(3)}$	CASI	$\overline{CAS}n$		2	7	14	ns
$t_{pd(4)}$	Any A	Any Q		3	9	17	ns
$t_{pd(5)}$	MSEL	Any Q		5	13	22	ns
$t_{pd(6)}$	LE↑	Any Q			13	22	ns
$t_{pd(7)}$	LE↑	Any $\overline{RAS}$			13	22	ns
$t_{pd(8)}$	LE↑	Any $\overline{CAS}$			13	22	ns
$t_{pd(9)}$	MC0 or MC1	Any Q		6	14	24	ns
$t_{pd(10)}$	MC0 or MC1	Any $\overline{RAS}$		2	10	15	ns
$t_{pd(11)}$	MC0 or MC1	Any $\overline{CAS}$		2	10	15	ns
$t_{pd(12)}$	$\overline{CS}$	Any Q			13	24	ns
$t_{pd(13)}$	$\overline{CS}$	Any $\overline{RAS}$			7	13	ns
$t_{pd(14)}$	$\overline{CS}$	Any $\overline{CAS}$			9	13	ns
$t_{pd(15)}$	SEL0 or SEL1	Any $\overline{RAS}$			9	15	ns
$t_{pd(16)}$	SEL0 or SEL1	Any $\overline{CAS}$			9	15	ns
$t_{en(17)}$	$\overline{OE}$↓	Any Q			10	18	ns
$t_{en(18)}$	$\overline{OE}$↓	Any $\overline{RAS}$			10	18	ns
$t_{en(19)}$	$\overline{OE}$↓	Any $\overline{CAS}$			10	18	ns
$t_{dis(20)}$	$\overline{OE}$↑	Any Q			12	20	ns
$t_{dis(21)}$	$\overline{OE}$↑	Any $\overline{RAS}$			12	20	ns
$t_{dis(22)}$	$\overline{OE}$↑	Any $\overline{CAS}$			12	20	ns

'ALS6302 switching characteristics, C_L = 150 pF

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS†	MIN	TYP‡	MAX	UNIT
$t_{pd(1)}$	RASI	Any Q	V_{CC} = 4.5 V to 5.5 V, T_A = 0°C to 70°C	10	20	35	ns
$t_{pd(2)}$	RASI	$\overline{RAS}n$		3	9	18	ns
$t_{pd(3)}$	CASI	$\overline{CAS}n$		2	7	18	ns
$t_{pd(4)}$	Any A	Any Q		5	11	18	ns
$t_{pd(5)}$	MSEL	Any Q		5	15	24	ns
$t_{pd(6)}$	LE↑	Any Q			13	24	ns
$t_{pd(7)}$	LE↑	Any $\overline{RAS}$			13	24	ns
$t_{pd(8)}$	LE↑	Any $\overline{CAS}$			13	24	ns
$t_{pd(9)}$	MC0 or MC1	Any Q		8	15	25	ns
$t_{pd(10)}$	MC0 or MC1	Any $\overline{RAS}$		5	10	16	ns
$t_{pd(11)}$	MC0 or MC1	Any $\overline{CAS}$		5	10	16	ns
$t_{pd(12)}$	$\overline{CS}$	Any Q			16	25	ns
$t_{pd(13)}$	$\overline{CS}$	Any $\overline{RAS}$			9	15	ns
$t_{pd(14)}$	$\overline{CS}$	Any $\overline{CAS}$			9	15	ns
$t_{pd(15)}$	SEL0 or SEL1	Any $\overline{RAS}$			10	17	ns
$t_{pd(16)}$	SEL0 or SEL1	Any $\overline{CAS}$			10	17	ns

†See Parameter Measurement Information for load circuit and voltage waveforms.
‡All typical values are at V_{CC} = 5 V, T_A = 25°C.

PARAMETER MEASUREMENT INFORMATION

* t_{pd} specified at C_L = 50, 150 pF

CAPACITIVE LOAD SWITCHING

THREE-STATE ENABLE/DISABLE

FIGURE 4. SWITCHING TEST CIRCUIT

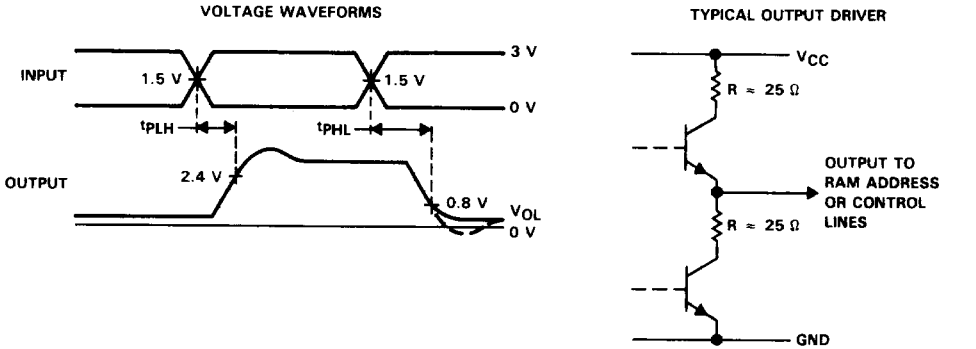
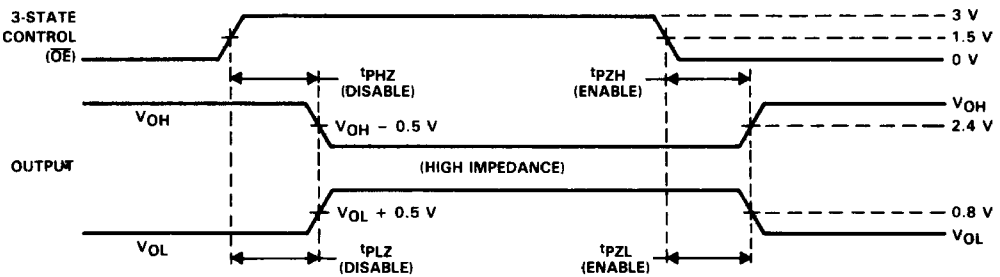


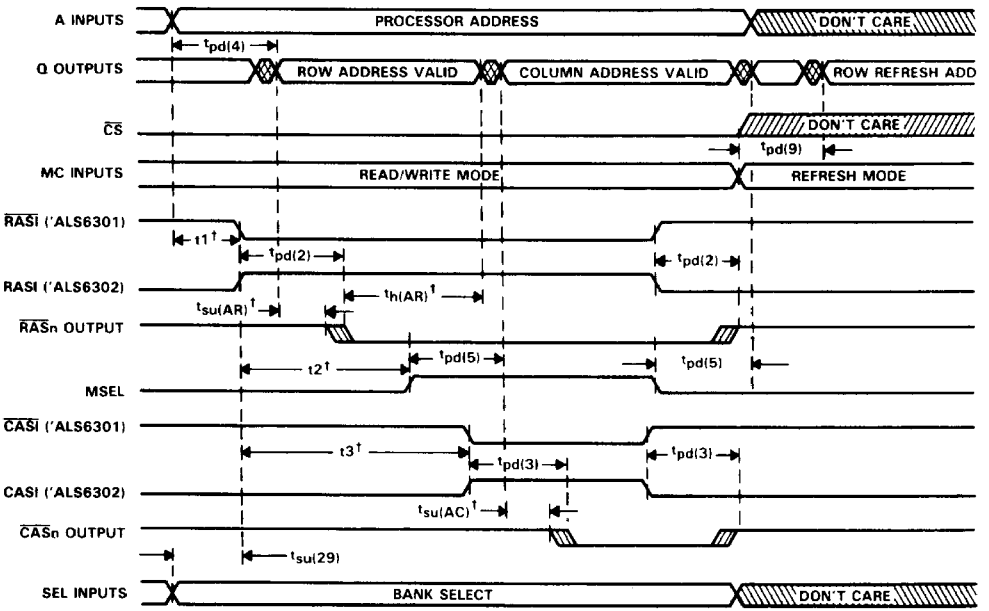
FIGURE 5. OUTPUT DRIVE LEVELS FOR TYPICAL SWITCHING CHARACTERISTICS



NOTE: Decoupling is needed for all AC tests

FIGURE 6. THREE-STATE CONTROL LEVELS

PARAMETER MEASUREMENT INFORMATION



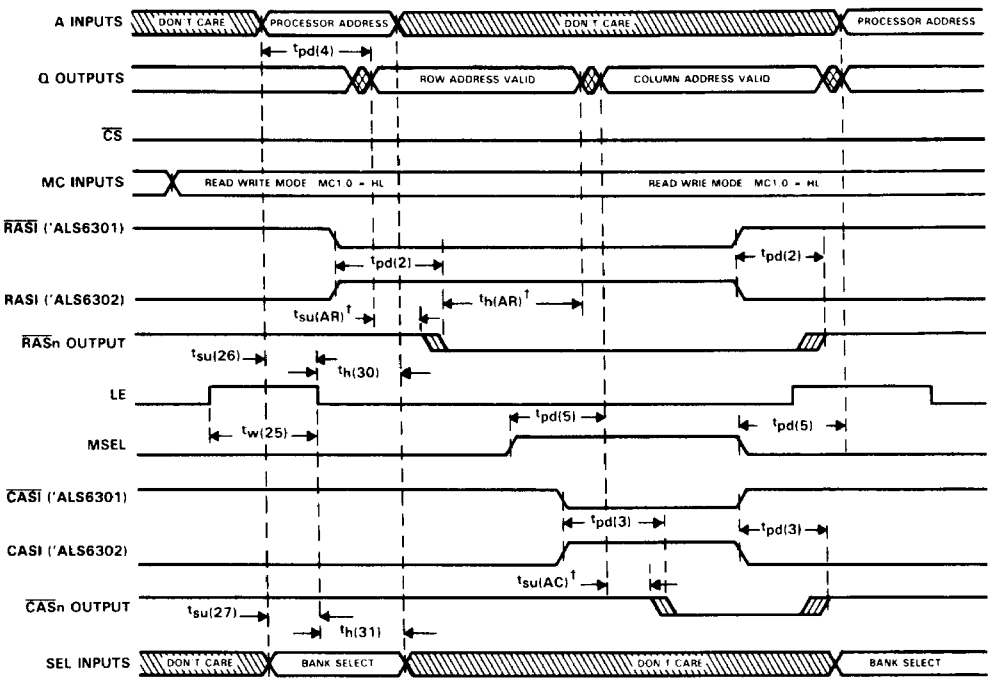
† Parameters $t_{su(AR)}$, $t_{su(AC)}$, and $t_{h(AR)}$ are timing requirements of the dynamic RAM. Parameters t1, t2, and t3 represent the minimum timing requirements at the inputs to the DMC that guarantee DRAM timing specifications and maximum system performance. The minimum requirements for t1, t2, and t3 are as follows:

$t1(min) = t_{pd(4)}\ max + t_{su(AR)}\ min - t_{pd(2)}\ min$
$t2(min) = t_{pd(2)}\ max + t_{h(AR)}\ min - t_{pd(5)}\ min$
$t3(min) = t2\ min + t_{pd(5)}\ max + t_{su(AC)} - t_{pd(3)}\ min$

See the DRAM data sheet for applicable $t_{su(AR)}$, $t_{su(AR)}$, and $t_{h(AR)}$. In addition, note that propagation delay times given in the above equations are functions of capacitive loading. The values used in these equations must relate to actual system capacitive loading.

FIGURE 7. READ/WRITE CYCLE TIMING (MC1, MC0 = 1, 0), (LE = H)

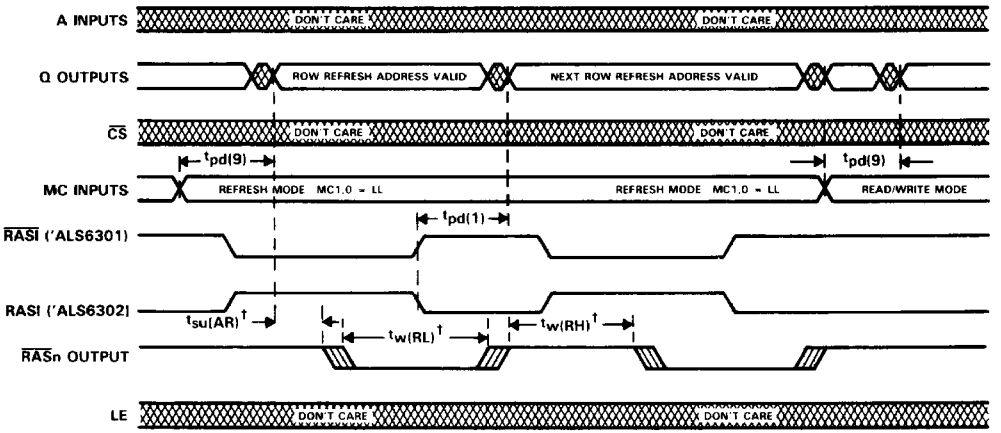
PARAMETER MEASUREMENT INFORMATION



†$t_{su(AR)}$, $t_{su(AC)}$, and $t_{h(AR)}$ are timing requirements of the dynamic RAM. See the DRAM data sheet for applicable specifications.

FIGURE 8. READ/WRITE CYCLE TIMING USING INPUT LATCHES (MC1, MC0 = H, L)

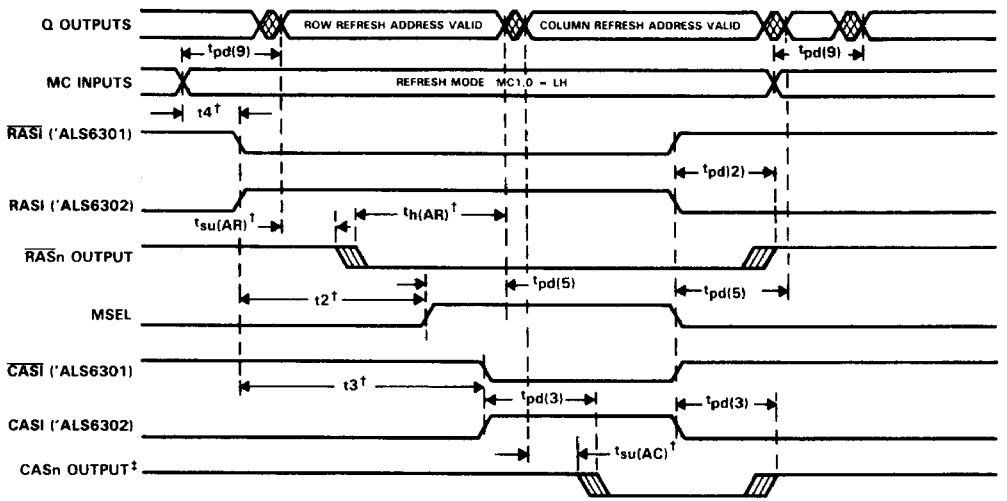
PARAMETER MEASUREMENT INFORMATION



†$t_{su(AR)}$, $t_{w(RL)}$, and $t_{w(RH)}$ are timing requirements of the dynamic RAM. See DRAM data sheet for applicable specifications.

FIGURE 9. REFRESH CYCLE TIMING (MC1, MC0 = L, L) WITHOUT SCRUBBING

PARAMETER MEASUREMENT INFORMATION



† Parameters $t_{su(AR)}$, $t_{su(AC)}$, and $t_{h(AR)}$ are timing requirements of the dynamic RAM. Parameters t2, t3, and t4 represent the minimum timing requirements at the inputs to the DMC that guarantee DRAM timing specifications and maximum system performance. The minimum requirement for t2, t3, and t4 are as follows:

$t2(min) = t_{pd(2)}\ max + t_{h(AR)}\ min - t_{pd(5)}\ min$
$t3(min) = t2\ min + t_{pd(5)}\ max + t_{su(AC)} - t_{pd(3)}\ min$
$t4(min) = t_{pd(9)}\ max + t_{su(AR)}\ min - t_{pd(2)}\ min$

See the DRAM data sheet for applicable $t_{su(AR)}$, $t_{su(AC)}$, and $t_{h(AR)}$. In addition, note that propagation delay times given in the above equations are functions of capacitive loading. The values used in these equations must correspond to actual system capacitive loading.

‡ A $\overline{CAS}$n output is selected by the bank counter. All other $\overline{CAS}$n outputs will remain high.

FIGURE 10. REFRESH CYCLE TIMING (MC1, MC0 = L, H) WITH MEMORY SCRUBBING

PARAMETER MEASUREMENT INFORMATION

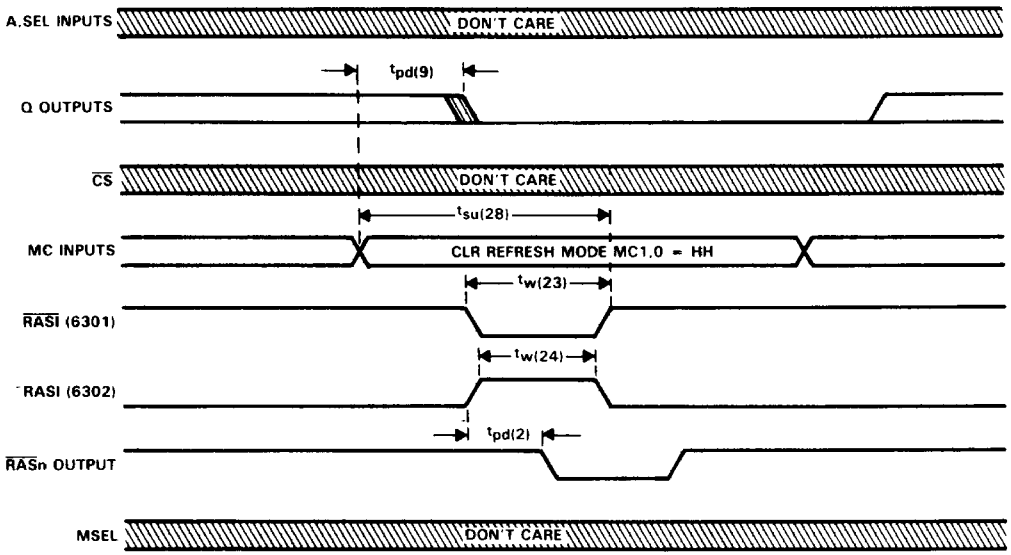


FIGURE 11. REFRESH COUNTER RESET (MC1, MC0 = H, H)

PARAMETER MEASUREMENT INFORMATION

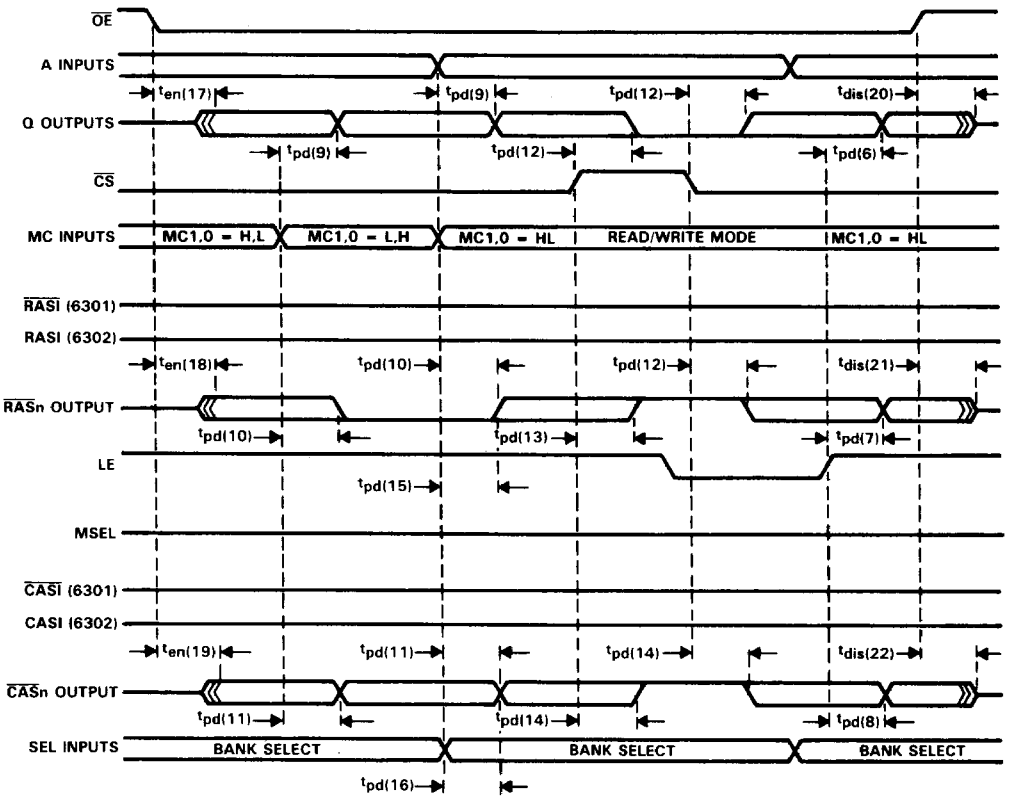


FIGURE 12. MISCELLANEOUS TIMING

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Designing and Manufacturing Surface Mount Assemblies

T-90-20

Elizabeth Gunther, Charles Hutchins, and Paul Peterson

The competitive nature of the semiconductor industry has driven vendors to minimize the size of electronic components, so that more functions can be achieved in a given volume. In addition, improved electrical performance, decreased mass, and the potential for lower system cost are all by-products of compacted packaging and circuitry which hold interest to component manufacturers and users alike.

Surface Mount Technology (SMT) offers an excellent method of reducing component size. A typical memory array can be reduced to 50 percent of its original PWB size with single-sided mounting, and 25 to 30 percent with double-sided mounting. Logic designs cannot achieve the same dramatic reduction, but decreases up to 40 to 60 percent can be achieved for single-sided and double-sided assemblies respectively.

The key design and manufacturing process issues must be understood in order to fully reap the benefits of Surface Mount Technology. This article gives a general overview of the key aspects of design, process, and manufacturing of surface mounted assemblies, and offers surface mount as an opportunity to lower a system's cost without sacrificing reliability.

Components

Most surface mount components are at least one-third the size of the comparable through-hole mounted device (Figure 1). The 68-pin chip carrier is approxmiately one square inch, while the 64-pin DIP is approximately three square inches. The 20-pin chip carrier is slightly larger than 0.1 square inch, while the 20-pin DIP is 0.3 square inch. Similarly, other IC packages are reduced to approximately one-third the size of comparable lead count packages. The passive components occupy approximately one-tenth the board area, and this is why they have been used in most small consumer products built in the last couple of years.

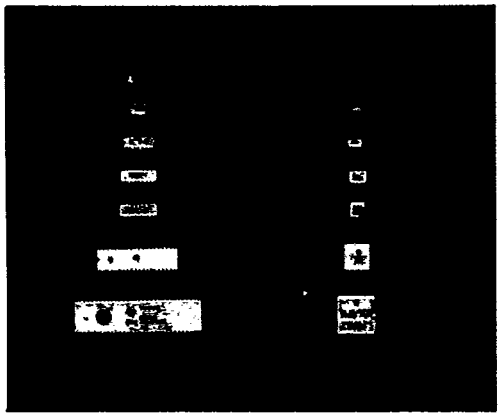

Figure 1. Component Site Reduction

There were many references in the recent past to problems with component availability, cost, and standardization. This area of SMT has probably received more attention than any other. Several recent magazine articles now state that significantly more components (particularly actives) are now available and that cost parity has been achieved on most of them. The effort by various industry committees on standardization has also been effective.

Thus, although more needs to be accomplished in these areas, a designer can begin a project with confidence that there will be no insurmountable barriers in this area. There are several consultants and subcontract assembly companies to assist in this effort. It is strongly recommended that all new designs utilize some form of SMT, particularly when space is an important consideration.

Process

The process to manufacture a surface mount assembly (SMA) is very simple. It consists of four basic steps, as shown in Figure 2. First, the solder paste is screened on the PWB. Then the component is placed on the board, with due care to get it positioned correctly. Typical geometries require placement accuracy of less than plus/minus 4 mils. Next the solder is reflowed with either a vapor phase or infrared system. Finally, the assembly is cleaned and is now ready for test. This process, although simple in concept, relies on board and component planarity and solderability. These are easily achievable with the chip carriers and memory modules we will discuss later.

Texas Instruments has installed a Surface Mount Technology Center at its plant in Houston, Texas. At this center, we have a complete and flexible engineering line to assist our customers in converting to Surface Mount Technology.

The engineering line is equipped with a screen printer, pick and place system, vapor phase reflow, and clean-up station that will easily handle PWBs up to 9″ × 10″. Larger boards up to 14″ × 16″ can be processed with some additional care. TI uses this engineering line to produce its prototype and demo boards. It is also available to any of TI's customers, free of charge, for use in building test or prototype boards.

The effectiveness of the assembly process can be characterized by the number of unacceptable solder joints formed during the process. Unacceptable joints are defined by their electrical and mechanical (strength and reliability) characteristics. The major problem is open solder joints, followed by bridging and misregistration.

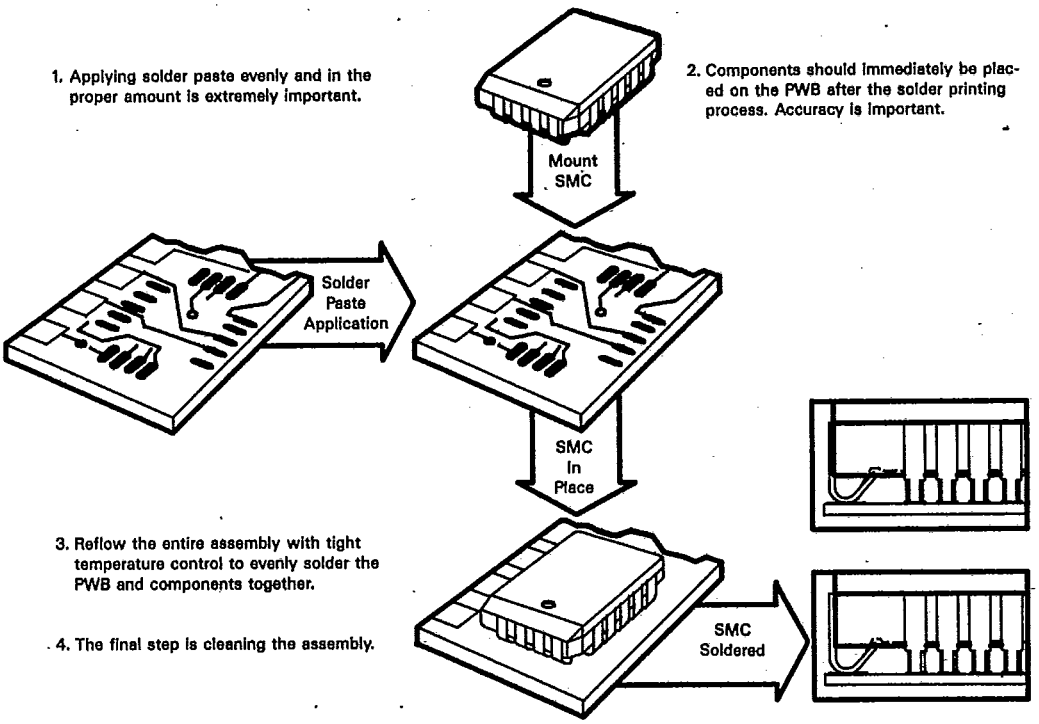

Figure 2. Basic Process Steps

Open circuits are detected at electrical test and are the first defects detected after soldering. At Texas Instruments, 10 PPM or less is the desirable defect level. Several factors that contribute to open solder joints were identified during production start-up. Lead tip planarity of the J-leaded plastic chip carriers is the most important factor in obtaining acceptable process yields. Lead position, lead finish, solder paste composition, and PWB solderability affect process yield as well.

Experiments in which lead tip planarity was confined to specific limits between 1 to 7 mils indicate that a 2 mil planarity requirement produces acceptable results with the process currently in use. Little gain in yield was noted at a 1 mil planarity requirement.

Another interesting result showed that silver in the process, either as a lead finish or in the solder paste, improves yields significantly. One explanation may have to do with the dynamics of the solder during the reflow process as they are affected by the different surface forces acting in the silver and non-silver process.

Design

The design of the PWB, in addition to providing the component interconnections, will provide the proper amount and correct placement of solder paste for a strong fillet formation. The wave soldering process, by comparison, provides a semi-infinite amount of solder, whereas the SMT process will provide only a predetermined amount. Thus, the component connection pad must be correctly placed and be of the proper size.

Further, consideration must be given for inspection, testing, and rework. The density achievable can lead to severe problems at these points if understanding and due care are not exercised in the design. The project team should include members from manufacturing, testing, QA, and purchasing, in addition to the design engineers, from the start. The design and processing of test boards is strongly recommended to provide experience and direction for the major project.

A very practical set of design guidelines is given in Figure 3. These have been used on a number of SMT designs and have given good results. With proper manufacturing techniques as described later, a high yield can be achieved. Component spacings should be approximately equal to the height of the tallest component. This allows an angle of 45 degrees for visual inspection of test probes.

Figure 4 shows the standard footprint for all Small Outline (SO) packages. The larger and more important fillet of an SO package is on the inside of the gull-wing lead. The solder pad, or land, should therefore be designed to extend slightly under the body of the package in order to optimize this fillet. From Table 1 we can see all packages have 50 mil centers with 25 mil spacings between lands. This allows the designer enough space to put traces between pads, and also reduces the occurrence of solder bridging of adjacent lands. Table 1 also summarizes the suggested land lengths and placement, depending on the terminal count of the SO. While not an absolute solution, these land sizes offer a conservative design solution that will meet most vendors' specifications and provide a mechanically and electrically sound solder joint.

● Geometries	
• Trace Width/Space	8/8 MIL Min., 10/10 MIL Typ.
• IC Lead Solder Pad Size	25 ± 5 MIL × 70 ± 10 MIL
• Via Hole Size	20 MIL DIA
• Via Pad Size	40 MIL DIA
• Cap/Resistor Pad Size	W = MAX Dimensions of Component L = 20 MIL Beyond Metallization 10 MIL Inside Metallization
• Solder Mask	5 MIL Larger than IC/Component Pad

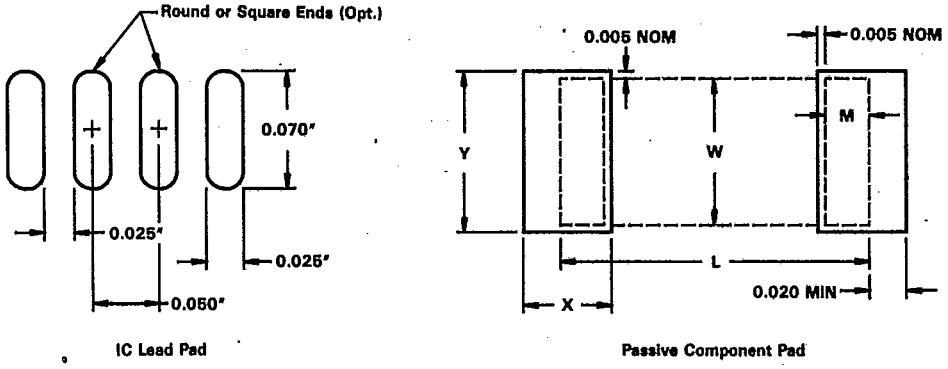

Figure 3. PWB Design Guidelines

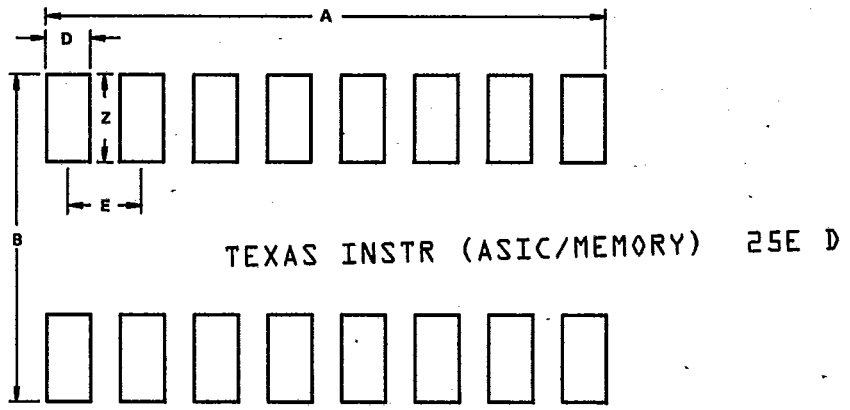

Figure 4. Standard SOIC Footprint

Table 1. SOIC Footprint Dimensions

No. of Terminals	A	B	Z	D	E
8	.175	.250	.050	.025	.050
14	.325	.250	.050	.025	.050
16	.375	.250	.050	.025	.050
20	.475	.430	.070	.025	.050
24	.575	.430	.070	.025	.050

Test	4164A PLCC	4164 DIP	Units
Life Test, 125°C	42	64	Fits*—60% UCL
85°C/85% RH	0.17	0.37	%/1000 Hours
Autoclave	0.17	0.96	%/240 Hours
T/C—65/150	0.52	1.44	%/1000 Cycles
T/C 0/125	0.0	0.0	%/2000 Cycles

*Derated to 55°C Assuming 0.5EV Activation Energy

Figure 5. Failure Rate Comparison 4164A PLCC VS DIP

Manufacturing

The SMT manufacturing area must have the following basic equipment:

- Solder Paste Printer
- Component Pick and Place Machine
- Solder Paste Reflow Machine
- Clean-up System
- Inspection/Process Control Aids
- Electrical Test

The criteria for choosing the above is determined mainly by the size(s) and quantity of PWBs per month, the gross number of components per PWB, and the number of different components per PWB.

The size of the largest PWB is an important criterion in the choice of all of the major items. The printer, pick and place, reflow, and clean-up must all be able to handle it with no difficulty or process nonuniformity. The number and size of the various PWBs that may be produced will secondarily be considered for ease of set up and changeover in the printer and pick and place. The pick and place machine(s) will probably be the most expensive item in the list above and therefore, should get the most attention.

The gross number of components and PWBs will provide data for choosing the pick and place. Component per hour placement speed should be checked in actual operation, as the interrelationship may affect ultimate speed. The number of different components per board will determine how many feeders and what types of feeders will be required. This is a very key issue, as well as the accuracy of placement.

Reflow

The solder reflow is easily achieved with any of the commercially available equipment. Subtle differences between vapor phase, either batch or in-line, and infrared are overshadowed by the choice of solder paste and the solderability/planarity issue. A batch vapor phase is extremely flexible for different sizes of boards with different component counts. The in-line vapor phase is a good choice for a more automated processing line with standard or similar sized boards. The infrared has the advantage of being less expensive to operate, but requires more alteration to set up the time-temperature profile for a different size PWB. This would be a minimal problem on a manufacturing line building high volumes of the same board.

Clean-up

The most popular flux for SMT is the mildly activated rosin flux (RMA). This was developed in the days of vacuum tube assembly when clean-up was next to impossible. It is noncorrosive but provides sufficient fluxing action for good quality components and PWBs. Thus it is the preferred choice for SMAs with small spacings under most passives and SOICs, where complete cleaning is difficult. A mild solvent, such as Freon TMS, is generally sufficient to achieve a good visual cleanup, and there are several systems available that provide hot vapor, spray, or ultrasonic de-fluxing.

Reliability

With the smaller surface mount packages, there is some concern about component reliability. Texas Instruments addressed the overall DRAM reliability issue several years ago. Through an extensive task force effort, the major problems of the life test, humidity performance, and temperature cycle were identified. The best solutions to these problems required several changes in the design and process of the silicon chip. In doing so, the reliability of the DRAM chip became independent of the package used. Thus, the 64K DRAM in the plastic chip carrier package performs equivalently to the same chip in a DIP as shown in Figure 5. Similar data is available on most semiconductor ICs.

An additional reliability concern originates in the surface mount solder reflow process, which submits components to higher reflow temperatures more suddenly than the wave-soldering methods of DIP components, with oftentimes repeated reflow cycles for rework and repair.

The best method for resolving this issue involves comparing the temperature-time differential of the vapor phase or infrared solder reflow process to the standard temperature

cycling reliability tests to which surface mount components are routinely submitted. Figures 6 and 7 show temperature profiles of the vapor phase and infrared solder reflow processes. In the vapor phase process, the maximum temperature change with time is:

$$\frac{215°C - 25°C}{45 \text{ sec}} = \frac{190°C}{45 \text{ sec}}$$

equaling approximately 4°C/sec. The infrared solder reflow method submits the ICs to a similar, yet less severe temperature over time change of 3°C/second. Comparing these temperature profile ramp-ups to that which a surface mount component undergoes in a temperature cycling reliability test proves that there should be no concern over damage to the component during reflow. In the temp cycling test, the surface mount components were submitted to 1000 cycles of sudden cycling from 150°C to −65°C within three seconds. This represents a temperature-time differential of:

$$\frac{150°C-(-65°C)}{3} = \frac{215°C}{3 \text{ sec}} = \frac{70°C}{\text{sec}}$$

with less than 0.5 percent failures.

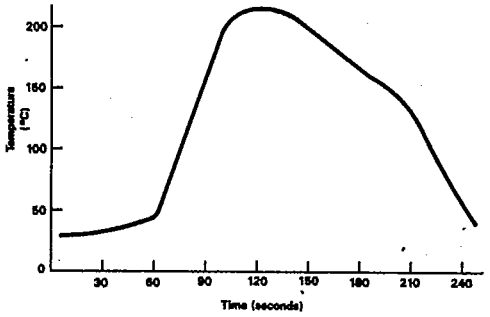

Figure 6. Typical Temperature Profile for In-Line Vapor Phase Reflow

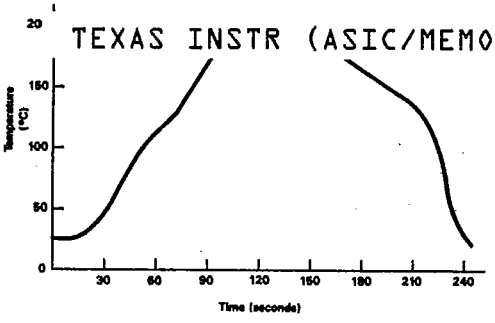

Figure 7. Typical IR Reflow System Profile

Since the surface mounted components were able to withstand a 70°C/second temperature change of 1000 cycles, they should be able to withstand the less severe conditions of a 4°C/second damage during reflow without reliability degradation.

Another concern in the solder reflow processing of surface mount components is the dwell time in reflow temperatures of 215°C or above. The dwell time for a small PWB populated with surface mount devices is about 20 seconds. For a larger board of about 10"×12" up to 50 seconds is needed for reflow. A generalized component degradation curve, relating accumulated time and temperature, can be assumed to exist. The shape of the curve for this discussion is assumed to be a decaying parabolic for simplicity and conservatism. There are two generally known points of this curve. The flame retardant mold compound (FRMC) of a plastic package starts to break down at 300°C in two to three seconds. Also, the molding and curing of a surface mount device is performed over several hours at 175°C. These two points are shown on the generalized curve shown in Figure 8, with the "safe" region being the area under the curve. Two points that fall within this region are the industry standard practice of solder dipping leads of several types of ICs, and of the soldering plastic devices on the bottom with Type III surface mount assembly, each submerges the component for three to four seconds in a solder wave.

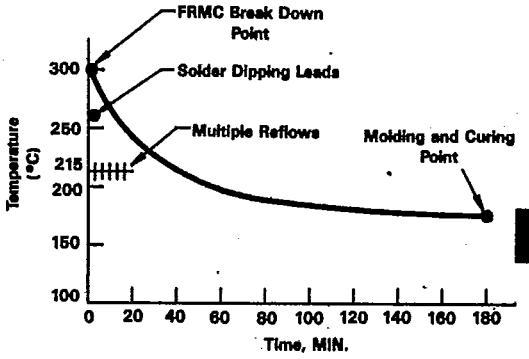

Figure 8. General Plastic Degradation Curve

Summary

Surface mount assembly techniques provide a significant advantage in cost, volume, and reliability over the current "thru-hole" technology. These are well documented, and the manufacturing equipment and related products are becoming readily available to support new production lines. Also, as experience grows, improved products and ideas are developed from the cooperative efforts of vendors and users in standardization organizations and in problem-solving sessions. The broad selection of package types and product technologies available now are sufficient to begin conversion of existing electronic system products for size reduction or feature enhancement. Definitely, new products should be designed with surface mount technology.