

# Digilent Pmod™ Interface Specification

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## Introduction

The Digilent Pmod interface is used to connect low frequency, low I/O pin count peripheral modules to host controller boards. There are six-pin and twelve-pin versions of the interface defined. The six-pin version provides four digital I/O signal pins, one power pin and one ground pin. The twelve-pin version provides eight I/O signal pins, two power pins and two ground pins. The signals of the twelve-pin version are arranged so that it provides two of the six-pin interfaces stacked.

In general, Pmod peripheral modules can plug directly into connectors on the host controller board, or be connected to the controller board via six-pin or twelve-pin cables. Two six-pin peripheral modules can be connected to a single twelve-pin host connector via a twelve-pin to dual six-pin splitter cable. Similarly, a single twelve-pin peripheral module can be connected to two six-pin host connectors via the same twelve-pin to dual six-pin splitter cable.

Pmod peripheral modules are powered by the host via the interface's power and ground pins.

The Pmod interface is not intended for high frequency operation, however, using RJ45 connectors and twisted pair Ethernet cable, signals have been sent reliably at 24Mhz and distances of up to 4 meters.

In addition to the six and twelve pin interfaces, the Pmod peripheral module interface also encompasses a variant using the I<sup>2</sup>C interface, and two or four wire MTE cables. In some cases, an I<sup>2</sup>C connected module can be connected directly to a Pmod connector on a system board, but generally the connection will be via MTE cables. The Pmod I<sup>2</sup>C interface provides the two I<sup>2</sup>C signals, SDA and SCL, plus power and ground.

## Electrical Specifications

The digital signal characteristics are not specified. However, the general expectation is that a 3.3V logic power supply will be used and the signals will conform to LVCMOS 3.3V or LVTTL 3.3V logic conventions.

The driver current source/sink capability isn't specified and depends on the capabilities of the specific system board or module. The I/O pins on the system board are generally directly driven by the FPGA or microcontroller. The I/O pins on Xilinx FPGAs generally have symmetrical 24mA source/sink capability. The drive capability of microcontrollers is generally less and some of them are not symmetrical. The drive strength for microcontroller pins is generally in the range +/-5mA to +/-10mA.

The I/O pins on system board Pmod connectors generally have ESD protection diodes and 200ohm series resistors. The resistors are to limit short circuit currents if pins are inadvertently shorted, or to protect against driver conflicts if outputs are inadvertently connected together.

Peripheral modules may be connected to the host via cables of up to 18" in length. The drivers on the host or peripheral module should have sufficient drive strength to drive this length of cable at

whatever the operating speed of the interface on the Pmod is expected to be. In general, this means that the driver should be able to source or sink at least 5mA of current.

Peripheral modules may not assume that pull-up or pull-down resistors are present on the host and must provide for proper termination of inputs, if necessary, and may not use open drain or open collector outputs, unless the pull-up is provided on the peripheral module itself.

For I<sup>2</sup>C connected modules, the digital signal characteristics conform to the I<sup>2</sup>C specification. Either 5V or 3.3V levels can be used on most modules, but Digilent system boards operate at 3.3V, and the modules are primarily intended for operation at 3.3V

The driver current sink capability isn't specified and depends on the capabilities of the specific system board or module. The I/O pins on the system board are generally directly driven by the FPGA or microcontroller. The I/O pins on Xilinx FPGAs generally have symmetrical 24mA source/sink capability. The drive capability of microcontrollers is generally less and some of them are not symmetrical.

The I<sup>2</sup>C bus is an open collector bus. The pull-up resistors used to provide the logic high level are not provided on the modules and therefore must be provided on the system board. Some Digilent system boards use current mirrors rather than simple pull-up resistors to provide the logic high level to allow driving longer busses with greater capacitive load.

Microcontroller system boards are generally provided with dedicated I<sup>2</sup>C connectors and provide pull-up resistors that are jumper selectable to be in or out of circuit. FPGA based system boards generally do not provide dedicated I<sup>2</sup>C connectors, and depend on the internal pull-up resistors in the FPGA I/O blocks to provide the pull-ups.

## Power Supply

The power pins of the interface provide power from the host to the peripheral. The complete interface requires that the host provide the ability to switch the voltage on the power pins between 5.0V and 3.3V. A reduced functionality subset of the spec. allows the host to provide only 3.3V at the power supply pins, with no ability to switch. On the twelve-pin version of the interface, both power supply pins switch together and always supply the same voltage. These pins may be shorted together at either the host end or the peripheral end.

On I<sup>2</sup>C connected modules, the power pins of the interface provide power from the system board to the peripheral module. The supplied voltage will generally be 3.3V, but operation at 5V is supported by some modules. The connector on the modules provides two sets of the I<sup>2</sup>C signals and the power and ground pins to allow daisy chaining multiple modules onto the bus. The two power pins and the two ground pins may be shorted together respectively at either the system board end or the peripheral module end of the connection.

The amount of power a peripheral module is allowed to draw from the host is not specified, but should not be assumed to be more than approximately 100mA.

## Physical Connection Standard

Pmod connections are made using standard 100mil spaced, 25mil square, pin-header style connectors.

The peripheral module board will have a male connector. This will typically be a right angle connector, at the board edge, for direct connection to a host board, This can be a straight male connector inboard from the board edge if only cable connections will be used.

The host board will typically have a right angle female connector at the board edge for direct connection of peripheral module boards. This connector can be a straight male connector inboard from the board edge if only cable connections will be used.

When multiple connectors are placed side-by-side along a board edge (either host or peripheral), the connectors are spaced 0.9", center-to-center. This allows for 0.8" wide modules to be plugged side-by-side into a host without interference. Peripheral modules with multiple connectors must also have them spaced on 0.9" centers for direct connection to a host.

Peripheral modules with a single connector that are intended for direct connection to a host, or that are intended to fit into the Pmod mounting clip, should be 0.8" wide. There should also be >25mil of clearance from the board edge to any components to allow clearance for the Pmod clip to latch the board edge. The connector should be centered along the 0.8" side of the module.

Peripheral modules that are more than 0.8" wide can be directly connected to a host in some cases but may interfere with adjacent connectors on the host.

The following diagrams show physical connector placement and pin numbering conventions for the host (system board) and peripheral module sides of the connection. Note that the pin numbering conventions for the 2x6 connectors are non-standard and are mirrored between the host connector and the peripheral board connector.

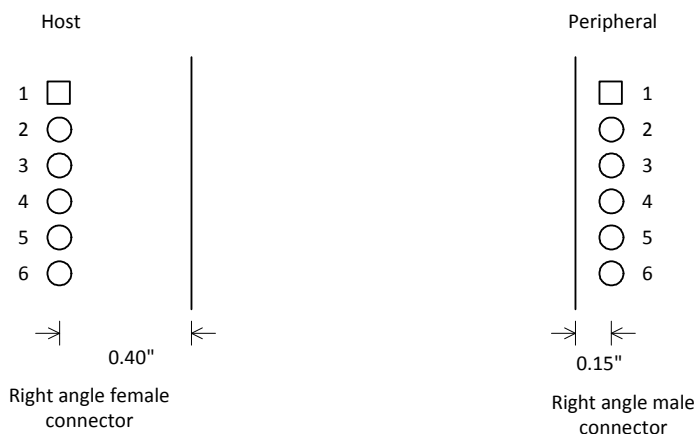


Fig 1: Standard Six-Pin Connector Placement

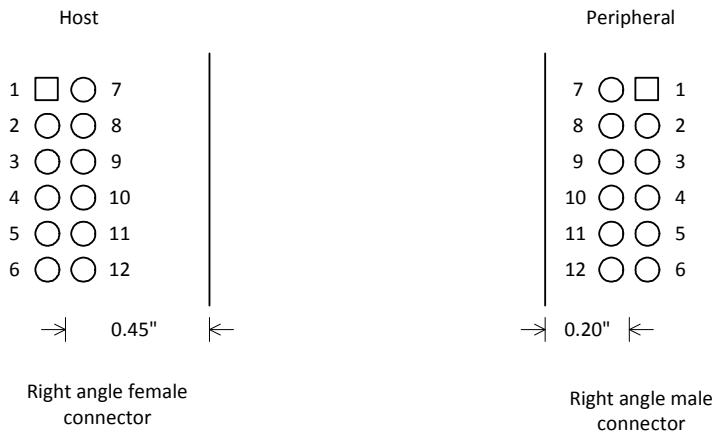


Fig 2: Standard Twelve-Pin Connector Placement

The connection standard for system boards that provide I<sup>2</sup>C connectors is to use a 2x4 male, 100 mil spaced, pin header connector with straight pins. This connector is generally not near a board edge, as the intent is to use cable connections rather than directly plugging the module into the connector. The connector provides two sets of the I<sup>2</sup>C signals, power and ground, so that the I<sup>2</sup>C bus can be formed by daisy chaining system boards or Pmods. The system board can either be the root of one or two daisy chains, or in the middle of a daisy chain.

Pmods with I<sup>2</sup>C interfaces will also have a 2x4 pin header connector so that the module can be included in a daisy chain of modules and system boards. The I<sup>2</sup>C connector can either be a right angle male connector at the board edge if reason to restrict overall module height or a straight male connector anywhere on the board if there is no reason to restrict module height. Some modules have both an SPI and an I<sup>2</sup>C interface. In this case the SPI interface will appear on a 2x6 right angle male connector conforming to the above placement conventions, and the I<sup>2</sup>C interface will appear on a 2x4 straight male connector inboard from the board edge.

The following diagram shows basic PCB dimensions, physical connector placement and pin numbering conventions for the module circuit boards intended to make use of Pmod clips or for direct connection to system boards. Note that the connector is offset from the center of the board. This offset allows I<sup>2</sup>C modules to be plugged into Pmod connectors on some boards with the appropriate pin offset so that the power and ground pins will mate appropriately and keep the module within the same geometry as a Pmod.

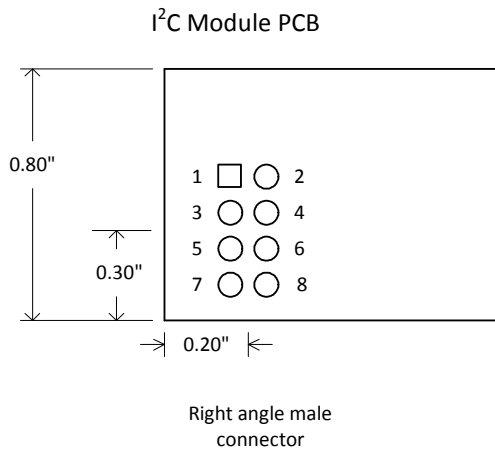


Fig 3: Standard Module Dimensions

Some early Digilent microcontroller based system boards have different connector layouts for the I<sup>2</sup>C connectors. Some have two sets of 2x2 connectors, one for signals, and the other for power and ground. One board has a 2x4 connector, but with the power and grounds reversed. All system boards going forward should use a 2x4 connector with the signal assignments as described below in the I/O Signal Assignment Conventions section.

Digilent has 2-wire MTE cables and a four wire cable specifically intended for I<sup>2</sup>C connections. The four wire cable has a 4-position MTE shell on one end and two 2-position MTE shells on the other end. This cable can be used to connect any Pmod with a standard (four wire) I<sup>2</sup>C connector to any Digilent system board.

## I/O Signal Assignment Conventions

The following define standard signal assignments to the I/O pins on the connector for certain standard interfaces. In the following, the direction is defined from the perspective of the host: i.e. 'Out' means from the host to the peripheral; 'In' means from the peripheral to the host. Generally the host is a Digilent system board (e.g. Nexys II or Cerebot 32MX4). The peripheral will generally be a Digilent Pmod peripheral module.

### I2C Interface

Pin Number	Signal	Pin Number	Signal
1	SCL	2	SCL
3	SDA	4	SDA
5	GND	6	GND
7	VCC	8	VCC

### Pmod Interface Type 1 (GPIO)

This interface is used for general purpose logic. The host must provide the ability for all signals to be bi-directional logic signals. The peripheral may use any of the pins as inputs, outputs, or bi-directional.

Pin	Signal	Direction
1	IO1	In/Out
2	IO2	In/Out
3	IO3	In/Out
4	IO4	In/Out
5	GND	
6	VCC	

### Pmod Interface Type 2 (SPI)

This provides a Serial Peripheral Interface (SPI) port. The host generally acts as an SPI master device and the peripheral module generally acts as an SPI slave device. When this interface is placed on a 12-pin connector on a host, it should use pins 1-6 (i.e. the upper row of pins).

Pin	Signal	Direction
1	SS	Out
2	MOSI	Out
3	MISO	In
4	SCK	Out
5	GND	
6	VCC	

SS - Slave Select. Active low to enable slave device  
 MOSI - Master Out Slave In. Data from master to slave

- MISO - Master In Slave Out. Data from slave to master  
 SCK - Serial clock. Data clock from master to slave

## Pmod Interface Type 2A (expanded SPI)

This provides an SPI interface plus additional control signals. Many SPI devices provide additional control or status signals that can provide additional functions between the master and slave devices. The host generally acts as an SPI master device and the peripheral module generally acts as an SPI slave device.

Pin	Signal	Direction
1	SS	Out
2	MOSI	Out
3	MISO	In
4	SCK	Out
5	GND	
6	VCC	
7	INT	In
8	RESET	Out
9	N/S	N/S
10	N/S	N/S
11	GND	
12	VCC	

- SS - Slave Select. Active low to enable slave device  
 MOSI - Master Out Slave In. Data from master to slave  
 MISO - Master In Slave Out. Data from slave to master  
 SCK - Serial clock. Master provides the clock to shift the data  
 INT - Interrupt signal from slave to master  
 RESET - Reset signal for master to reset slave  
 N/S - not-specified, depending on the module, these pins may be unconnected or additional module specific inputs or outputs.

## Pmod Interface Type 3 (UART)

This provides a UART interface with optional RTS/CTS handshaking. When this interface is placed on a twelve-pin connector on a host, pins 1-6 should be used (i.e. the upper row of pins). The RTS/CTS handshaking signals are optional, and some Pmods do not use them. In this case, pins 1 & 2 are not used.

NOTE: This interface definition is deprecated. System boards and peripheral module boards designed before 07/2010 use this signal definition. This has been superseded by Pmod Interface Type 4 below. When making connections between a Type 3 UART connection and a Type 4 UART connection, a flying lead cable or crossover cable is required.

Pin	Signal	Direction
1	CTS	Out
2	RTS	In
3	RXD	In
4	TXD	Out
5	GND	
6	VCC	

- CTS - Permission for peripheral to send data to host
- RTS - Request from peripheral to send data to host
- RXD - Data from peripheral to host
- TXD - Data from host to peripheral

## Pmod Interface Type 4 (UART)

This provides a UART interface with optional hardware flow control. When this interface is placed on a twelve-pin connector on a host, pins 1-6 should be used (i.e. the upper row of pins). The hardware flow control signals are optional, and some Pmods do not use them. In this case pins 1 & 4 are not used.

The hardware flow control signal names are defined from the system board perspective. The RTS signal is an output indicating that the device (host or peripheral) is ready to receive data. The device asserts this signal low when it is ready to receive data. The CTS signal is an input to the device (host or peripheral). The device will only transmit data when the CTS input is asserted low. A peripheral module that uses hardware flow control will connect the host's RTS signal to its internal CTS input and the host's CTS signal to its internal RTS output.

**NOTE:** This interface type supersedes the Type 3 UART interface. System and peripheral module boards designed after 07/2010 use this signal definition for UART connectors. When making connections between the Type 3 UART interface and the Type 4 UART interface, a flying lead cable or crossover cable is required.

The change in UART signal definition from Type 3 UART to Type 4 UART was motivated by the fact that some microcontroller families (notable some Microchip PIC32 parts) have serial interface controllers that support both SPI operation and UART operation. This signal definition allows system boards using those microcontroller chips to have Pmod connectors that can support both SPI and UART on the same connector.



Pin	Signal	Direction
1	CTS	In
2	TXD	Out
3	RXD	In
4	RTS	Out
5	GND	
6	VCC	

- CTS - Device will only transmit when this signal is asserted  
 RTS - Device is ready to receive data  
 RXD - Data from peripheral to host  
 TXD - Data from host to peripheral

### Pmod Interface Type 4A (expanded UART)

This provides a UART interface with optional hardware flow control plus additional control signals. The hardware flow control signals are optional, and some Pmods do not use them. In this case pins 1 & 4 are not used.

The hardware flow control signal names are defined from the system board perspective. The RTS signal is an output indicating that the device (host or peripheral) is ready to receive data. The device asserts this signal low when it is ready to receive data. The CTS signal is an input to the device (host or peripheral). The device will only transmit data when the CTS input is asserted low. A peripheral module that uses hardware flow control will connect the host's RTS signal to its internal CTS input and the host's CTS signal to its internal RTS output.

Pin	Signal	Direction
1	CTS	In
2	TXD	Out
3	RXD	In
4	RTS	Out
5	GND	
6	VCC	
7	INT	In
8	RESET	Out
9	N/S	N/S
10	N/S	N/S
11	GND	
12	VCC	

- CTS - Device will only transmit when this signal is asserted  
 RTS - Device is ready to receive data  
 RXD - Data from peripheral to host  
 TXD - Data from host to peripheral  
 INT - Interrupt signal from peripheral to host  
 RESET - Reset signal for host to reset peripheral

N/S - not-specified, depending on the module, these pins may be unconnected or additional module specific inputs or outputs.

## Pmod Interface Type 5 (H-Bridge)

This interface provides for controlling a single H-Bridge with motor speed sensing feedback. The DIR pin sets the rotational direction of the motor. The EN signal is pulse width modulated to control the effective voltage applied to the motor. EN is an active high signal, i.e. a high logic level enable current flow through the bridge. The SA and SB signals are quadrature encoder feedback signals used to sense the motor speed. These are square wave signals, whose frequency is proportional to motor rotational speed and that are in quadrature. (i.e. 90° out of phase).

Pin	Signal	Direction
1	DIR	Out
2	EN	Out
3	SA	In
4	SB	In
5	GND	
6	VCC	

DIR - Motor direction  
 EN - Motor enable, active high  
 SA - feedback sense A  
 SB - feedback sense B

## Pmod Interface Type 6 (dual H-Bridge)

This interface provides for controlling two independent H-Bridges. This can be used to control two brushed DC motors, or the two phases of a bi-polar stepper motor.

Pin	Signal	Direction
1	DIR1	Out
2	EN1	Out
3	DIR2	Out
4	EN2	Out
5	GND	
6	VCC	

DIR1 - Motor/Phase 1 direction  
 EN1 - Motor/Phase 1 enable, active high  
 DIR2 - Motor/Phase 2 direction  
 EN2 - Motor/Phase 2 enable, active high

Revision History:

11/20/2011(Gene Apperson)  
Added descriptions for I<sup>2</sup>C interface.

05/05/2011(Gene Apperson)  
Formatted for public release

12/06/2010(Gene Apperson)  
Corrected pin number errors in descriptions of UART interfaces  
Minor rewording of several sections to improve clarity.

09/02/2010(Gene Apperson)  
Revised Electrical Specification section to add discussion of drive strength, ESD protection diodes  
and series current limiting resistors.

Revised Physical Connection Standard section to add note about pin numbering conventions on 2x6  
connectors.

Added Pmod Interface Type 2A (expanded SPI) definition  
Deprecated Pmod Interface Type 3 (UART)  
Added Pmod Interface Type 4 (UART) definition  
Added Pmod Interface Type 4A (expanded UART) definition  
Changed H-Bridge Interface number from Type 4 to Type 5  
Changed Dual H-Bridge Interface number from Type 5 to Type 6

05/14/2009(Gene Apperson)  
Created