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July 2014

FDMA1430JP

Integrated P-Channel PowerTrench® MOSFET and BJT

-30 V, -2.9 A, 90 mΩ

Features

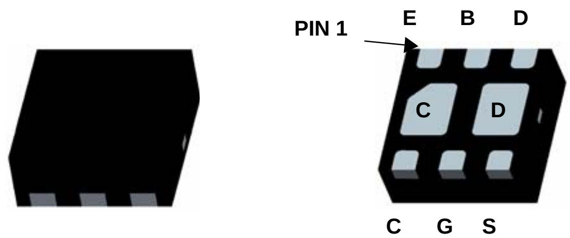
- Max $r_{DS(on)}$ = 90 mΩ at V_{GS} = -4.5 V, I_D = -2.9 A
- Max $r_{DS(on)}$ = 130 mΩ at V_{GS} = -2.5 V, I_D = -2.6 A
- Max $r_{DS(on)}$ = 170 mΩ at V_{GS} = -1.8 V, I_D = -1.7 A
- Max $r_{DS(on)}$ = 240 mΩ at V_{GS} = -1.5 V, I_D = -1 A
- Low profile - 0.8 mm maximum - in the new package MicroFET 2x2
- HBM ESD protection level > 2 kV typical (Note 3)
- RoHS Compliant

General Description

This device is designed specifically as a single package solution for loadswitching in cellular handset and other ultra-portable applications. It features a 50 V NPN BJT and a 30 V P-ch Trench MOSFET in the space saving MicroFET 2x2 package that offers exceptional thermal performance for it's physical size and is well suited to linear mode applications.

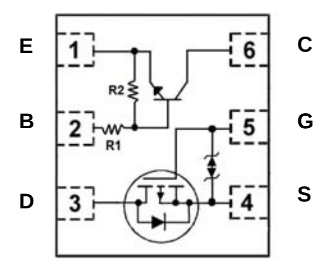
Application

- Loadswitching



Top　　Bottom

MicroFET 2x2



Maximum Ratings T_A = 25 °C unless otherwise noted

Symbol	Parameter	Ratings	Units
V_{DS}	Drain to Source Voltage	-30	V
V_{GS}	Gate to Source Voltage	±8	V
I_D	Drain Current -Continuous T_A = 25°C (Note 1a)	-2.9	A
	-Pulsed	-12	
V_{CBO}	Collector-Base Voltage (Note 4)	50	V
V_{CEO}	Collector-Emitter Voltage (Note 5)	50	V
V_{EBO}	Emitter-Base Voltage	10	V
I_C	Collector Current	100	mA
P_C	Collector Power Dissipation	200	mW
T_J	Junction Temperature	150	°C
P_D	Power Dissipation T_A = 25°C (Note 1a)	1.5	W
	T_A = 25°C (Note 1b)	0.7	
T_J, T_{STG}	Operating and Storage Junction Temperature Range	-55 to +150	°C

Thermal Characteristics

$R_{\theta JA}$	Thermal Resistance, Junction to Ambient(MOSFET) (Note 1a)	86	°C/W
$R_{\theta JA}$	Thermal Resistance, Junction to Ambient(MOSFET) (Note 1b)	173	

Package Marking and Ordering Information

Device Marking	Device	Package	Reel Size	Tape Width	Quantity
143	FDMA1430JP	MicroFET 2x2	7”	8 mm	5000 units

Electrical Characteristics T_J = 25 °C unless otherwise noted

Symbol	Parameter	Test Conditions	Min	Typ	Max	Units

Off Characteristics

Symbol	Parameter	Test Conditions	Min	Typ	Max	Units
BV_{DSS}	Drain to Source Breakdown Voltage	I_D = -250 μA, V_{GS} = 0 V	-30			V
$\frac{\Delta BV_{DSS}}{\Delta T_J}$	Breakdown Voltage Temperature Coefficient	I_D = -250 μA, referenced to 25 °C		-23		mV/°C
I_{DSS}	Zero Gate Voltage Drain Current	V_{DS} = -24 V, V_{GS} = 0 V			-1	μA
I_{GSS}	Gate to Source Leakage Current	V_{GS} = ±8 V, V_{DS} = 0 V			±1	μA

On Characteristics

Symbol	Parameter	Test Conditions	Min	Typ	Max	Units
$V_{GS(th)}$	Gate to Source Threshold Voltage	V_{GS} = V_{DS}, I_D = -250 μA	-0.4	-0.6	-1	V
$\frac{\Delta V_{GS(th)}}{\Delta T_J}$	Gate to Source Threshold Voltage Temperature Coefficient	I_D = -250 μA, referenced to 25 °C		2.4		mV/°C
$r_{DS(on)}$	Static Drain to Source On Resistance	V_{GS} = -4.5 V, I_D = -2.9 A		67	90	mΩ
		V_{GS} = -2.5 V, I_D = -2.6 A		81	130	
		V_{GS} = -1.8 V, I_D = -1.7 A		98	170	
		V_{GS} = -1.5 V, I_D = -1 A		114	240	
		V_{GS} = -4.5 V, I_D = -2.9 A, T_J = 125 °C		102	133	
g_{FS}	Forward Transconductance	V_{DS} = -5 V, I_D = -2.9 A		11		S

Dynamic Characteristics

Symbol	Parameter	Test Conditions	Min	Typ	Max	Units
C_{iss}	Input Capacitance	V_{DS} = -15 V, V_{GS} = 0 V, f = 1 MHz		438	580	pF
C_{oss}	Output Capacitance			47	70	pF
C_{rss}	Reverse Transfer Capacitance			41	60	pF

Switching Characteristics

Symbol	Parameter	Test Conditions	Min	Typ	Max	Units
$t_{d(on)}$	Turn-On Delay Time	V_{DD} = -15 V, I_D = -1 A, V_{GS} = -4.5 V, R_{GEN} = 6 Ω		4.8	10	ns
t_r	Rise Time			4.4	10	ns
$t_{d(off)}$	Turn-Off Delay Time			67	107	ns
t_f	Fall Time			21	33	ns
Q_g	Total Gate Charge	V_{DD} = -15 V, I_D = -2.9 A, V_{GS} = -4.5 V		7.2	10	nC
Q_{gs}	Gate to Source Charge			0.7		nC
Q_{gd}	Gate to Drain "Miller" Charge			1.6		nC

Drain-Source Diode Characteristics

Symbol	Parameter	Test Conditions	Min	Typ	Max	Units
V_{SD}	Source to Drain Diode Forward Voltage	V_{GS} = 0 V, I_S = -1.1 A (Note 2)		-0.7	-1.2	V
t_{rr}	Reverse Recovery Time	I_F = -2.9 A, di/dt = 100 A/μs		16	29	ns
Q_{rr}	Reverse Recovery Charge			5	10	nC

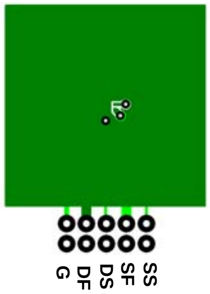
BJT Characteristics

Symbol	Parameter	Test Conditions	Min	Typ	Max	Units
I_{CBO}	Collector Cut-off Current	V_{CB} = 40 V, I_E = 0 A			0.1	μA
h_{FE}	DC Current Gain	V_{CE} = 5 V, I_C = 5 mA	68			
$V_{CE}(sat)$	Collector-Emitter Saturation Voltage	I_C = 10 mA, I_B = 0.5 mA			0.3	V
f_T	Current Gain Bandwidth Product	V_{CE} = 10 V, I_C = 5 mA		250		MHz
C_{ob}	Output Capacitance	V_{CB} = 10 V, I_E = 0 A, f = 1 MHz		3.7		pF
$V_I(off)$	Input Off Voltage	V_{CE} = 5 V, I_C = 100 μA	0.5			V
$V_I(on)$	Input On Voltage	V_{CE} = 0.2 V, I_C = 5 mA			1.3	V
R1	Input Resistor			4.7		kΩ
R1/R2	Resistor Ratio			0.1		

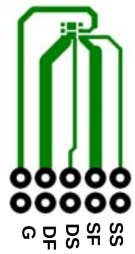
Electrical Characteristics

Notes:

1. $R_{\theta JA}$ is determined with the device mounted on a 1 in^2 oz. copper pad on a 1.5 x 1.5 in. board of FR-4 material. $R_{\theta JC}$ is guaranteed by design while $R_{\theta JA}$ is determined by the user's board design.



a. 86 °C/W when mounted on a 1 in^2 pad of 2 oz copper



b. 173 °C/W when mounted on a minimum pad of 2 oz copper

2. Pulse Test : Pulse Width < 300 us, Duty Cycle < 2.0%
3. The diode connected between the gate and source serves only as protection against ESD. No gate overvoltage rating is implied.
4. Guaranteed by Icbo
5. Guaranteed by Iceo

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Typical Characteristics T_J = 25 °C unless otherwise noted

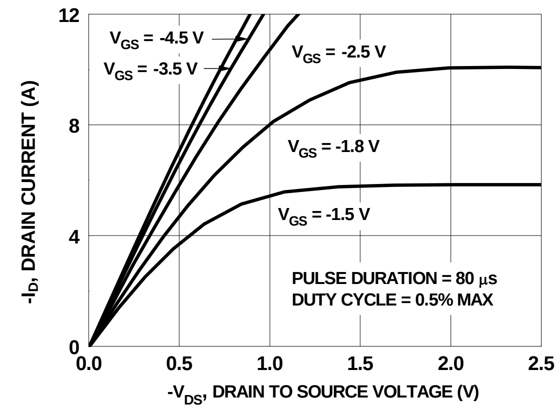


Figure 1. On-Region Characteristics

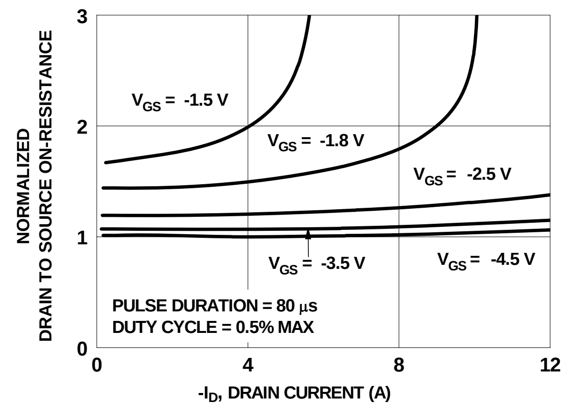


Figure 2. Normalized On-Resistance vs Drain Current and Gate Voltage

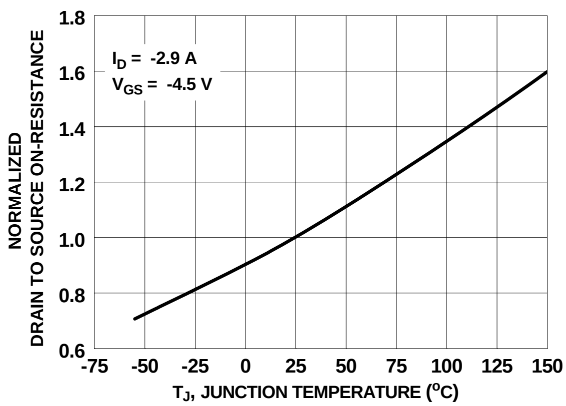


Figure 3. Normalized On-Resistance vs Junction Temperature

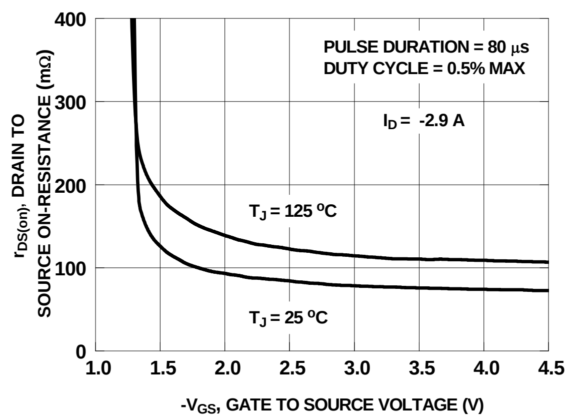


Figure 4. On-Resistance vs Gate to Source Voltage

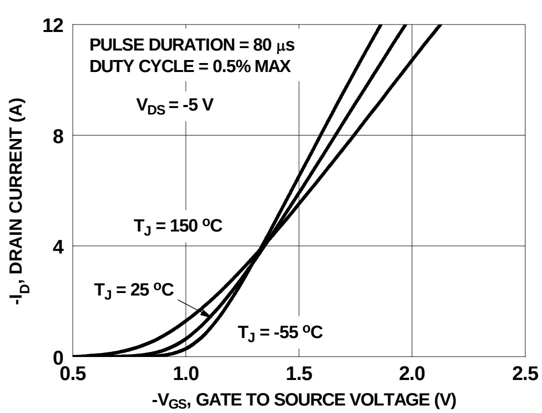


Figure 5. Transfer Characteristics

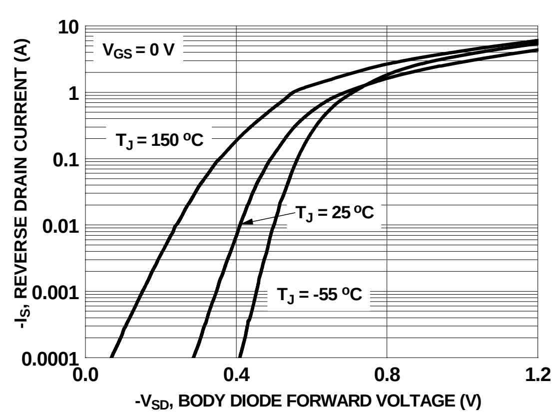


Figure 6. Source to Drain Diode Forward Voltage vs Source Current

Typical Characteristics T_J = 25 °C unless otherwise noted

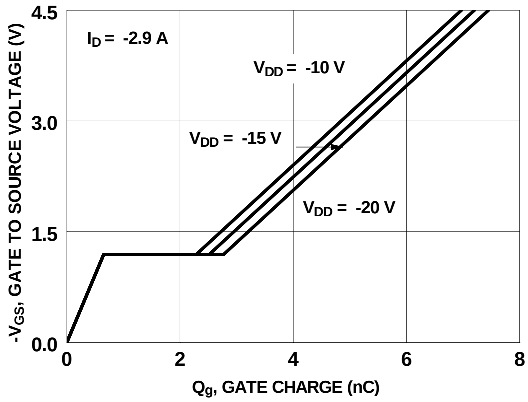


Figure 7. Gate Charge Characteristics

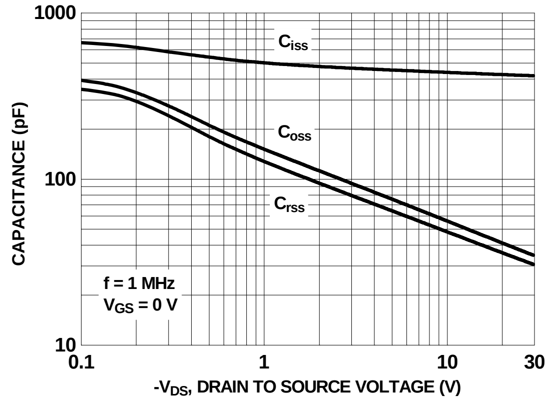


Figure 8. Capacitance vs Drain to Source Voltage

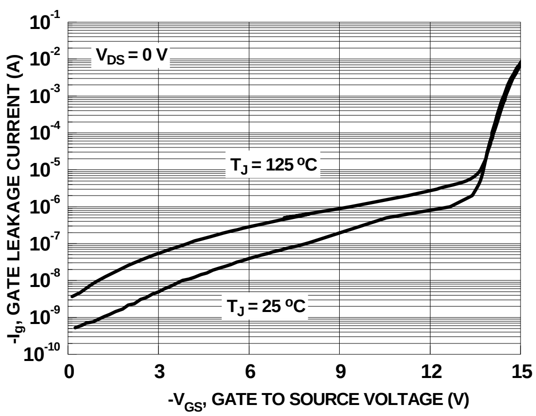


Figure 9. Gate Leakage vs Gate to Source Voltage

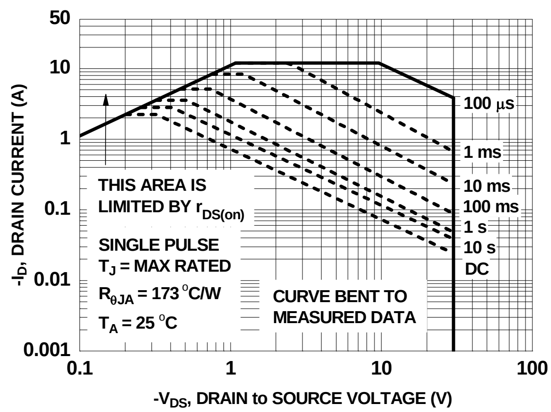


Figure 10. Forward Bias Safe Operating Area

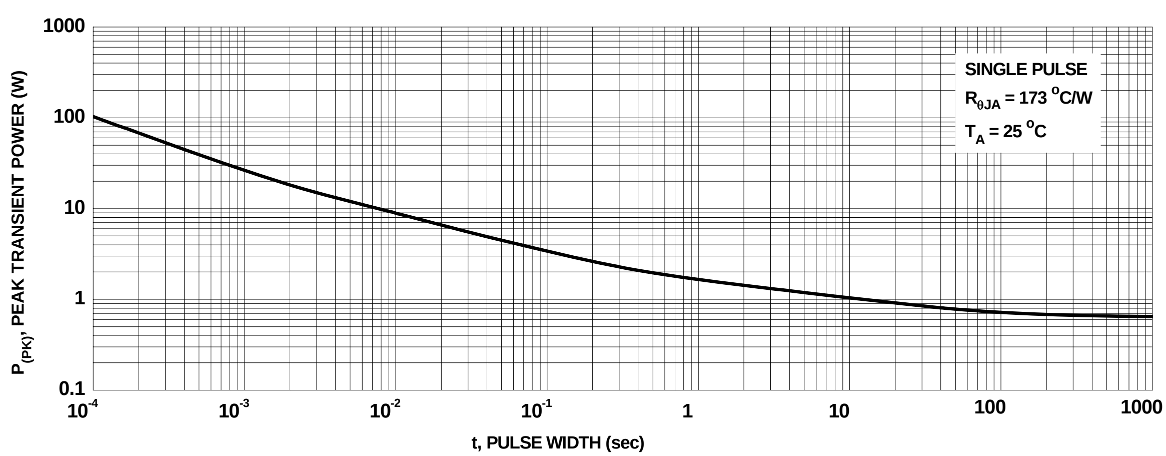


Figure 11. Single Pulse Maximum Power Dissipation

Typical Characteristics T_J = 25 °C unless otherwise noted

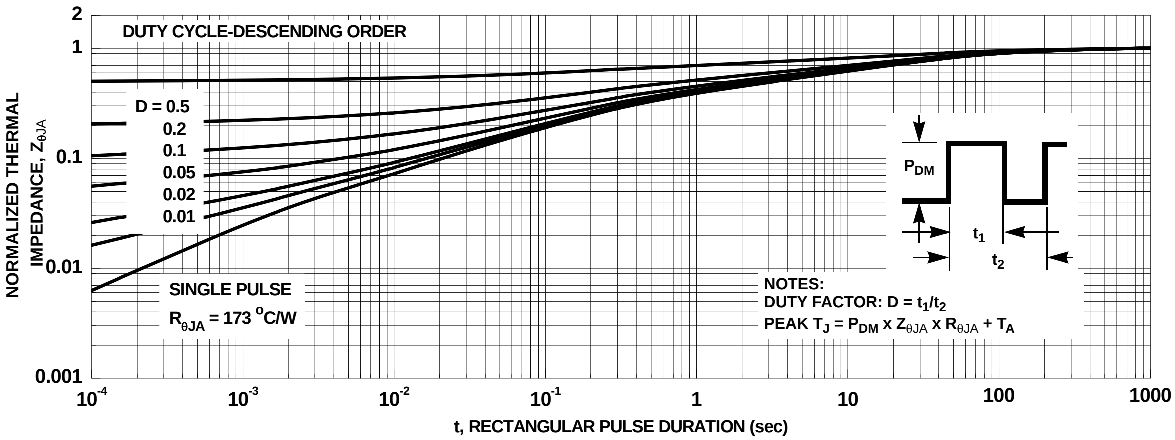
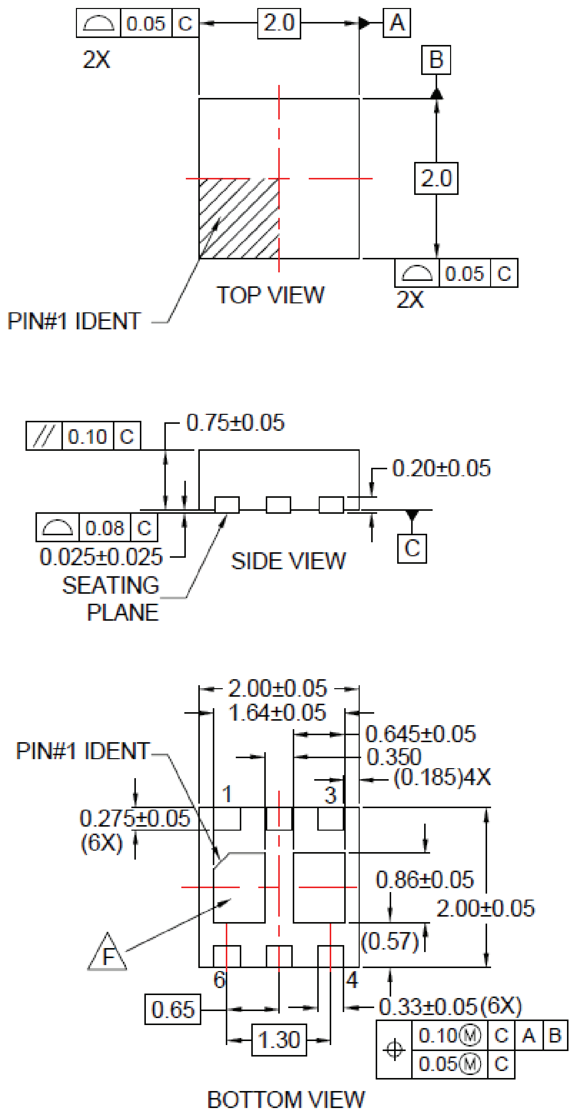
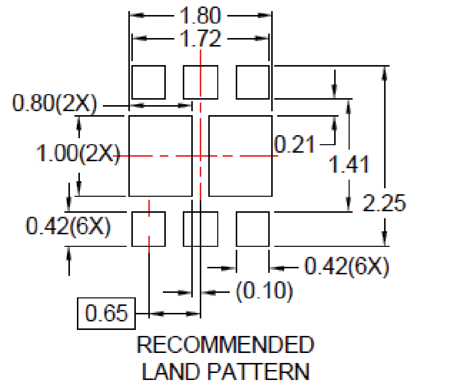


Figure 12. Junction-to-Ambient Transient Thermal Response Curve

Dimensional Outline and Pad Layout





NOTES:

A. CONFORM TO JADEC REGISTRATIONS MO-229, VARIATION VCCC, EXCEPT WHERE NOTED.

B. DIMENSIONS ARE IN MILLIMETERS.

C. DIMENSIONS AND TOLERANCES PER ASME Y14.5M, 2009.

D. LAND PATTERN RECOMMENDATION IS EXISTING INDUSTRY LAND PATTERN.

E. DRAWING FILENAME: MKT-UMLP16Erev4

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Preliminary	First Production	Datasheet contains preliminary data; supplementary data will be published at a later date. Fairchild Semiconductor reserves the right to make changes at any time without notice to improve design.
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Rev. I68

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