MicroRAM™

µRAMxxxx

Actual Size:
2.28 x 1.45 x 0.5in
[57,9 x 36,8 x 12,7mm]

Output Ripple Attenuation Module

Features & Benefits

- RoHS Compliant (with F or G pin option)
- >40dB ripple attenuation from 1.1kHz to 1MHz
- >40dB ripple attenuation from 100Hz to 1.1kHz with additional component
- Integrated OR'ing diode supports N+1 redundancy
- Significantly improves load transient response
- Efficiency up to 98%
- User selectable performance optimization
- Combined active and passive filtering
- 3 – 30V_{DC} input range
- 20 and 30 Ampere ratings

Product Highlights

The Vicor MicroRAM output ripple attenuation module combines both active and passive filtering to achieve greater than 40dB of noise attenuation from 1.1kHz to 1MHz. The lower frequency limit can be extended down to 100Hz, with greater than 40dB of attenuation, with the addition of a single external capacitor. The MicroRAM operates over a range of 3 – 30V_{DC}, is available in either 20 or 30A models and is compatible with most manufacturers switching converters including all Vicor DC-DC converter models.

The MicroRAM's closed-loop architecture greatly improves load transient response and can insure precise point-of-load voltage regulation using its SC function.

The MicroRAM supports redundant and parallel operation with its integrated OR'ing diode function. It is available in Vicor standard Micro package (quarter brick) with a variety of terminations for through-hole, socket or surface-mount applications.

Absolute Maximum Ratings

Parameter	Rating	Unit	Notes
+IN to –IN	30	V_{DC}	Continuous
	40	V_{DC}	100ms
Load current	40	A_{DC}	10 second pulse
V_{REF}	V_{IN} ±1V	V_{DC}	Continuous
Ripple Input (V_{P-P})	100	mV	100Hz – 100kHz
	500	mV	100kHz – 2MHz
Mounting torque	4 – 6 [0.45 – 0.68]	In·lbs [N·m]	6 each, 4-40 screw
Pin soldering temperature	500 [260]	°F [°C]	<5sec; wave solder
	750 [390]	°F [°C]	<7sec; wave solder

Thermal Resistance

Parameter	Typ	Unit
Baseplate to sink		
flat, greased surface	0.16	°C/Watt
with thermal pad (P/N 20265)	0.14	°C/Watt
Baseplate to ambient		
free convection	8.0	°C/Watt
1000LFM	1.9	°C/Watt

Part Numbering

µRAM **2** **C** **2** **1**

Product

Type
2 = 20A
3 = 30A

Product Grade Temperatures (°C)

Grade	Operating	Storage
C =	–20 to +100	–40 to +125
T =	–40 to +100	–40 to +125
H =	–40 to +100	–55 to +125
M =	–55 to +100	–65 to +125

Pin Style
1 = Short Pin
2 = Long Pin
S = Short ModuMate [a]
N = Long ModuMate [a]
F = Short RoHS
G = Long RoHS
K = Extra-Long RoHS [b]

Baseplate
1 = Slotted
2 = Threaded
3 = Thru-hole

[a] Compatible with the ModuMate interconnect system for socketing and surface mounting
[b] Not intended for socket or Surfmate mounting

Note: Product images may not highlight current product markings.

Electrical Characteristics

Electrical characteristics apply over the full operating range of input voltage, output power and baseplate temperature, unless otherwise specified.
All temperatures refer to the operating temperature at the center of the baseplate.

µRAM Module Specifications

(–20 to +100°C baseplate temperature)

Parameter	Min	Typ	Max	Unit	Notes
Operating current range µRAM2xxx	0.02		20	A	No internal current limiting. Converter input must be properly fused such that the µRAM output current does not exceed the maximum operating current rating by more than 30% under a steady state condition.
Operating current range µRAM3xxx	0.02		30	A	
Operating input voltage	3.0		30	V	Continuous
Transient output response Load current step < 1A/µsec			50	mV_{P-P}	Step load change; see Figures 20, 23, & 26, pp. 16 – 17
Transient output response Load current step < 1A/µsec (C_{TRAN} = 820µF)			50	mV_{P-P}	Optional capacitance C_{TRAN} can be used to increase transient current capability; See Figures 21, 24 & 27, pp. 16 – 17
Recommended headroom voltage range (V_{HR}) @ 1A load [c]	325		425	mV	See Figures 4 and 5, p. 5 for detailed explanation. See Table 1 for typical headroom setting resistor values.
Output ripple			10	mV_{P-P}	Ripple frequency of 60Hz to 100kHz; optional CHR capacitor of 100µF required to increase low frequency attenuation as shown in Figure 2, p. 3
Input V_{P-P} = 100mV			5	MV_{RMS}	
Output ripple			10	mV_{P-P}	Ripple frequency of 100kHz to 2MHz; as shown in Figure 2, p. 3
Input V_{P-P} = 500mV			5	MV_{RMS}	
SC output voltage [d]	1.23			V_{DC}	See table 1 for typical R_{SC} values, note 2 for calculation.
OR'ing threshold		–10		mV	$V_{IN} – V_{OUT}$
µRAM bias current			60	mA	
Power dissipation µRAM2xxx V_{HR} = 380mV @ 1A		7.5		W	V_{IN} = 28V; I_{OUT} = 20A
Power dissipation µµRAM3xxx V_{HR} = 380mV @ 1A		11.5		W	V_{IN} = 28V; I_{OUT} = 30A

[c] The headroom voltage V_{HR} is the voltage difference between the V_{IN+} and the V_{OUT+} pins of the µRAM.

$$R_{HR} = \frac{V_{OUT+}}{V_{HR}} \bullet 2.3k \qquad \textit{(See Table 1 for example } R_{HR} \textit{ values)}$$

[d] The SC resistor is used to trim the converter's output voltage (Vnom) to compensate for the headroom voltage drop of the µRAM when remote sense is not used. This feature can only be used with converter's that have a trim reference range between 1.21 and 1.25V.

$$R_{SC} = \frac{(V_{NOM} \bullet 1k)}{1.23V} - 2k \qquad \textit{(See Table 1 for example } R_{SC} \textit{ values)}$$

µRAM Output Voltage	V_{HR} @ 1A	R_{HR} Value (Ω)	R_{SC} Value (Ω)
3V	375mV	18.2k	442
5V	375mV	30.9k	2.05k
12V	375mV	73.2k	7.68k
15V	375mV	90.9k	10.20k
24V	375mV	147.0k	17.40k
28V	375mV	174.0k	21.00k

Table 1 — *Calculated values of R_{SC} and R_{HR} for a headroom voltage of 375mV.*
Use notes 1 and 2 to compute R_{SC} and R_{HR} values for different headroom voltages.

MicroRAM Theory of Operation

PARD Attenuation

The Vicor MicroRAM uses both active and passive filtering to attenuate PARD (Periodic and Random Deviations), typically associated with a DC to DC converter's output voltage. The passive filter provides effective attenuation in the 50kHz to 20MHz range. The low frequency range of the passive filter (i.e., resonant frequency) can be lowered by adding capacitance to the CTRAN pin to ground and will improve the transient load capability, as is shown in Figure 7. The active filter provides attenuation from lower frequencies up to 2MHz. The lower frequency range of the active filter can be extended down by adding an external bypass cap across the R_{HR} resistor.

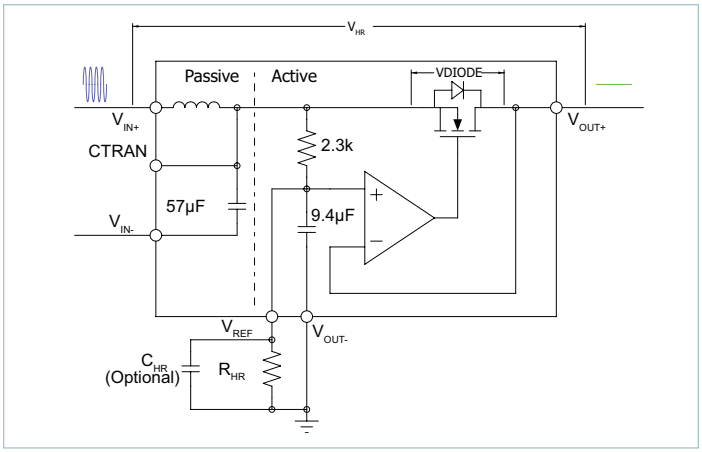


Figure 1 — *Simplified MicroRAM block diagram*

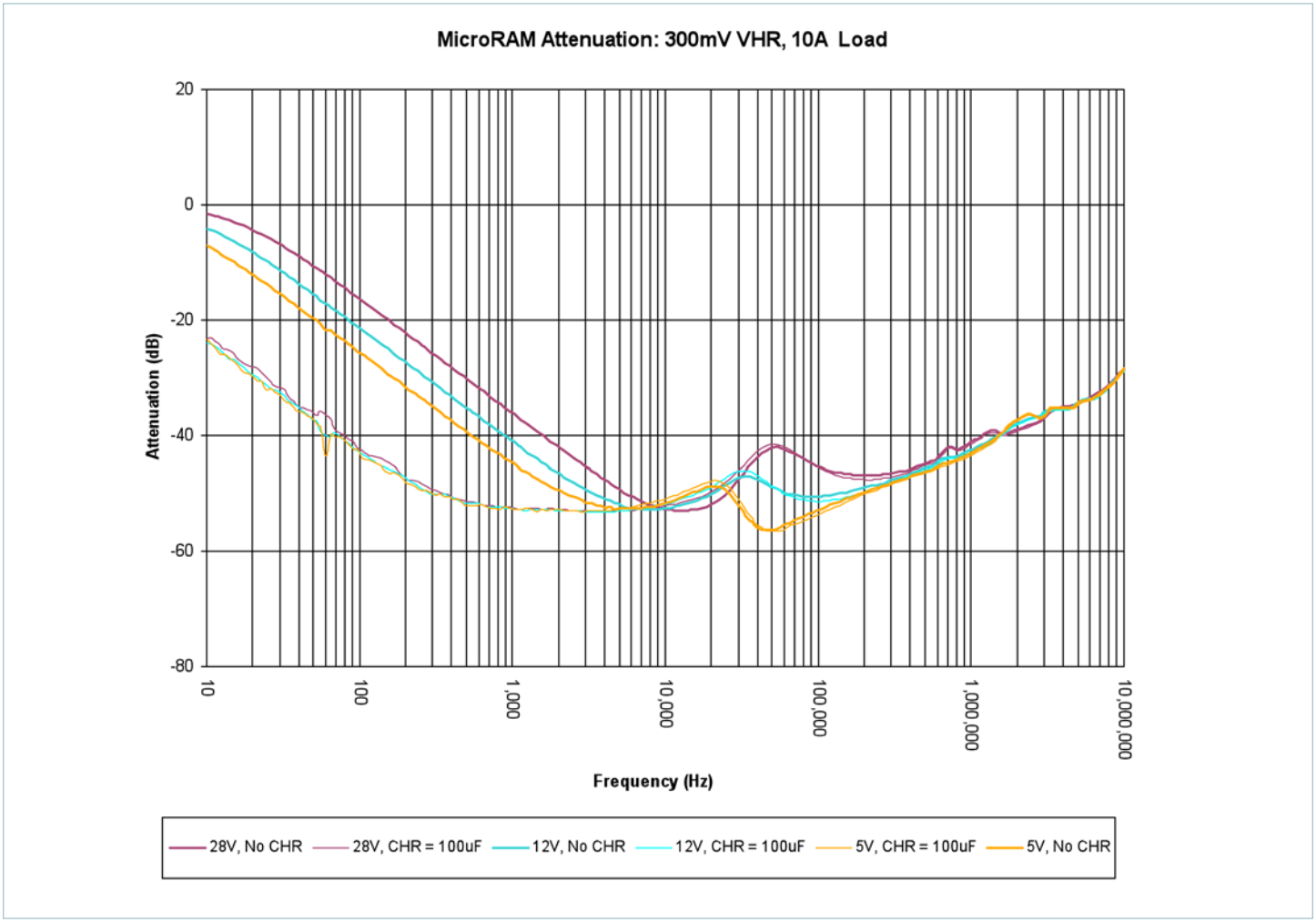


Figure 2 — *MicroRAM attenuation with and without an additional C_{HR} capacitor*

The plots in Figure 2 show the increase in attenuation range that can be realized by adding an additional capacitor, CHR, across the RHR resistor, as shown in Figure 1. These plots represent the total attenuation, due to both the active and passive filtering, before and after adding an additional 100μF of capacitance for C_{HR}. There are practical limitations to the amount of capacitance that can be added, which is explained in more detail under the VREF section.

PARD Attenuation (Cont.)

Active attenuation is achieved by using power MOSFETs as a variable resistor that can dynamically change its impedance in order to maintain a constant output voltage, equal to the voltage programmed on its reference pin. When the input is lower, the active loop reduces the FET's resistance, lowering the overall voltage drop across the MicroRAM. When the input is higher, the resistance is increased, increasing the voltage drop across the MicroRAM. The bandwidth of the active loop must be sufficiently higher than the converter's control loop so it does not introduce significant phase shift to the sense loop of the converter.

There are both upper and lower limits to the range of resistance variations. The lower limit is based on the path resistance between V_{IN+} and V_{OUT+} and the amount of current passing through the MicroRAM. On the high end, the resistance of the FET, and therefore the maximum voltage drop, is limited to the voltage when the body diode of the FET starts to conduct and ripple passes through it to the output, exhibiting positive peaks of ripple at the load.

The waveforms in Figure 3 are representative of a typical ripple signal, riding on a DC voltage. The headroom voltage across the MicroRAM (V_{HR}) is the difference in DC voltage between V_{IN} and V_{OUT}. This headroom is programmed via R_{HR}, shown in Figure 1. The headroom voltage should be selected such that the headroom voltage minus half the peak-to-peak ripple does not cross the minimum headroom limit, or that the headroom voltage plus half the peak-to-peak ripple does not exceed the voltage drop of the FET's intrinsic body diode voltage drop, that is current and temperature dependent. The headroom must be properly set below the point of diode conduction. In either of these two cases if the headroom is depleted or the diode conducts, the ripple at the CTRAN node will be exhibited as peaks of the ripple voltage amplitude at the load, negating the active attenuation.

If the fundamental switching frequency of the converter is above the resonant frequency of the passive LC filter (see Figure 8) the fundamental switching and harmonic frequencies will be reduced at the rate of 40dB per decade in frequency. The active filter will be presented with lower peak-to-peak ripple and will have sufficient dynamic range to attenuate the ripple. If the fundamental is below the resonant frequency of the LC filter, then the active circuit will attenuate the full noise signal.

The plot in Figure 4 illustrates the "effective" headroom voltage over the full operating current range of the MicroRAM. The reduction in headroom voltage, seen across the MicroRAM over the full 30A load current range, is due to two factors; the effects of the slope adjust and the insertion resistance of the MicroRAM. The two green shaded areas represent the minimum and maximum recommended headroom voltages listed in the MicroRAM's specification table. The gray area is the voltage drop due to the MicroRAM's insertion resistance, from the positive input to the positive output, of the MicroRAM, multiplied by the load current. This insertion resistance is typically 5mΩ at 25°C and can increase to 6.5mΩ at 100°C.

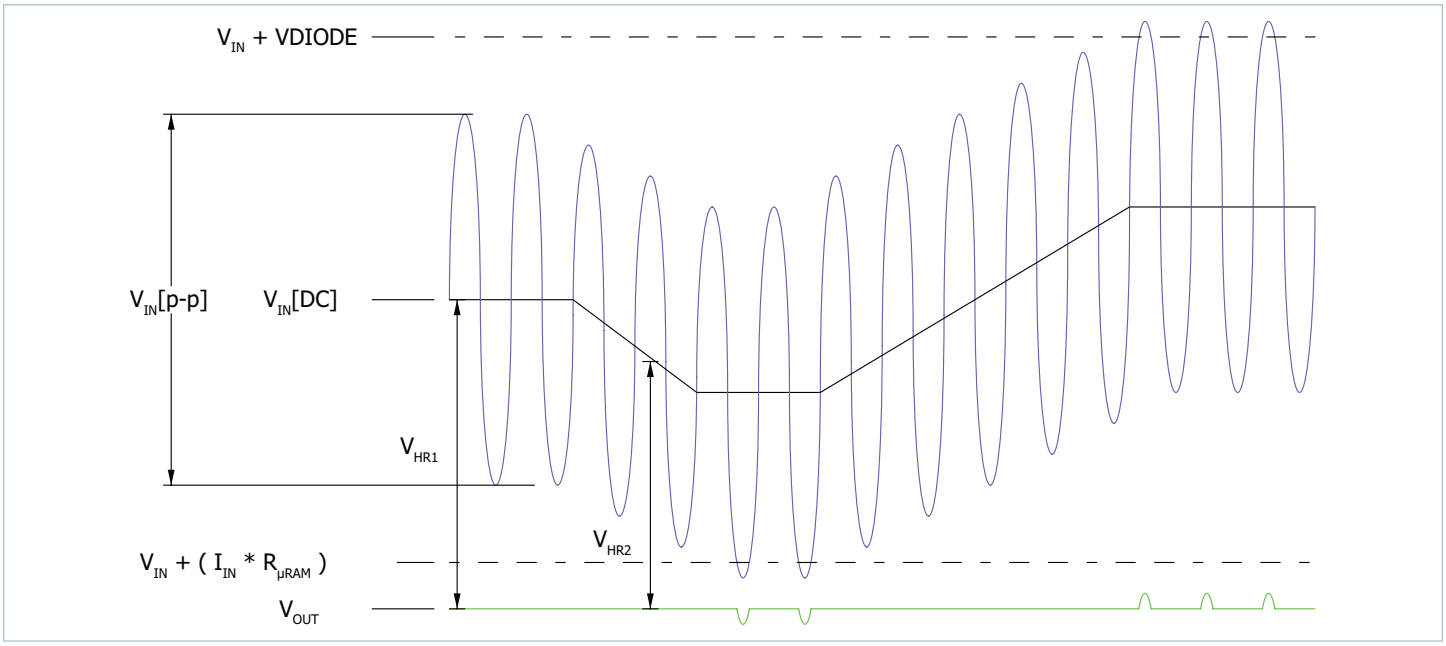


Figure 3 — *Active attenuation and the effects of headroom*

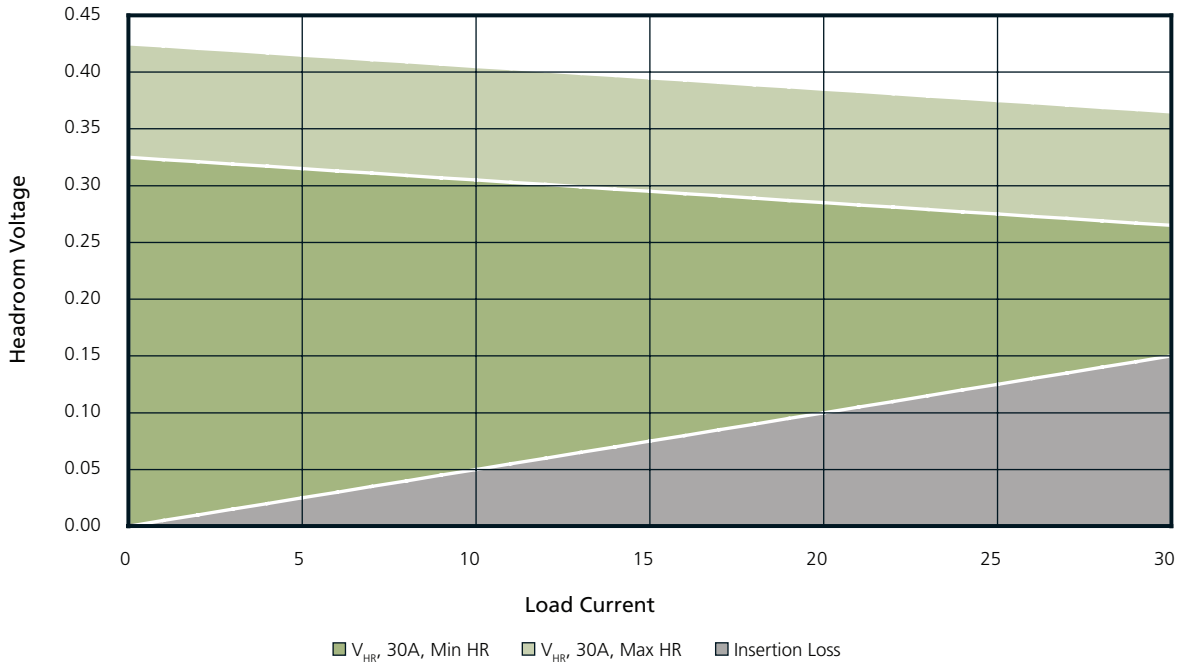


Figure 4 — *MicroRAM headroom voltage reduction over full-load current range.*

As the load current is increased, the internal slope adjust of the MicroRAM will reduce the headroom voltage across the MicroRAM at a rate of about 2mV/A for the 30A version (4mV/A for 20A version) in an effort to reduce the power loss across the MicroRAM.

This headroom reduction, in conjunction with the increased voltage drop across the MicroRAM due to its resistance, reduces the effective headroom voltage and therefore the MicroRAM's ability to attenuate PARD at higher load currents.

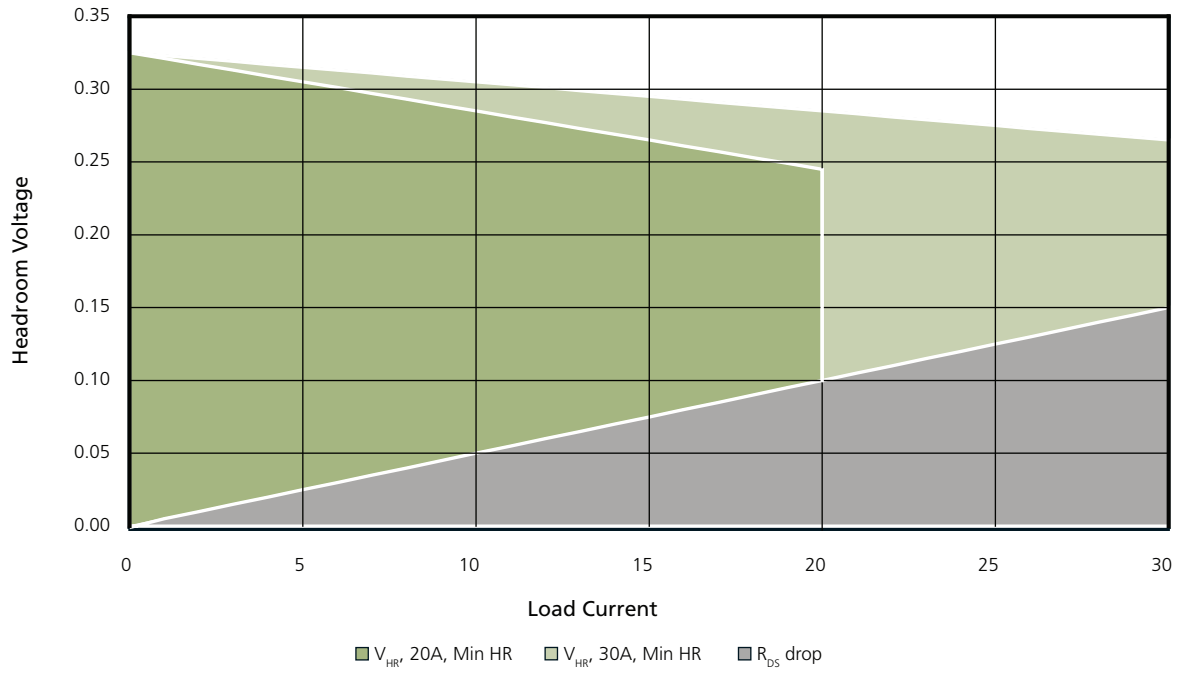


Figure 5 — *Slope adjust comparison of 20A and 30A MicroRAM.*

The plots in Figure 5 show the difference in the slope adjust effect between the two versions of the MicroRAM and that the minimum recommended headroom of 325mV will still leave an effective headroom voltage of about 140mV at 20A, using the 20A MicroRAM. When using the 30A version at 30A, the headroom would be about 120mV, so a higher initial headroom voltage might be required.

The recommended minimum and maximum headroom voltages, stated on page two, are listed as reference points for designers and should not be considered as absolutes when designing with the MicroRAM. At lower operating currents, a lower initial headroom voltage can be used with no detrimental effects on the MicroRAM's ability to attenuate PARD. The designer should have a good idea of the amount of PARD, at the maximum operating current, the MicroRAM is to filter when selecting the MicroRAM's headroom voltage. He could use the slope adjust rate to calculate what the headroom voltage should be at the minimum load to determine his headroom programming resistor value. The attenuation plots, shown in Figure 2, are of a MicroRAM with 300mV of headroom initially programmed, running at 10A load with 115mV$_{P-P}$ of ripple on the input voltage. Lowering the headroom voltage will reduce the MicroRAM's transient performance, so consideration of the filter's performance priorities should be used when determining the best headroom setting.

For example: a designer needs to filter 100mV of ripple at 10A, and is using a 20A MicroRAM. He should have 100mV of headroom plus 50mV for the insertion resistance at 10A, or 150mV of programmed headroom. At minimum load, the programmed headroom voltage would be 150mV plus 40mV (10A multiplied by 4mV/A slope adjust), or 190mV of programmed headroom. This will ensure enough attenuation headroom voltage at the 10A max load and save power making the overall system more efficient.

CTRAN

CTRAN is the passive filtered node that feeds into the active filter portion of the MicroRAM. Adding extra storage capacitors here can improve the overall system response to load transients.

The waveforms in Figures 6 and 7 represent the MicroRAM's response to a step in load current, from 10A to 14A, with and without an additional 470μF capacitor on C_{TRAN}.

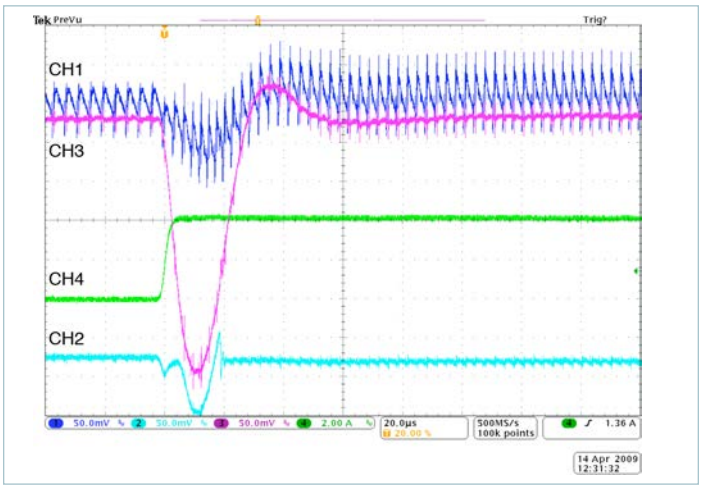


Figure 6 — *Normal transient load response*

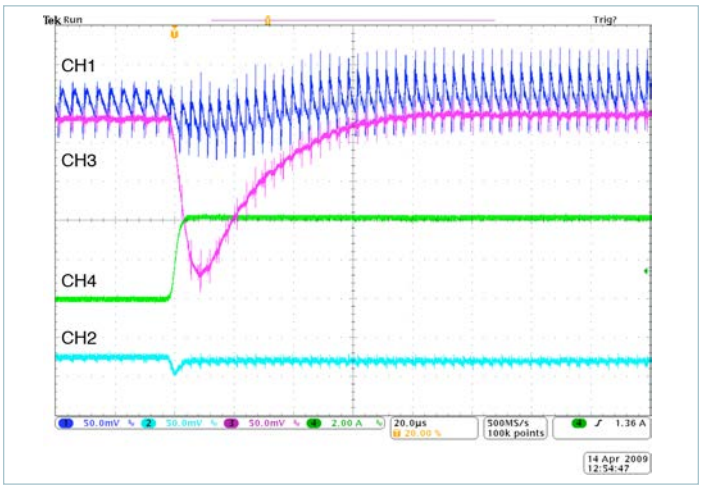


Figure 7 — *Transient response with added CTRAN capacitor*

Note: Channel 1 (blue) is V_{IN+} from the converter, Channel 2 (light blue) is V_{OUT+}, Channel 3 (pink) is CTRAN and Channel 4 (green) is the output step load current. Channels 1 through 3 are DC measured with a 5V offset and referenced to the same point on the y (voltage) axis. Channel 4 has no offset and is the step load added to the continuous 10A static load, which is not shown.

Passive Attenuation

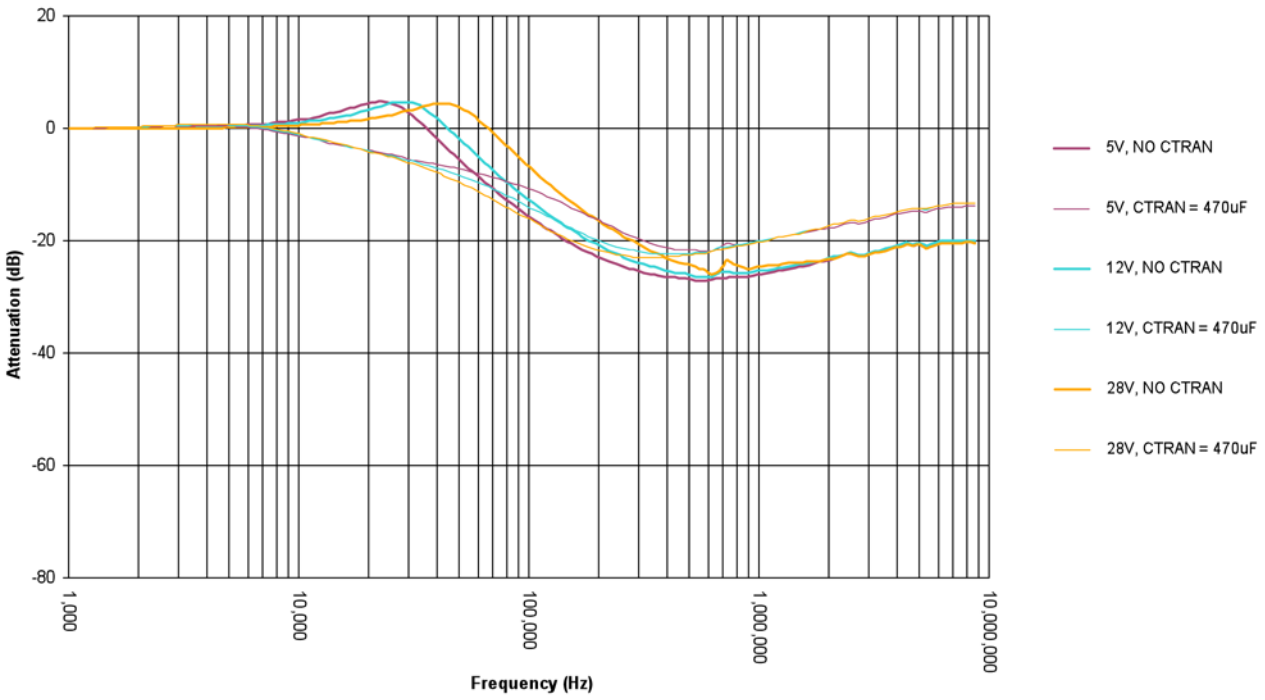


Figure 8 — *MicroRAM's passive filter attenuation with V_{HR} = 300mV, I_{OUT} = 10A*

The affects of input voltage on the internal ceramic capacitors in the LC circuit shifts the resonant bump higher in frequency as capacitance goes down with increased DC potential. The attenuation shape changes with the addition of electrolytic capacitance (with relatively low ESR compared with ceramic) at CTRAN lowering the resonant frequency and quality factor (Q) of the tank.

VREF/Slope Adjust

VREF is the headroom programming pin for the MicroRAM. The voltage on this pin will be the voltage seen on the MicroRAM's output. This pin is used to program the voltage drop across the MicroRAM. Its value is calculated using the following equation:

$$R_{HR} = \frac{2.3k \bullet V_{OUT}}{V_{HR}}$$

Where:

R_{HR} = MicroRAM headroom programming resistor,

V_{OUT} = voltage seen on the MicroRAM's output pins,

V_{HR} = desired headroom voltage across the MicroRAM.

"Slope Adjust" is the MicroRAM's built-in headroom adjust feature that takes advantage of Vicor 2nd Generation converter product characteristic of presenting lower ripple amplitude and higher fundamental switching frequencies with increased load current.

The MicroRAM slope adjust feature improves the filter's efficiency by sensing the load current and is designed to maintain a constant power drop across the MicroRAM as the load current varies. As the load current increases, the slope adjust circuit reduces the headroom linearly based on the slope of the changing load current. The typical passive filter within the MicroRAM will increase losses with increased current. The Slope Adjust feature will decrease the headroom voltage by about 50mV from minimum load to max load, for either the 20A or 30A version of the filter.

There is a limit to how much additional capacitance can be added to the VREF pin. Depending on the low frequency ripple component of the converter's output (especially off-line converters), a low frequency (5 – 20Hz) oscillation may occur at the MicroRAM output due to excessive lag of the MicroRAM's output vs. the converter's, when additional VREF capacitance is greater than 50μF.

SC

The SC pin of the MicroRAM provides a means of headroom voltage drop compensation for the converter, when remote sensing is not possible, as with Vicor 2nd Generation Micro converter product line. The equivalent circuit is shown in Figure 9 and consists of a current source, whose nominal source current can be calculated as the MicroRAM's headroom voltage, divided by 1,000Ω. Internally, this current source is fed into a reference circuit consisting of a 1.23V reference with a 1kΩ series resistor. Since the MicroRAM's SC circuit generates a fixed current, part of that current gets shunted away by the internal reference circuit, the rest flows into the converter's SC pin. The value of R_{SC} determines how much of the MicroRAM's SC current goes to the converter's SC circuit.

$$R_{SC} = \frac{1k \bullet V_{NOM}}{1.23V} - 2k$$

Where:

V_{NOM} = nominal converter output voltage

The internal reference circuit of the MicroRAM is designed to match the 1.23V reference circuit of Vicor "Brick" converters, which limits the voltage range that the SC pin can span. This function will not work with Vicor 1st Gen converters due to its 2.5V internal reference voltage.

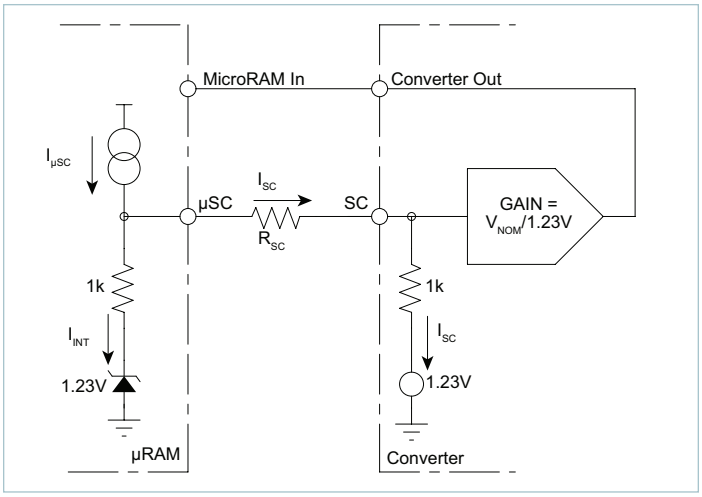


Figure 9 — *MicroRAM's SC control circuit*

ORing

The attenuation MOSFETs used in the MicroRAM are orientated such that they form an OR'ing circuit between the converter's output and the load. Less than 50mA will flow from the output to the input terminal of the MicroRAM over the full output voltage range while the input is shorted.

Typical Circuit Applications

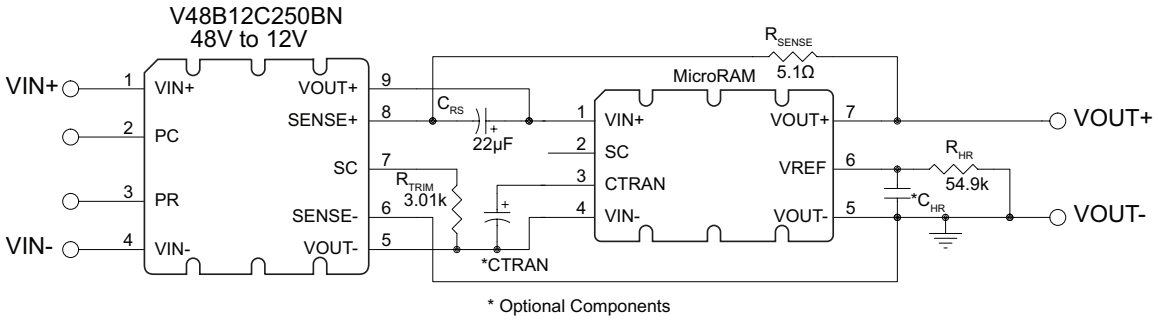


Figure 10 — *Typical configuration using remote-sense control and a 12V converter trimmed down to 9V; R_{HR} set for 375mV of headroom voltage*

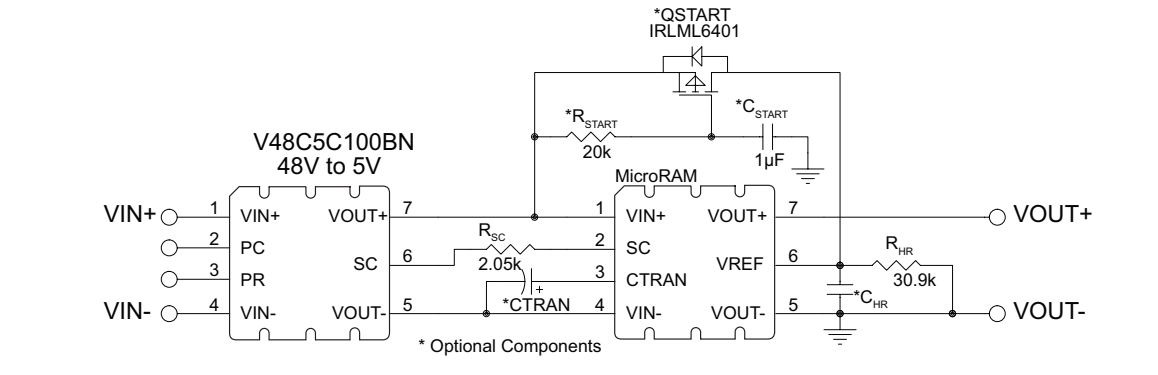


Figure 11 — *Typical SC control configuration and an optional start-up circuit; R_{HR} set for 375mV of headroom voltage*

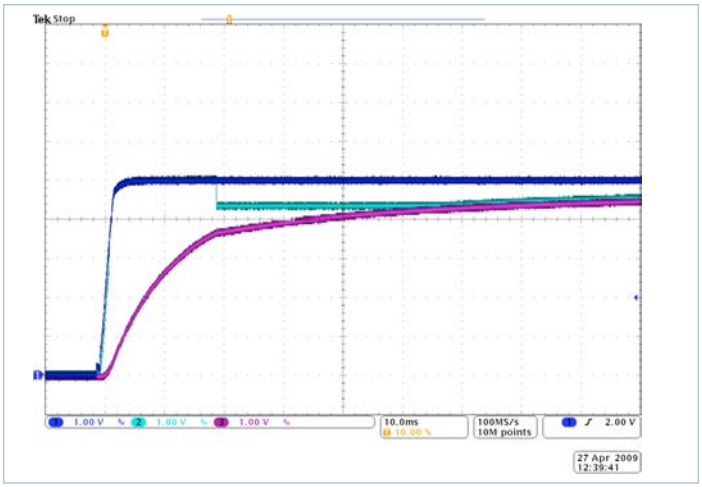


Figure 12 — *Normal start-up waveforms*

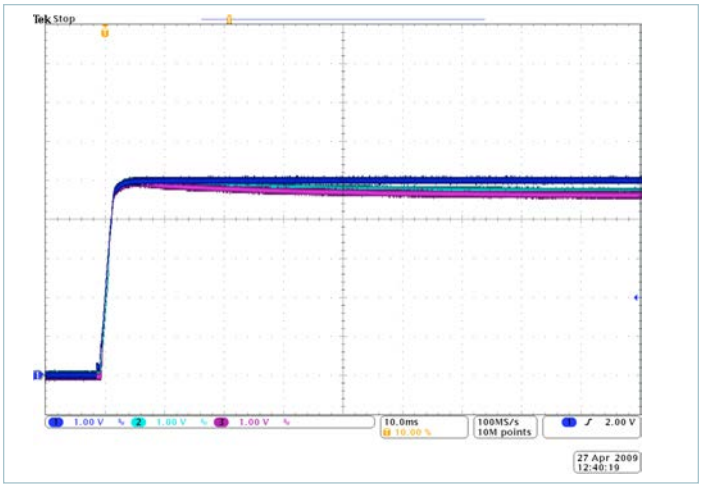


Figure 13 — *Start-up waveforms with the optional start-up circuitry*

In Figure 10, a 48V to 12V Vicor Mini converter is used to create a 9V output supply. The converter is trimmed down from 12V to 9V, using a 3.01kΩ resistor from the converter's SC to its VOUT– pins, then uses the remote-sense pins, along with the RRS and CRS components, to maintain proper output voltage and converter stability. Again, the headroom voltage is designed to be 375mV.

The circuit shown in Figure 11 is of a Vicor Micro 48V to $5V_{DC}$ to DC converter with a MicroRAM, set to have 375mV of headroom voltage drop across it. To compensate for the headroom drop, the MicroRAM's SC circuit is used to adjust the converter to have 5.375V on its output, so the voltage seen on the MicroRAM's output is 5V.

Figure 11 also shows an optional start-up circuit that might be required in some designs which are sensitive to any voltage "glitches" during the initial start-up of the MicroRAM. The waveforms in Figures 12 and 13 show a comparison of typical start-up waveforms, with and without the optional start-up circuit. In Figure 12, the voltage on the MicroRAM's V_{IN+} (Ch1, blue) and V_{OUT+} (Ch2, light blue) pin are equal at start up. This is due to the VREF voltage (Ch3, pink) being much lower than V_{IN+}. The time required to charge the internal VREF cap, and any external C_{HR} caps that where added, through the 2.3kΩ internal resistor (Figure 1) is the cause of the delay. This voltage difference forces the active circuit to drive the attenuation MOSFET's to their minimum r_{DSON} value, essentially shorting the input and output together. Once the VREF voltage is within a diode voltage drop of the MicroRAM's output voltage, the internal active circuit will turn-off the MOSFET's and the difference between the input and output is the MOSFET's body diode voltage drop. As the voltage on VREF continues to increase in value, the output voltage starts to follow the VREF voltage until it reaches the programmed headroom offset voltage.

The waveforms in Figure 13 demonstrate the optional start-up circuit's ability to eliminate the start-up glitch by shorting the VREF pin (Ch3, violet) to V_{IN+} (Ch1, blue) for a short period of time, determined by the RC components connected to the gate of the PFET. The circuit releases the VREF pin to discharge down to its programmed value and creates the headroom voltage needed for attenuation. V_{OUT+} (Ch3, light blue) can be seen following the VREF voltage.

Note: In any design using the MicroRAM, a minimum output load of 20mA is required for proper operation. Without this load, the internal circuitry of the MicroRAM can force the output rail to be as much as 8V greater than the input rail.

Converter Trimming Using a MicroRAM: Remote Sense

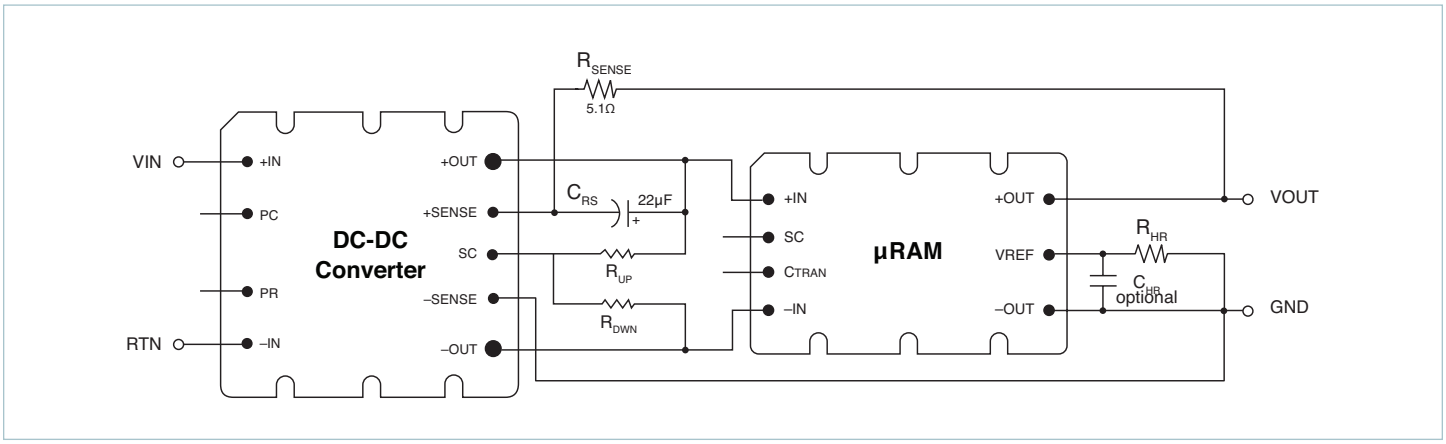


Figure 14 — *Configuration for trimming a converter's output up/down using remote sensing*

When trimming up a converter in a remote-sense configuration, the designer must be aware that the voltage the trim-up resistor is connected to, the output of the converter, is not just the desired trim-up voltage but also the headroom voltage of the filter. The voltage programmed on the converter's SC pin is based on just the trimmed up voltage alone.

Vicor recommends that the value of R_{SENSE} resistor in Figure 14 should be 5.1Ω for proper operation. For converters other than Vicor, this value can be increased up to 10 x (51Ω) to help with system stability.

When trimming down a converter in remote sense, there are no other voltage drops to take into consideration so the equation is much simpler.

Trim-up Equation:

$$R_{UP} = \frac{1k\Omega\left(V_{NOM} \bullet (V_{OUT} + V_{HR}) - (V_{OUT} \bullet 1.23V)\right)}{1.23V\,(V_{OUT} - V_{NOM})}$$

Where:

R_{UP} = trim-up resistor

V_{NOM} = nominal converter output voltage

V_{OUT} = desired output voltage, seen on MicroRAM's output

V_{HR} = headroom voltage drop across the MicroRAM

1.23V = converter's internal reference voltage

1kΩ = converter's internal series resistor

Trim-Down Equation:

$$R_{DWN} = \frac{1k\Omega \bullet V_{OUT}}{V_{NOM} - V_{OUT}}$$

Where:

R_{DWN} = trim-down resistor

V_{NOM} = nominal converter output voltage

V_{OUT} = desired output voltage, seen on MicroRAM's output

1kΩ = converter's internal series resistor

Converter Trimming Using a MicroRAM: SC Controlled Trimming

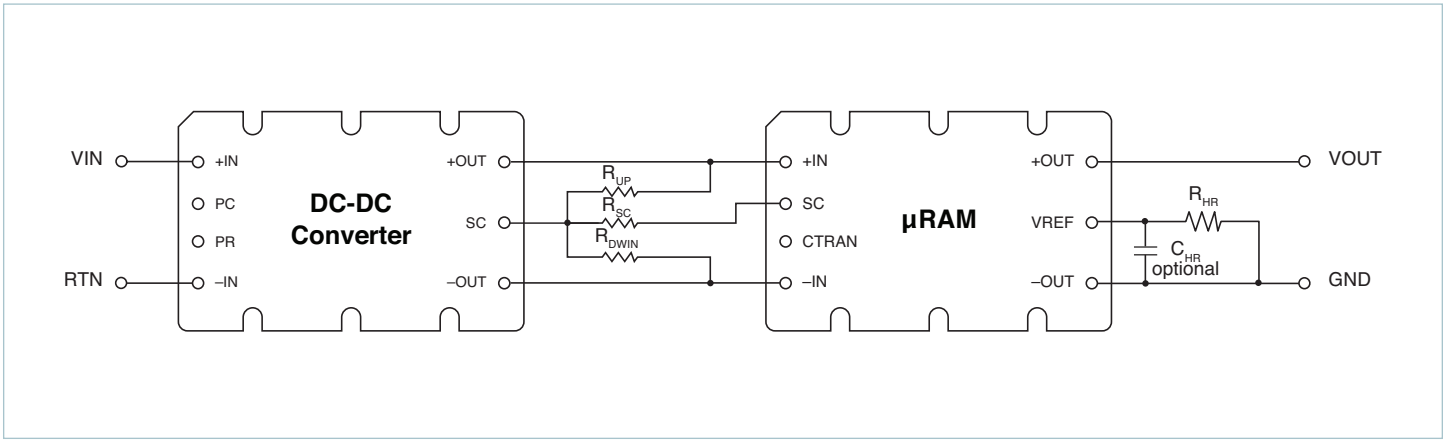


Figure 15 — *Configuration for trimming a converter's output up/down using SC*

When trimming up a converter using SC control, the designer would calculate the trim-up resistor based on the designed trimmed up voltage without regard for the headroom voltage drop. The SC circuit will adapt the converter's output for the additional headroom voltage drop of the filter.

Converter's Trim-Up Resistor Equation:

$$R_{UP} = \frac{1k\Omega \bullet V_{OUT} \bullet (V_{NOM} - 1.23V)}{1.23V \bullet (V_{OUT} - V_{NOM})}$$

Where:

R_{UP} = trim-up resistor

V_{NOM} = nominal converter output voltage

V_{OUT} = desired output voltage, seen on MicroRAM's output

1.23V = converter's internal reference voltage

1kΩ = converter's internal series resistor

Converter's Trim-Down Resistor Equation:

$$R_{DWN} = \frac{1k\Omega \bullet V_{OUT}}{(V_{NOM} - V_{OUT})}$$

Where:

R_{DWN} = trim-up resistor

V_{NOM} = nominal converter output voltage

V_{OUT} = desired output voltage, seen on MicroRAM's output

1kΩ = converter's internal series resistor

μRAM's SC Resistor Calculation With a Trim-Up Resistor

The equation to calculate the R_{SC} resistor is as follows:

$$R_{SC} = \frac{V_{\mu SC} - V_{SC}}{I_{SC}}$$

Where:

R_{SC} = resistor that programs the trim up current from the MicroRAM

$V_{\mu SC}$ = the voltage seen on the MicroRAM's SC pin

V_{SC} = the voltage seen on the converter's SC pin

I_{SC} = the trim current generated by the MicroRAM

To calculate R_{SC}, the three missing terms must be calculated. To find the value of V_{SC} use the following:

$$V_{SC} = \frac{(V_{OUT} + V_{HR}) \bullet 1.23V}{V_{NOM}}$$

Where:

V_{HR} = programmed voltage drop (headroom) across the MicroRAM

V_{SC} is the trimmed up voltage measured on the converter's SC pin to produce the trimmed up V_{OUT} with the V_{HR} (filter headroom voltage) added. The current required to elevate the SC voltage can be calculated using the following equation:

$$I = \frac{(V_{SC} - 1.23V)}{1k\Omega}$$

The current I is the total current needed by the SC pin to create the desired trimmed up voltage. This current is made up of the current from the R_{UP} resistor and the current from the MicroRAM. With the value of the trim-up resistor is known, the current provided by R_{UP} can be calculated as follows:

$$I_{UP} = \frac{(V_{OUT} + V_{HR} - V_{SC})}{R_{UP}}$$

The current required from the MicroRAM is the difference between the total current (I) and the current provided by the R_{UP} resistor (I_{UP}).

$$I_{SC} = I - I_{UP}$$

The last term to find is the voltage measured on the MicroRAM's SC pin ($V_{\mu SC}$), which can be calculated using the following equation:

$$V_{\mu SC} = 1.23V + V_{HR} - I_{SC} \bullet 1k\Omega$$

R_{SC}'s value is the found by taking the difference in the voltage between the MicroRAM's SC pin and the converter's SC pin, and dividing that by the current required from the MicroRAM to source into the converter's SC pin.

μRAM's SC Resistor Calculation With a Trim-Down Resistor

The equations to calculate the R_{SC} resistor and the V_{SC} voltage are the same when trimming a converter up or down. When trimming a converter down, current is drawn out of the converter's SC pin through the R_{DWN} resistor.

This current can be calculated using the following equation:

$$I = \frac{(1.23 - V_{SC})}{1k\Omega}$$

To determine the amount of current drawn through the trim-down resistor, I_{DWN}, use the following equation:

$$I_{DWN} = \frac{V_{SC}}{R_{DWN}}$$

Since R_{DWN} is calculated without adding the MicroRAM's headroom voltage, its value is lower than if it were trimming down with the headroom added. The current through R_{DWN} is greater than the current that must be drawn from the converter's SC pin, so the MicroRAM must source its current into R_{DWN} to get proper regulation. The current required from the MicroRAM can be calculated as follows:

$$I_{SC} = I_{DWN} - I$$

The same equation is used to calculate the voltage on the MicroRAM's SC pin as when trimming up:

$$V_{\mu SC} = 1.23V + V_{HR} - I_{SC} \bullet 1k\Omega$$

The value of R_{SC} can now be calculated using:

$$R_{SC} = \frac{(V_{\mu SC} - V_{SC})}{I_{SC}}$$

Paralleling Applications

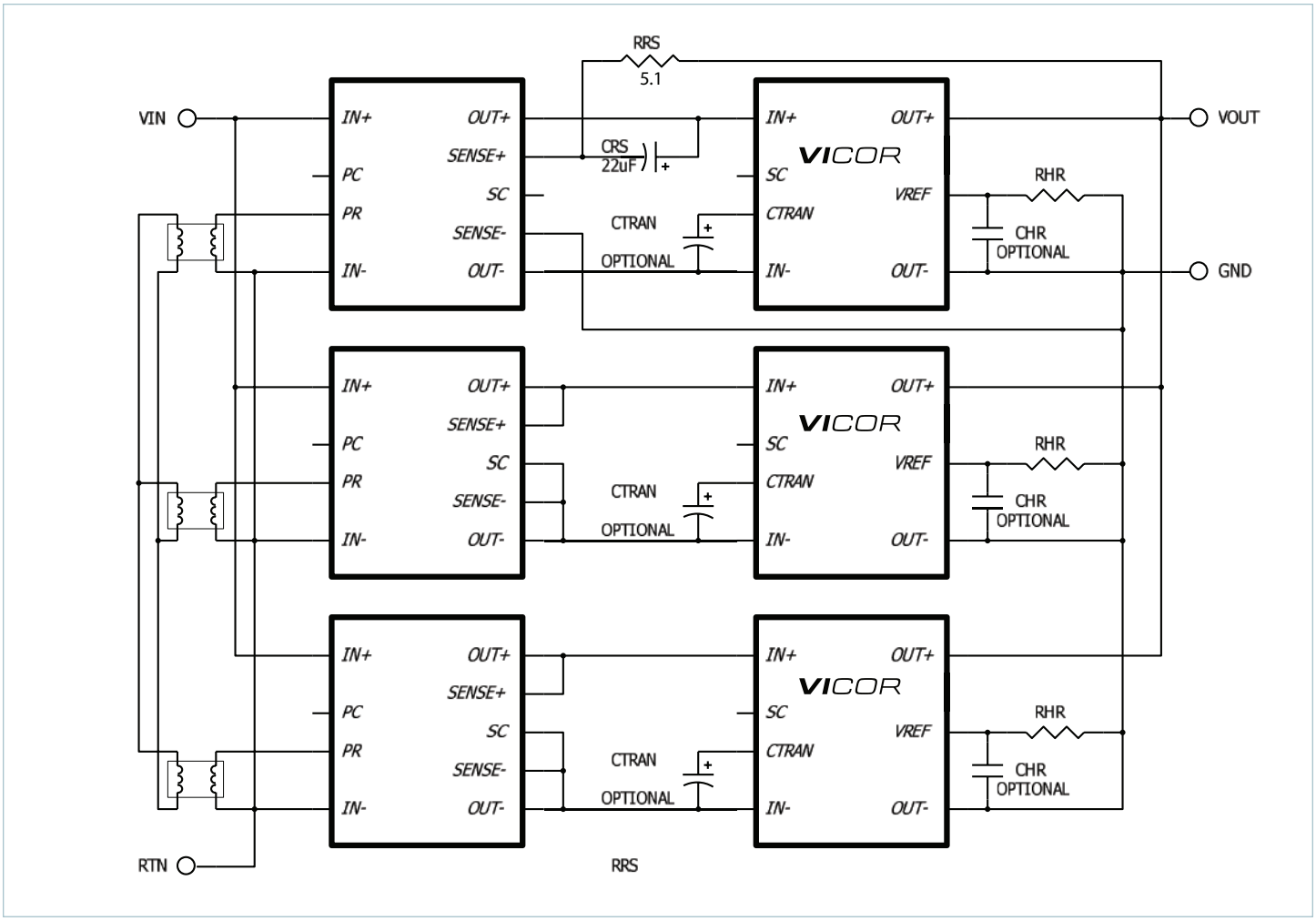


Figure 16 — *Recommended paralleling connections of Vicor converters and paired MicroRAMs.*

A MicroRAM doesn't have the capability to current share when paralleling with another filter. To use the MicroRAM in parallel/ redundant designs, the recommended method is to have one converter act as the "parent" controller of the system, forcing the paralleled converters to act as "child" devices, regulated by the parent via the PR pins. Figure 17 shows a simplified version of the circuit. For more detailed information, please refer to these Vicor application notes:

http://www.vicorpower.com/documents/application_notes/an2_pr-pin.pdf

http://www.vicorpower.com/documents/application_notes/AN_Designing High-Power Arrays.pdf

Filter Calculator Application

To make the task of calculating the required external resistors much easier, Vicor has developed a filter calculator program that is designed to be used with the MicroRAM output filter as well as with QPO output filters.

The filter program will automatically calculate any trim resistors that might be required, in either remote sense or SC control modes, and all the external resistors required by the filter. The resulting values are of standard 1% tolerance resistors.

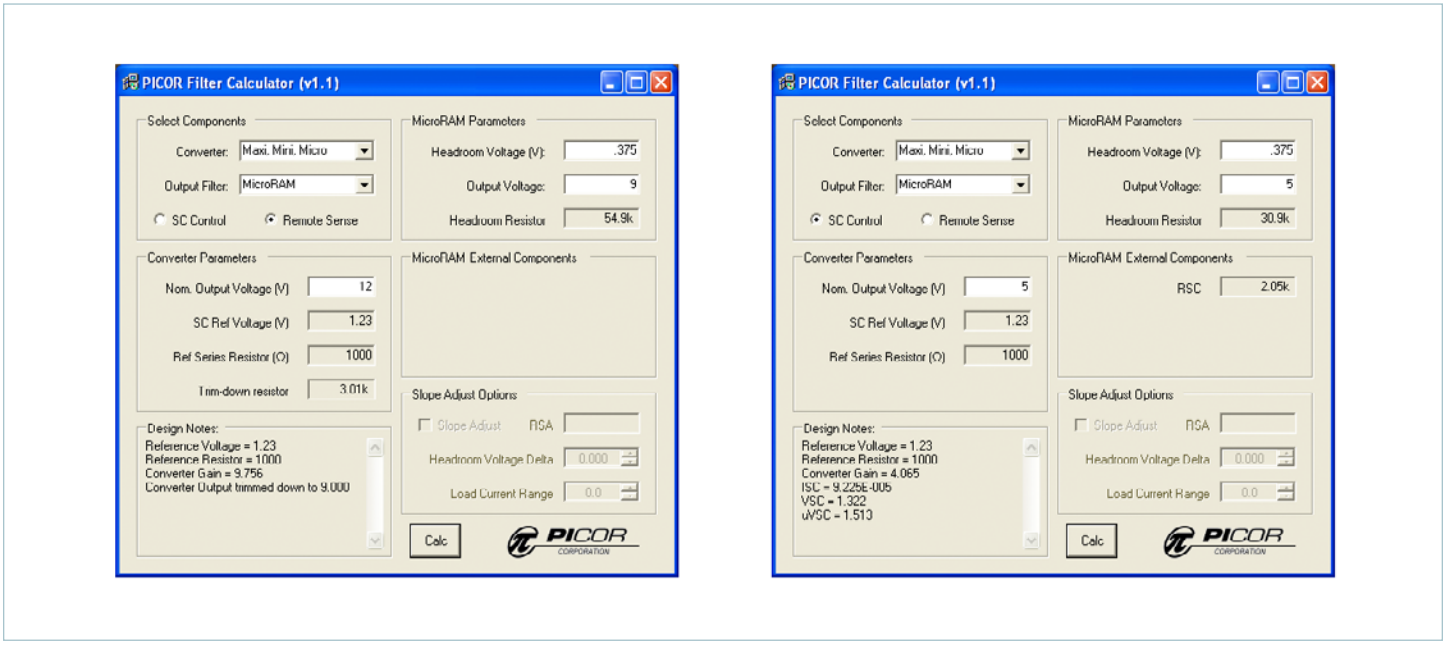


Figure 17 — *Screen shots of the Filter Calculator program for determining the external resistor values used in the circuits of Figures 10 and 11*

Note: The screen shots shown in Figure 17 are of the output filter calculator program, a tool which can be used to calculate the resistor values needed in the circuits shown in Figure 10 and Figure 11. This program is a Windows based executable file that is available to Vicor Applications Engineering, and which can also made available to our customers upon request. To request a copy of the program please contact your local Vicor Field Applications Engineer or email your request to apps@vicorpower.com.

Application Notes

Load capacitance can affect the overall phase margin of the MicroRAM active loop as well as the phase margin of the converter loop. The distributed variables such as inductance of the load path, the capacitor type and value as well as its ESR and ESL also affect transient capability at the load. The following guidelines are based on circuit simulation and should be considered when point of load capacitance is used with the MicroRAM in order to maintain a minimum of 30° of phase margin.

Using ceramic load capacitance with <1milliohm ESR and <1nH ESL:

20 – 200µF requires 20nH of trace/wire load path inductance

200 – 1,000µF requires 60nH of trace/wire load path inductance

For the case where load capacitance is connected directly to the output of the MicroRAM, i.e., no trace inductance, and the ESR is >1mΩ:

20 – 200µF load capacitance needs an ESL of >50nH

200 – 1,000µF load capacitance needs an ESL of >5nH

Adding low ESR capacitance directly at the output terminals of MicroRAM is not recommended and may cause stability problems.

In practice the distributed board or wire inductance at a load or on a load board will be sufficient to isolate the output of the MicroRAM from any load capacitance and minimize any appreciable effect on phase margin.

Recommended PCB Layout

To achieve the best attenuation, proper routing of the power nodes must be followed. The V_{IN-} and V_{OUT-} are internally connected within the MicroRAM module and should not be connected externally. Doing so will create a ground loop and will degrade attenuation results. All measurements should be made using the VOUT– of the MicroRAM as reference ground. If possible, waveform measurements should be made with an oscilloscope that is AC line isolated from other test equipment, and should use probes without the grounding clip attached.
Please contact apps@vicorpower.com for of proper PARD measurements techniques.

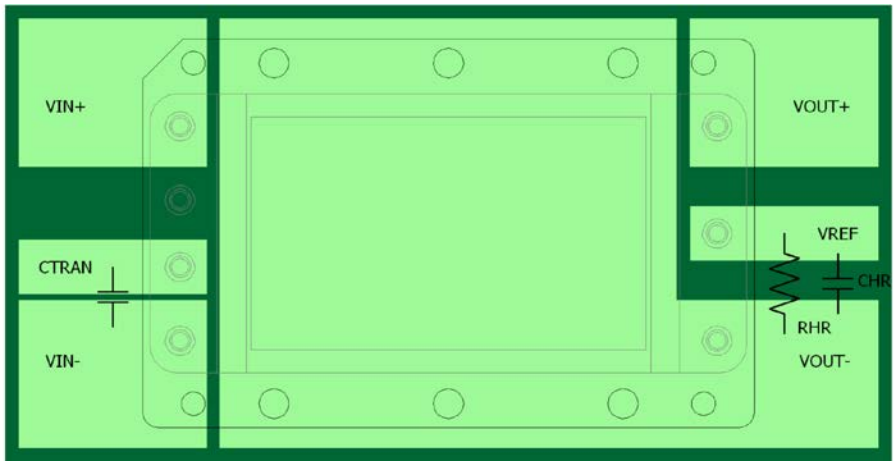


Figure 18 — *Recommended copper patterns, top view*

µRAM2xxx

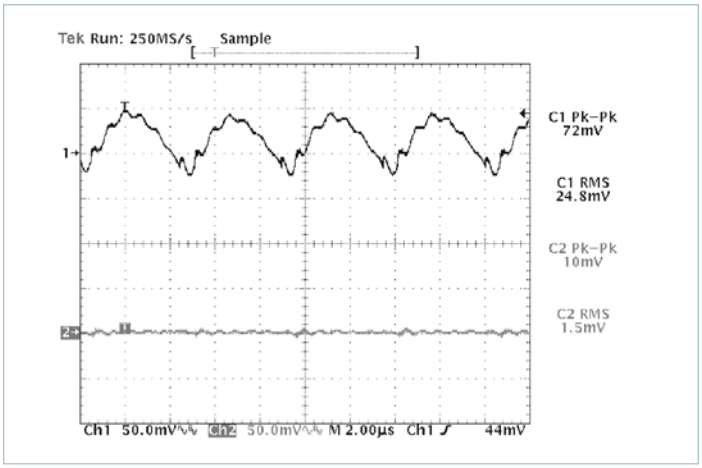


Figure 19 — *V375A28C600B and µRAM; Input and output ripple @50% (10A) load CH1 = V_{IN}; CH2 = V_{OUT}; $V_{IN} - V_{OUT}$ = 332mV; R_{HR} = 178kΩ*

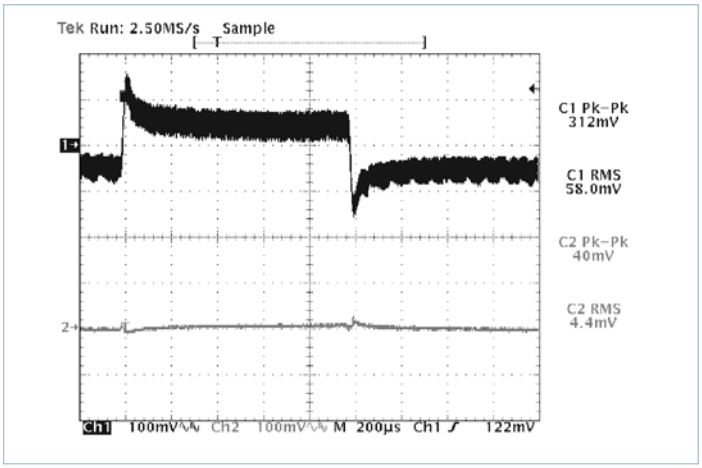


Figure 20 — *V375A28C600B and µRAM; Input and output dynamic response no added C_{TRAN}; 20% of 20A rating load step of 4A (10A – 14A); R_{HR} = 178kΩ (configured as in Figure 7 w/o Trim)*

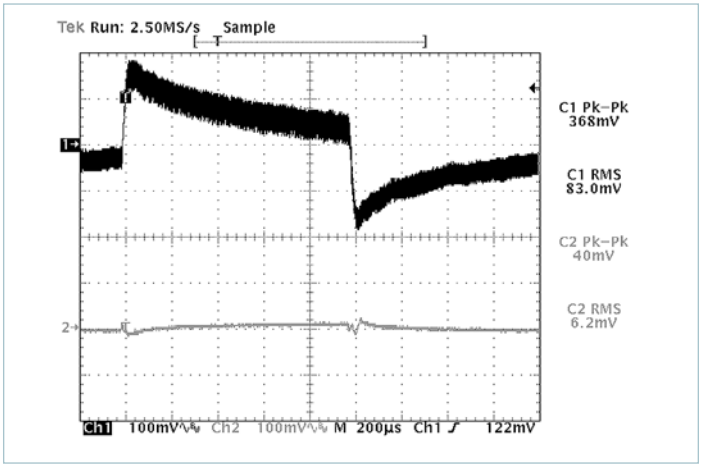


Figure 21 — *V375A28C600B and µRAM; Input and output dynamic response C_{TRAN} = 820µF Electrolytic; 32.5% of load step of 6.5A (10A – 16.5A); R_{HR} = 178kΩ (configured as in Figure 7 w/o Trim)*

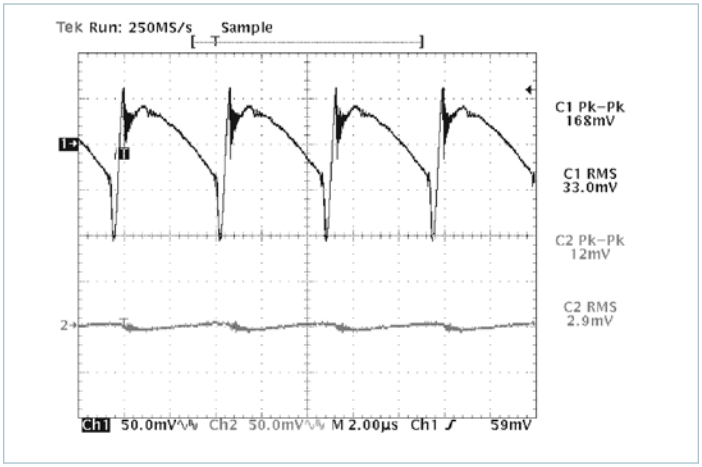


Figure 22 — *V375B12C250B and µRAM; Input and output ripple @50% (10A) load CH1 = V_{IN}; CH2 = V_{OUT}; $V_{IN} - V_{OUT}$ = 305mV; R_{HR} = 80kΩ (configured as in Figure 7 w/o Trim)*

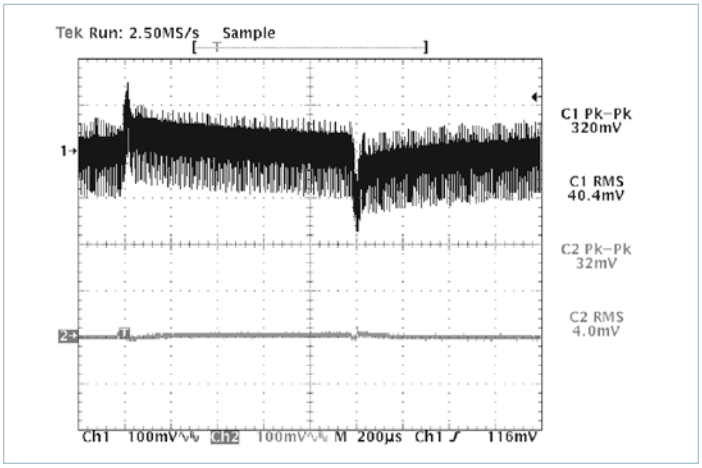


Figure 23 — *V300B12C250B and µRAM; Input and output dynamic response no added C_{TRAN}; 17.5% of 20A rating load step of 3.5A (10A – 13.5A); R_{HR} = 80kΩ (configured as in Figure 7 w/o Trim)*

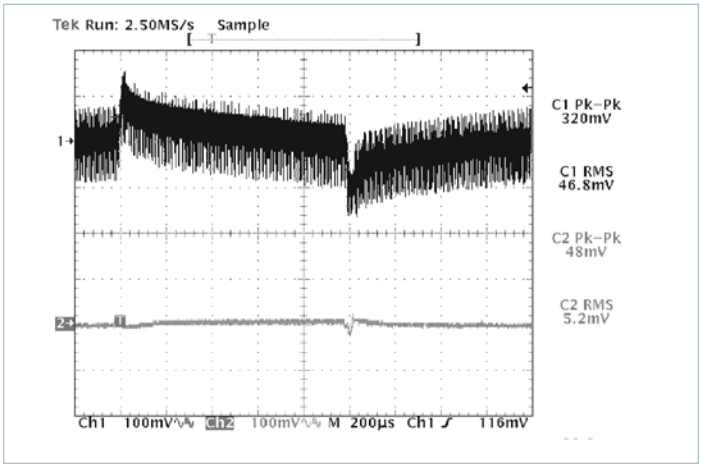


Figure 24 — *V300B12C250B and µRAM; Input and output dynamic response C_{TRAN} = 820µF Electrolytic; 30% of load step of 6A (10A – 16A); R_{HR} = 80kΩ (configured as in Figure 8 w/o Trim)*

µRAM2xxx

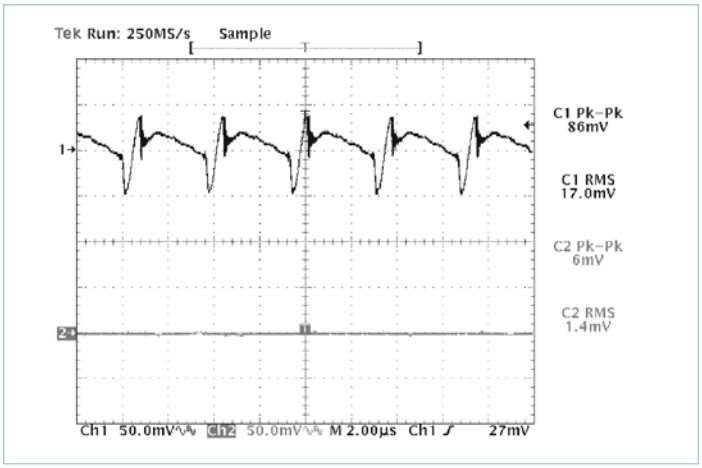


Figure 25 — *V48C5C100B and µRAM; Input and output ripple @50% (10A) load CH1 = V_{IN}; CH2 = V_{OUT}; $V_{IN} - V_{OUT}$ = 327mV; R_{HR} = 31kΩ (configured as in Figure 8)*

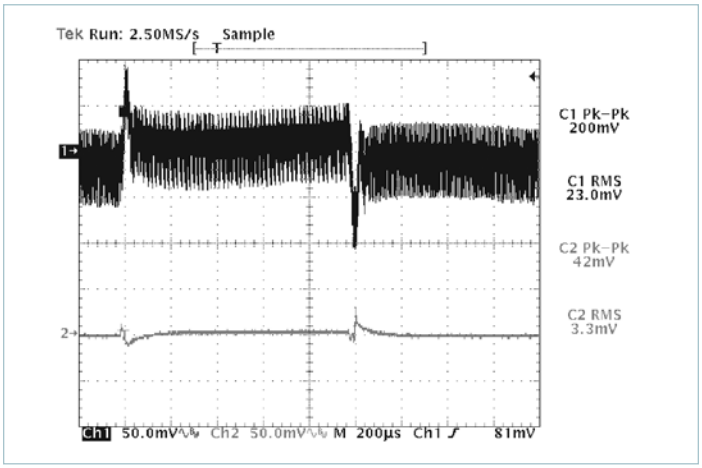


Figure 26 — *V48C5C100B and µRAM; Input and output dynamic response no added C_{TRAN}; 22.5% of 20A rating load step of 4.5A (10A – 14.5A); R_{HR} = 31kΩ (configured as in Figure 8)*

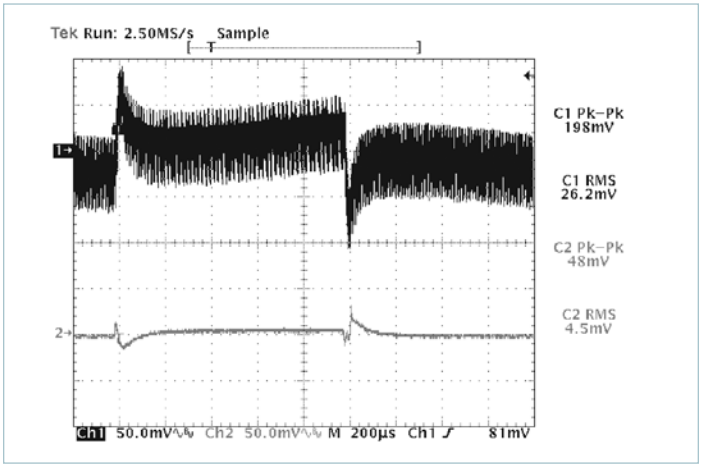


Figure 27 — *V48C5C100B and µRAM; Input and output dynamic response C_{TRAN} = 820µF Electrolytic; 35% of load step of 7A (10A – 17A); R_{HR} = 31kΩ (configured as in Figure 8)*

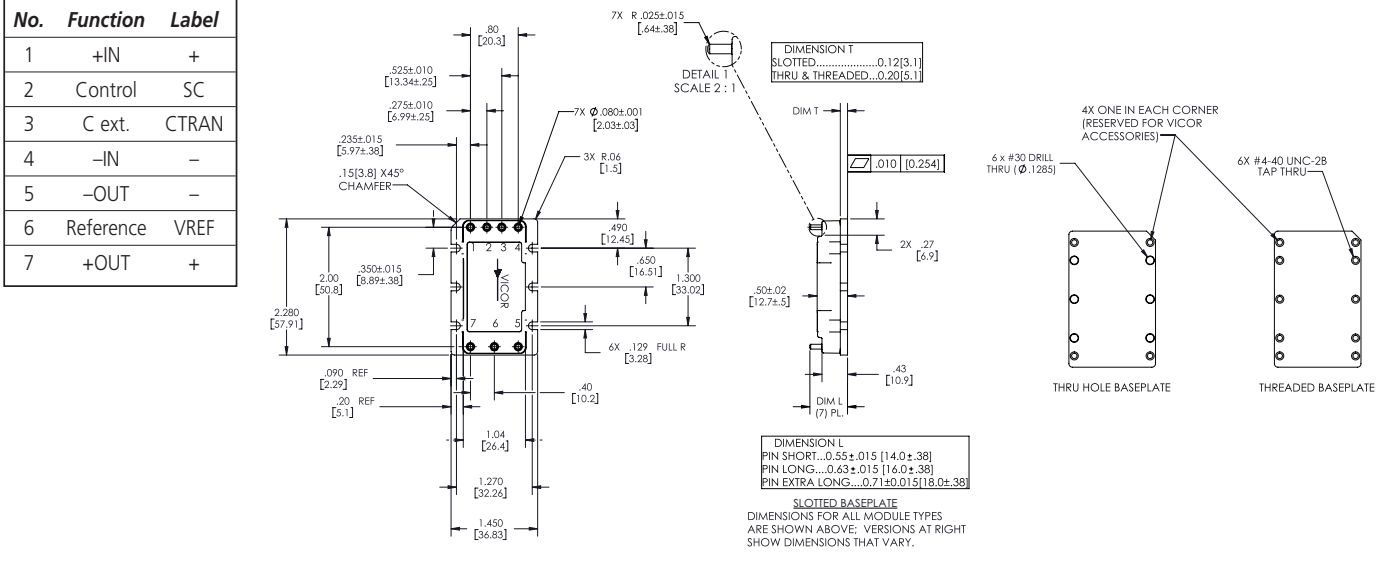
Storage

Vicor products, when not installed in customer units, should be stored in ESD safe packaging in accordance with ANSI/ESD S20.20, "Protection of Electrical and Electronic Parts, Assemblies and Equipment" and should be maintained in a temperature controlled factory/ warehouse environment not exposed to outside elements controlled between the temperature ranges of 15°C and 38°C. Humidity shall not be condensing, no minimum humidity when stored in an ESD compliant package.

Notes: The measurements in Figures 20 – 28 were taken with a µRAM2C21 and standard scope probes with a 20MHz bandwidth scope setting. The criteria for transient current capability was as follows: The transient load current step was incremented from 10A to the peak value indicated, then stepped back to 10A until the resulting output peak to peak was around 40mV.

Mechanical Drawings

µRAM Pins		
No.	*Function*	*Label*
1	+IN	+
2	Control	SC
3	C ext.	CTRAN
4	–IN	–
5	–OUT	–
6	Reference	VREF
7	+OUT	+



NOTES:
1. MATERIAL:
   BASE: 6000 SERIES ALUMINUM
   PIN PLATING: NICKEL BARRIER FOLLOWED BY
   (RoHS PINS) GOLD PLATE (30 MICRO INCH MIN); OR PALLADIUM (35 UIN MIN), FOLLOWED BY 3 TO 5 UIN GOLD.
   (NON-RoHS PINS) TIN/LEAD 90/10 BRIGHT
2. DIMENSIONS AND VALUES IN BRACKETS ARE METRIC
3. MANUFACTURING CONTROL IS IN PLACE TO ENSURE THAT THE SPACING BETWEEN THE MODULES LABEL SURFACE TO THE PRINTED CIRCUIT BOARD OF THE APPLICATION RANGES FROM DIRECT CONTACT (ZERO), TO THE MAXIMUM GAP AS CALCULATED FROM THE TOLERANCE STACK-UP AND IS NOT SUBJECT NEGATIVE TOLERANCE ACCUMULATION

Figure 28 — *Module outline*

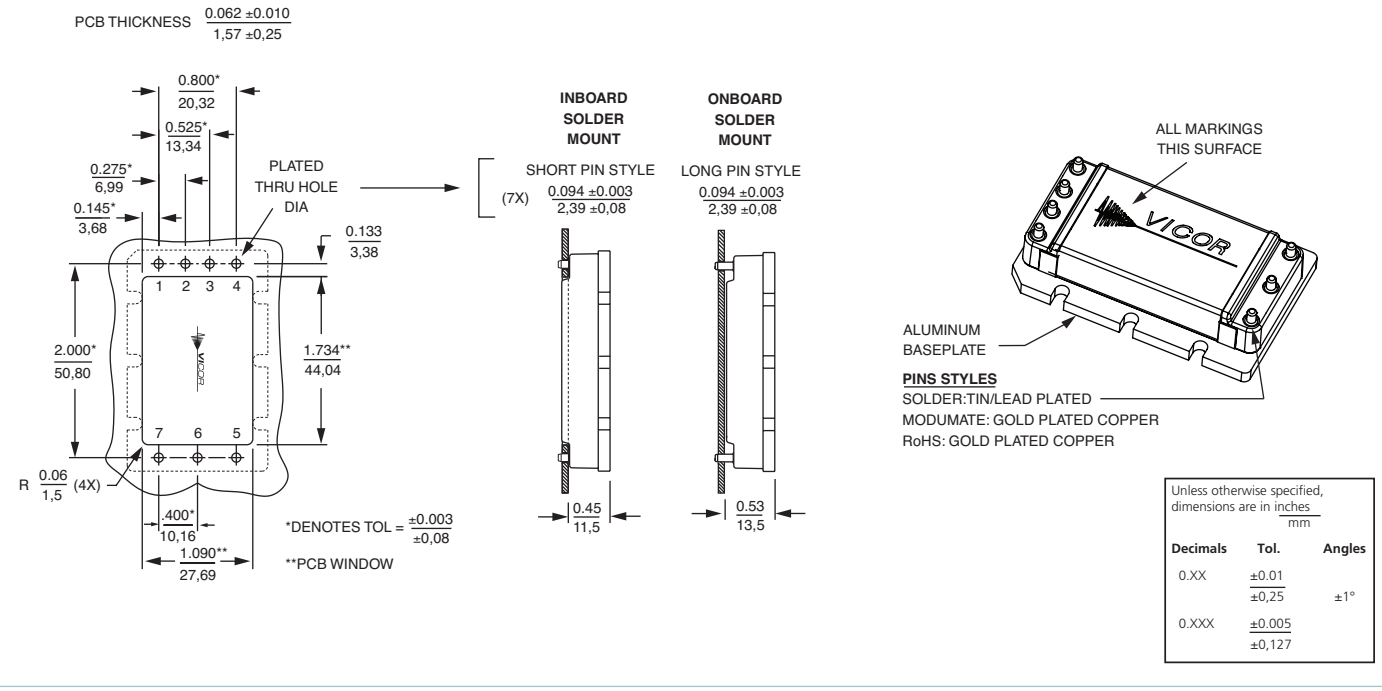


Figure 29 — *PCB mounting specifications*

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