TPS6112x Synchronous Boost Converter With 1.1-A Switch and Integrated LDO

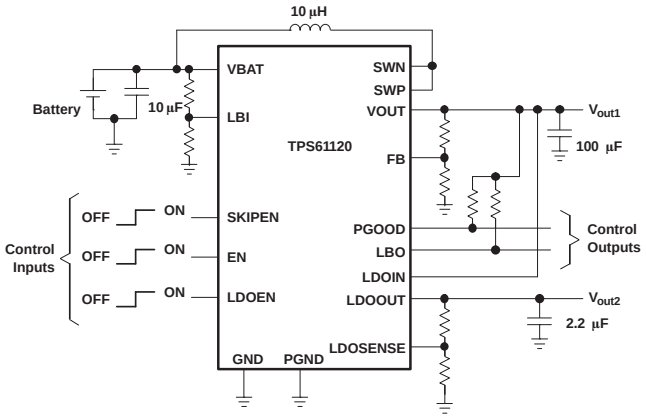
1 Features

- Synchronous, 95% Efficient, Boost Converter With 500-mA Output Current From 1.8-V Input
- Integrated 200-mA Reverse Voltage Protected LDO for DC-DC Output Voltage Post Regulation or Second Output Voltage
- 40-µA (Typical) Total Device Quiescent Current
- Input Voltage Range: 1.8 V to 5.5 V
- Fixed and Adjustable Output Voltage Options up to 5.5 V
- Power Save Mode for Improved Efficiency at Low Output Power
- Low Battery Comparator
- Power Good Output
- Low EMI-Converter (Integrated Antiringing Switch)
- Load Disconnect During Shutdown
- Overtemperature Protection
- Available in a Small 4-mm × 4-mm VQFN-16 or in a TSSOP-16 Package

2 Applications

- All Single Cell Li or Dual Cell Battery or USB Powered Products as MP-3 Player, PDAs, and Other Portable Equipment
- Dual Input or Dual Output Mode
- Simple Li-Ion to 3.3-V Conversion

Typical Application Schematic



3 Description

The TPS6112x devices provide a complete power supply solution for products powered by either a one-cell Li-Ion or Li-Polymer by either a one-cell Li-Ion or Li-Polymer battery, or a two- to four-cell Alkaline, NiCd, or NiMH battery. The devices can generate two stable output voltages that are either adjusted by an external resistor divider or are fixed internally on the chip. The device also provides a simple solution for generating 3.3 V out of a one-cell Li-Ion or Li-Polymer battery at a maximum output current of at least 200 mA with supply voltages down to 1.8 V. The implemented boost converter is based on a fixed frequency, pulse-width-modulation (PWM) controller using a synchronous rectifier to obtain maximum efficiency. The maximum peak current in the boost switch is limited to a value of 1600 mA.

The converter can be disabled to minimize battery drain. During shutdown, the load is completely disconnected from the battery. A low-EMI mode is implemented to reduce ringing and, in effect, lower radiated electromagnetic energy when the converter enters discontinuous conduction mode. A power good output at the boost stage simplifies control of any connected circuits like cascaded power supply stages or microprocessors.

The built-in LDO can be used for a second output voltage derived either from the boost output or directly from the battery. The LDO can be enabled separately that is, using the power good of the boost stage. The device is packaged in a 16-pin VQFN (RSA) package measuring 4 mm x 4 mm or in a 16-pin TSSOP (PW) package.

Device Information(1)

PART NUMBER	PACKAGE	BODY SIZE (NOM)
TPS61120	TSSOP (16)	5.00 mm × 4.40 mm
	VQFN (16)	4.00 mm × 4.00 mm
TPS61121	TSSOP (16)	5.00 mm × 4.40 mm
TPS61122		

(1) For all available packages, see the orderable addendum at the end of the datasheet.

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4 Revision History

Changes from Revision C (April 2004) to Revision D **Page**

- Added *Pin Configuration and Functions* section, *ESD Ratings* table, *Feature Description* section, *Device Functional Modes*, *Application and Implementation* section, *Power Supply Recommendations* section, *Layout* section, *Device and Documentation Support* section, and *Mechanical, Packaging, and Orderable Information* section ... 1

5 Device Options

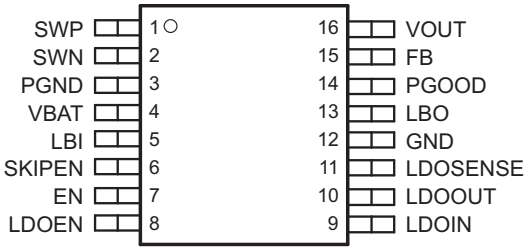
Table 1. Available Output Voltage Options(1)

PART NUMBER(2)	OUTPUT VOLTAGE DC-DC	OUTPUT VOLTAGE LDO
TPS61120PW	Adjustable	Adjustable
TPS61121PW	3.3 V	1.5 V
TPS61122PW	3.6 V	3.3 V
TPS61120RSA	Adjustable	Adjustable
TPS61121RSA	3.3 V	1.5 V

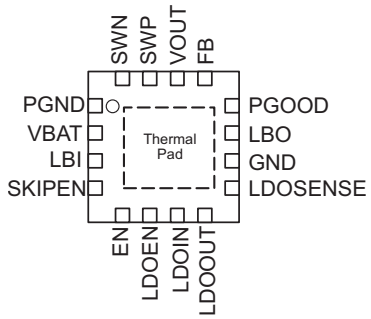
(1) Contact the factory to check availability of other fixed output voltage versions.
(2) The packages are available taped and reeled. Add R suffix to device type (for example TPS61120PWR or TPS61120RSAR) to order quantities of 2000 devices per reel for the TSSOP (PW) package and 3000 devices per reel for the QFN (RSA) package.

6 Pin Configuration and Functions

PW Package
16-Pin TSSOP
Top View



RSA Package
16-Pin VQFN With Thermal Pad
Top View



Pin Functions

PIN			I/O	DESCRIPTION
NAME	NO.			
	TSSOP	VQFN		
EN	7	5	I	DC-DC-enable input. (1: VBAT enabled, 0: GND disabled)
FB	15	13	I	DC-DC voltage feedback of adjustable versions
GND	12	10	I/O	Control/logic ground
LBI	5	3	I	Low battery comparator input (comparator enabled with EN)
LBO	13	11	O	Low battery comparator output (open drain)
LDOEN	8	6	I	LDO-enable input (1: LDOIN enabled, 0: GND disabled)
LDOOUT	10	8	O	LDO output
LDOIN	9	7	I	LDO input
LDOSENSE	11	9	I	LDO feedback for voltage adjustment, must be connected to LDOOUT at fixed output voltage versions
SWP	1	15	I	DC-DC rectifying switch input
PGND	3	1	I/O	Power ground
PGOOD	14	12	O	DC-DC output power good (1: good, 0 : failure) (open drain)
SKIPEN	6	4	I	Enable/disable power save mode (1: VBAT enabled, 0: GND disabled)
SWN	2	16	I	DC-DC switch input
VBAT	4	2	I	Supply pin
VOUT	16	14	O	DC-DC output

7 Specifications

7.1 Absolute Maximum Ratings

over operating free-air temperature range unless otherwise noted(1)

		MIN	MAX	UNIT
Input voltage	FB	–0.3	3.6	V
	SWN, SWP	–0.3	10	V
	VOUT, LDOIN, LDOOUT, LDOEN, LDOSENSE, PGOOD, LBO, VBAT, LBI, SKIPEN, EN	–0.3	7	V
Maximum junction temperature T_J		–40	150	°C
Storage temperature T_{stg}		–65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

7.2 ESD Ratings

		VALUE	UNIT
$V_{(ESD)}$ Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)	±2000	V
	Charged-device model (CDM), per JEDEC specification JESD22-C101(2)	±750	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

7.3 Recommended Operating Conditions

	MIN	NOM	MAX	UNIT
Supply voltage at VBAT, V_I	1.8		5.5	V
Operating ambient temperature range, T_A	–40		85	°C
Operating virtual junction temperature range, T_J	–40		125	°C

7.4 Thermal Information

THERMAL METRIC(1)		TPS61120, TPS61121, TPS61122	TPS61120	UNIT
		PW (TSSOP)	RSA (VQFN)	
		16 PINS	16 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	100.5	33.9	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	35.8	36.3	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	45.4	11	°C/W
ψ_{JT}	Junction-to-top characterization parameter	2.6	0.5	°C/W
ψ_{JB}	Junction-to-board characterization parameter	44.8	11	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	n/a	2.2	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report, SPRA953.

7.5 Electrical Characteristics

over recommended free-air temperature range and over recommended input voltage range (typical at an ambient temperature range of 25°C) (unless otherwise noted)

PARAMETER			TEST CONDITIONS	MIN	TYP	MAX	UNIT
DC-DC STAGE							
V_I	Input voltage range			1.8		5.5	V
V_O	Adjustable output voltage range (TPS61120)			2.5		5.5	V
V_{ref}	Reference voltage			485	500	515	mV
f	Oscillator frequency			400	500	600	kHz
I_{SW}	Switch current limit		VOUT= 3.3 V	1100	1300	1600	mA
	Startup current limit				0.4 * I_{SW}		mA
	SWN switch on resistance		VOUT= 3.3 V		200	350	mΩ
	SWP switch on resistance		VOUT= 3.3 V		250	500	mΩ
	Total accuracy (including line and load regulation)			-3%		±3%	
	DC-DC quiescent current	into VBAT	I_O= 0 mA, V_{EN} = VBAT = 1.8 V, VOUT = 3.3 V, ENLDO = 0		10	25	µA
		into VOUT	I_O = 0 mA, V_{EN} = VBAT = 1.8 V, VOUT = 3.3 V, ENLDO = 0		10	25	µA
	DC-DC shutdown current		V_{EN}= 0 V		0.2	1	µA
LDO STAGE							
$V_{I(LDO)}$	Input voltage range			1.8		7	V
$V_{O(LDO)}$	Adjustable output voltage range (TPS61120)			0.9		5.5	V
$I_{O(max)}$	Output current			200	320		mA
	LDO short circuit current limit					500	mA
	Minimum voltage drop		I_O= 200 mA			300	mV
	Total accuracy (including line and load regulation)		I_O≥ 1 mA			±3%	
	Line regulation		LDOIN change from 1.8 V to 2.6 V at 100 mA, LDOOUT = 1.5 V			0.6%	
	Load regulation		Load change from 10% to 90%, LDOIN = 3.3 V			0.6%	
	LDO quiescent current		LDOIN = 7 V, VBAT = 1.8 V, EN = VBAT		20	30	µA
	LDO shutdown current		LDOEN = 0 V, LDOIN = 7 V		0.1	1	µA
CONTROL STAGE							
V_{IL}	LBI voltage threshold		V_{LBI} voltage decreasing	490	500	510	mV
	LBI input hysteresis				10		mV
	LBI input current		EN = VBAT or GND		0.01	0.1	µA
	LBO output low voltage		V_O = 3.3 V, I_{OI} = 100 µA		0.04	0.4	V
	LBO output low current				100		µA
	LBO output leakage current		V_{LBO} = 7 V		0.01	0.1	µA
V_{IL}	EN, SKIPEN input low voltage					0.2 × VBAT	V
V_{IH}	EN, SKIPEN input high voltage			0.8 × VBAT			V
V_{IL}	LDOEN input low voltage					0.2 × V_{LDOIN}	V
V_{IH}	LDOEN input high voltage			0.8 × V_{LDOIN}			V
	EN, SKIPEN input current		Clamped on GND or VBAT		0.01	0.1	µA
	Power-Good threshold		V_O = 3.3 V	0.9*V_O	0.92*V_O	0.95*V_O	V

Electrical Characteristics (continued)

over recommended free-air temperature range and over recommended input voltage range (typical at an ambient temperature range of 25°C) (unless otherwise noted)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Power-Good delay			30		µs
Power-Good output low voltage	V_O = 3.3 V, I_{OI} = 100 µA		0.04	0.4	V
Power-Good output low current			100		µA
Power-Good output leakage current	V_{PG} = 7 V		0.01	0.1	µA
Overtemperature protection			140		°C
Overtemperature hysteresis			20		°C

7.6 Typical Characteristics

Table 2. Table of Graphs

		FIGURE
BOOST CONVERTER		
Maximum output current	vs Input voltage	Figure 1, Figure 2
Efficiency	vs Output current (TPS61120) (V_O = 2.5 V, V_I = 1.8 V)	Figure 3
	vs Output current (TPS61121) (V_O = 3.3 V, V_I = 1.8 V, 2.4 V)	Figure 4
	vs Output current (TPS61120) (V_O = 5.0 V, V_I = 2.4 V, 3.3 V)	Figure 5
	vs Input voltage (TPS61121)	Figure 6
Output voltage	vs Output current (TPS61121)	Figure 7
No-load supply current into VBAT	vs Input voltage (TPS61121)	Figure 8
No-load supply current into VOUT	vs Input voltage (TPS61121)	Figure 9
LDO		
Maximum output current	vs Input voltage (V_O = 2.5 V, 3.3 V)	Figure 10
	vs Input voltage (V_O = 1.5 V, 1.8 V)	Figure 11
Output voltage	vs Output current (TPS61122)	Figure 12
Dropout voltage	vs Output current (TPS61121, TPS61122)	Figure 13
Supply current into LDOIN	vs LDOIN input voltage (TPS61121)	Figure 14
PSRR	vs Frequency (TPS61121)	Figure 15

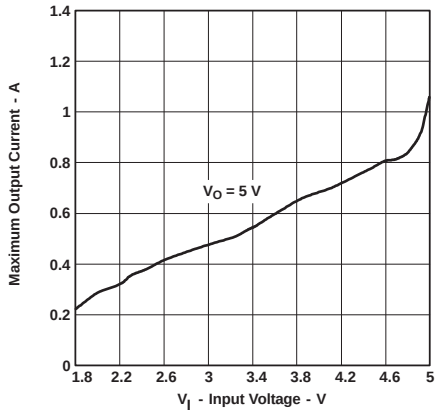


Figure 1. TPS61120 Maximum Boost Converter Output Current vs Input Voltage

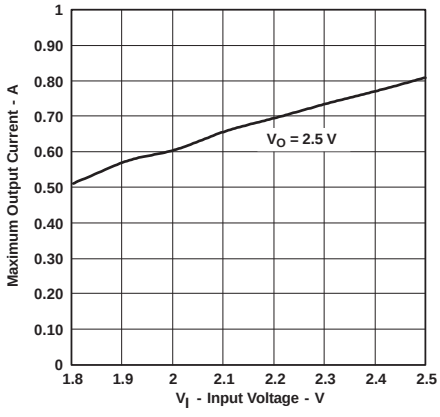


Figure 2. TPS61120 Maximum Boost Converter Output Current vs Input Voltage

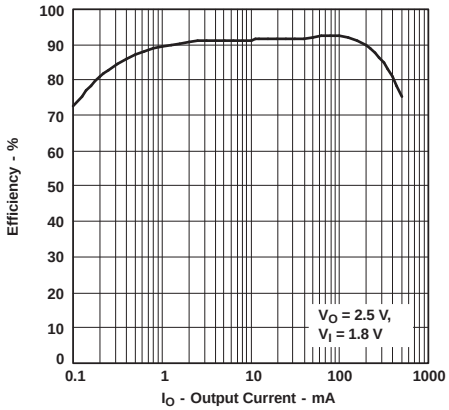


Figure 3. TPS61120 Boost Converter Efficiency vs Output Current

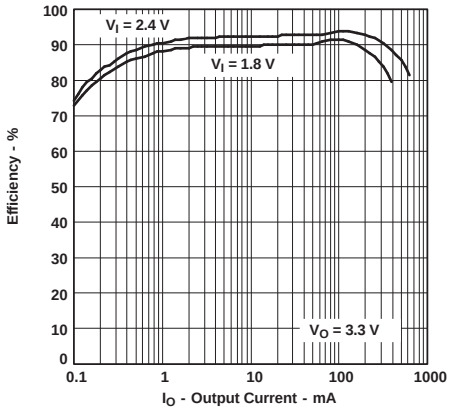


Figure 4. TPS61121 Boost Converter Efficiency vs Output Current

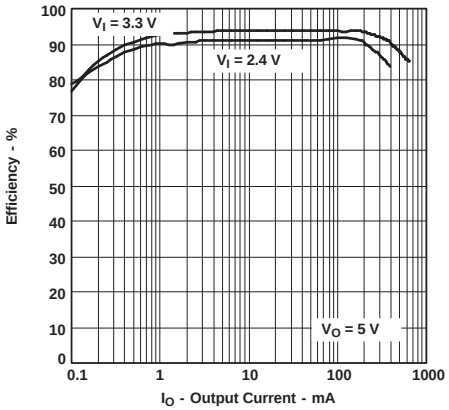


Figure 5. TPS61120 Boost Converter Efficiency vs Output Current

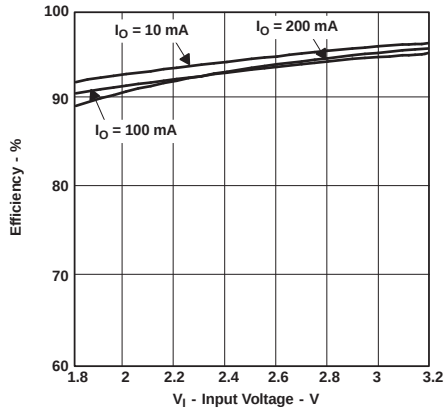


Figure 6. TPS61121 Boost Converter Efficiency vs Input Voltage

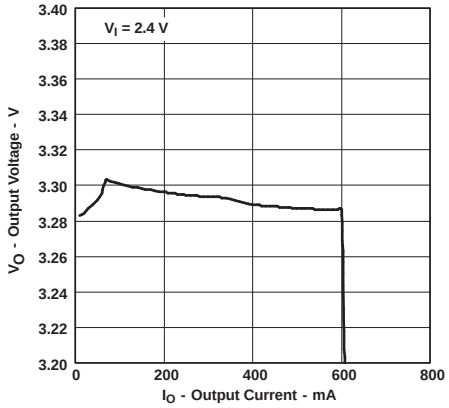


Figure 7. TPS61121 Boost Converter Output Voltage vs Output Current

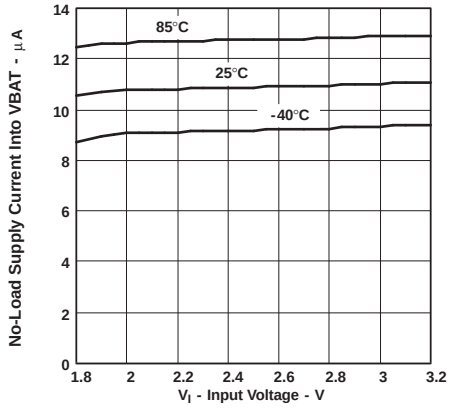


Figure 8. TPS61121 No-Load Supply Current Into VBAT vs Input Voltage

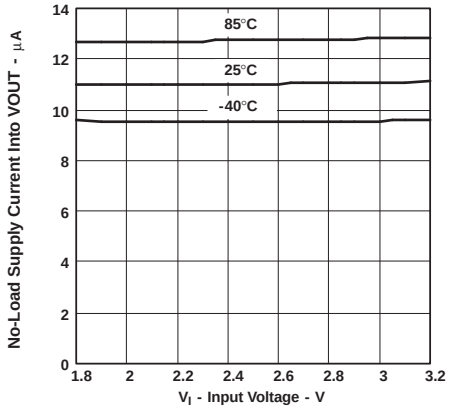


Figure 9. TPS61121 No-Load Supply Current Into VOUT vs Input Voltage

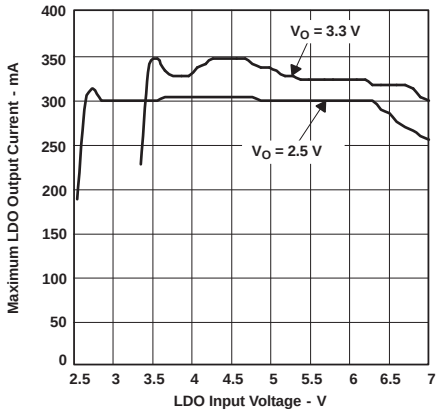


Figure 10. TPS61120 Maximum LDO Output Current vs LDO Input Voltage

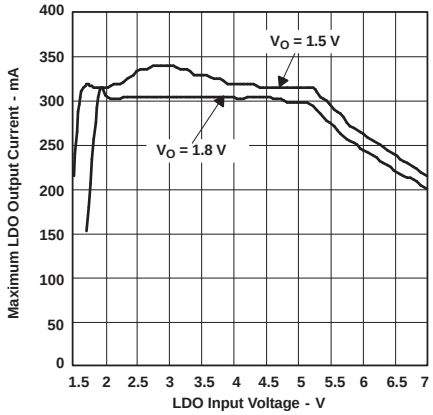


Figure 11. TPS61120 Maximum LDO Output Current vs LDO Input Voltage

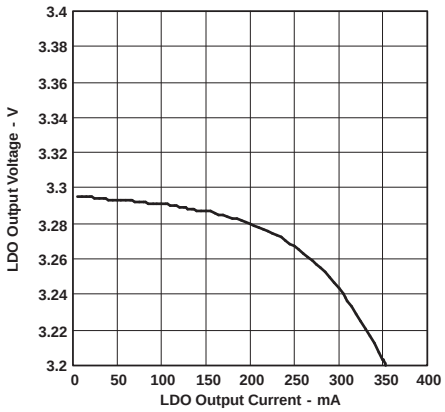


Figure 12. TPS61122 LDO Output Voltage vs LDO Output Current

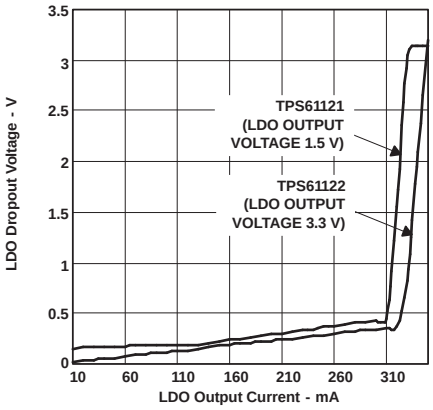


Figure 13. LDO Dropout Voltage vs LDO Output Current

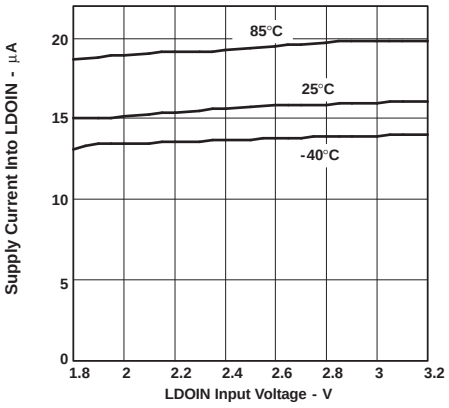


Figure 14. TPS61121 Supply Current Into LDOIN vs LDO Input Voltage

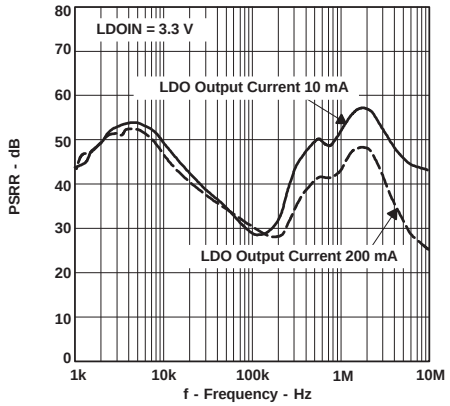


Figure 15. TPS61121 PSRR vs Frequency

8 Parameter Measurement Information

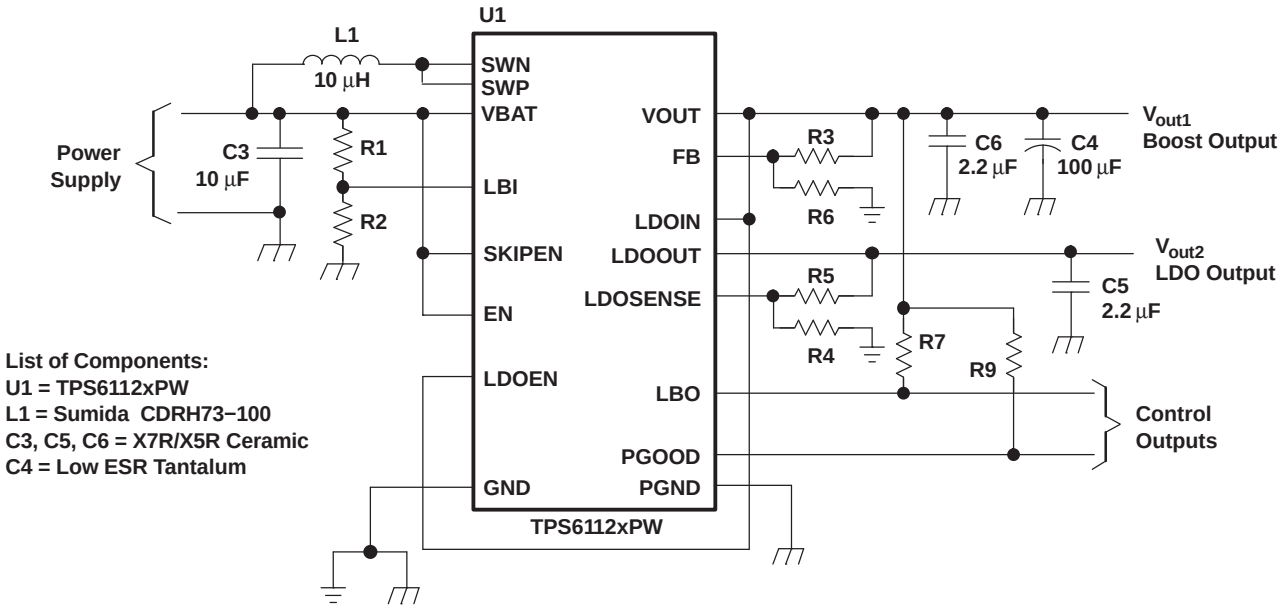


Figure 16. TPS61120 Typical Application Schematic

9 Detailed Description

9.1 Overview

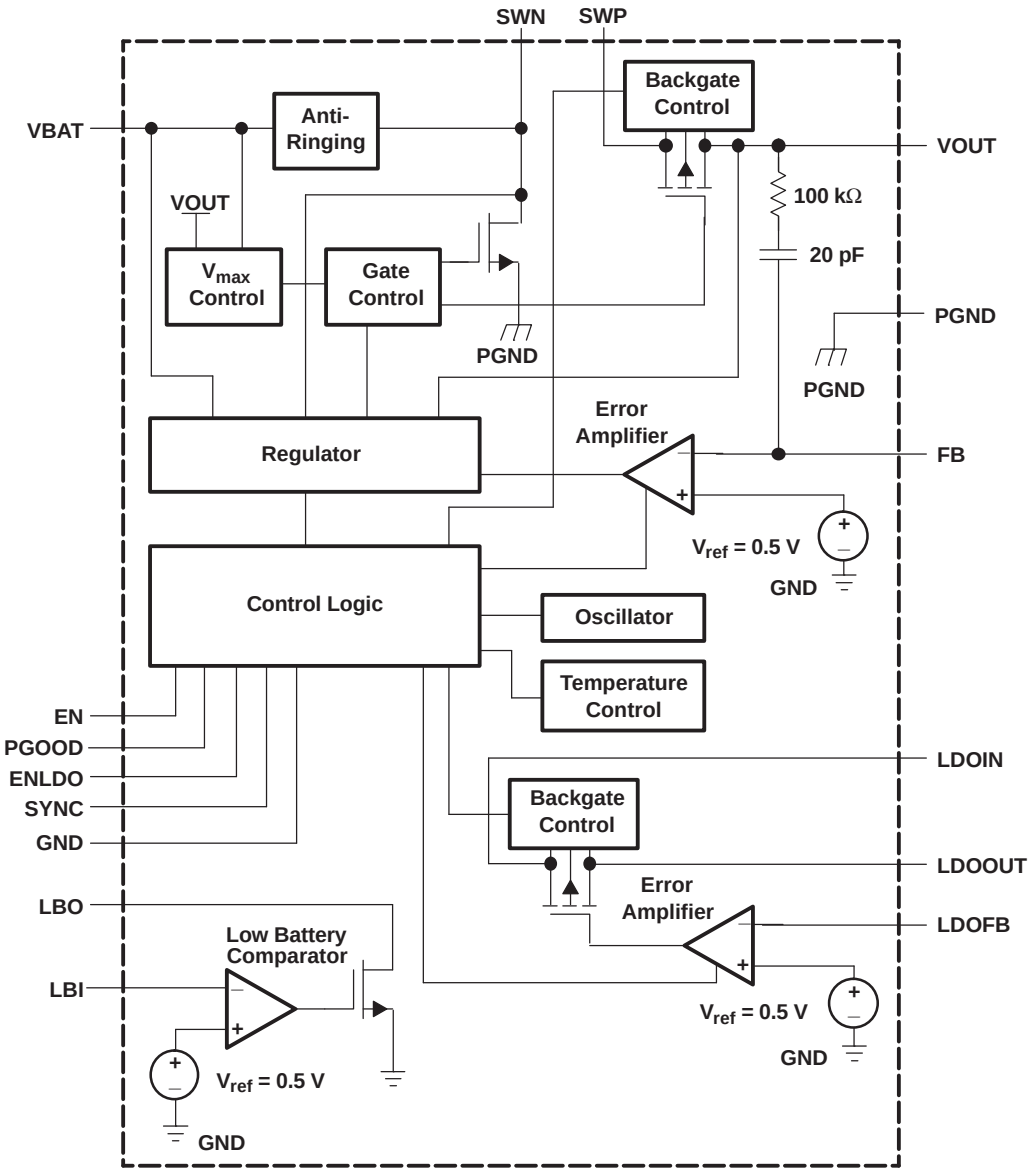
The TPS6112x synchronous step-up converter typically operates at a 500-kHz frequency pulse width modulation (PWM) at moderate to heavy load currents. The converter enters Power Save mode at low load currents to maintain a high efficiency over a wide load. The Power Save mode can also be disabled, forcing the converter to operate at a fixed switching frequency.

The TPS6112x family of devices is based on a fixed frequency with multiple feed forward controller topology. Input voltage, output voltage, and voltage drop on the NMOS switch are monitored and forwarded to the regulator. Also, the peak current of the NMOS switch is sensed to limit the maximum current flowing through the switch and the inductor.

The device includes an additional built-in LDO which can be used to generate a second output voltage derived from the output of the TPS6112x or an external power supply.

Additionally, TPS6112x integrated the low-battery detector circuit is used to supervise the battery voltage and to generate an error flag when the battery voltage drops below a user-set threshold voltage.

9.2 Functional Block Diagram



9.3 Feature Description

9.3.1 Controller Circuit

The controller circuit of the device is based on a fixed-frequency multiple feedforward controller topology. Input voltage, output voltage, and voltage drop on the NMOS switch are monitored and forwarded to the regulator. So changes in the operating conditions of the converter directly affect the duty cycle and must not take the indirect and slow way through the control loop and the error amplifier. The control loop, determined by the error amplifier, only has to handle small signal errors. The input for it is the feedback voltage on the FB pin or, at fixed output voltage versions, the voltage on the internal resistor divider. It is compared with the internal reference voltage to generate an accurate and stable output voltage.

The peak current of the NMOS switch is also sensed to limit the maximum current flowing through the switch and the inductor. The typical peak current limit is set to 1300 mA. An internal temperature sensor prevents the device from getting overheated in case of excessive power dissipation.

Feature Description (continued)

9.3.2 Synchronous Rectifier

The device integrates an N-channel and a P-channel MOSFET transistor to realize a synchronous rectifier. Because the commonly used discrete Schottky rectifier is replaced with a low RDS(ON) PMOS switch, the power conversion efficiency reaches 95%. To avoid ground shift due to the high currents in the NMOS switch, two separate ground pins are used. The reference for all control functions is the GND pin. The source of the NMOS switch is connected to PGND. Both grounds must be connected on the PCB at only one point close to the GND pin. A special circuit is applied to disconnect the load from the input during shutdown of the converter. In conventional synchronous rectifier circuits, the backgate diode of the high-side PMOS is forward biased in shutdown and allows current flowing from the battery to the output. This device however uses a special circuit which takes the cathode of the backgate diode of the high-side PMOS and disconnects it from the source when the regulator is not enabled (EN = low).

The benefit of this feature for the system design engineer is that the battery is not depleted during shutdown of the converter. No additional components have to be added to the design to make sure that the battery is disconnected from the output of the converter.

9.3.3 LDO

The built-in LDO can be used to generate a second output voltage derived from the DC-DC converter output, from the battery, or from another power source like an ac adapter or a USB power rail. The LDO is capable of being back biased. This allows the user to just connect the outputs of DC-DC converter and LDO. So the device is able to supply the load via DC-DC converter when the energy comes from the battery and efficiency is most important and from another external power source via the LDO when lower efficiency is not critical. The LDO must be disabled if the LDOIN voltage drops below LDOOUT to block reverse current flowing. The status of the DC-DC stage (enabled or disabled) does not matter.

9.3.4 Device Enable

The device is put into operation when EN is set high. It is put into a shutdown mode when EN is set to GND. In shutdown mode, the regulator stops switching, all internal control circuitry including the low-battery comparator is switched off, and the load is isolated from the input (as described in the *Synchronous Rectifier* section). This also means that the output voltage can drop below the input voltage during shutdown.

9.3.4.1 Undervoltage Lockout

An undervoltage lockout function prevents device start-up if the supply voltage on VBAT is lower than approximately 1.6 V. When in operation and the battery is being discharged, the device automatically enters the shutdown mode if the voltage on VBAT drops below approximately 1.6 V. This undervoltage lockout function is implemented in order to prevent the malfunctioning of the converter.

9.3.4.2 Softstart

During start-up of the converter, the duty cycle and the peak current are limited in order to avoid high peak currents drawn from the battery. When the boost section is enabled, the internal startup cycle starts with the first step, the precharge phase. During precharge, the rectifying switch is turned on until the output capacitor is charged to a value close to the input voltage. The rectifying switch current is limited in that phase. This also limits the output current under short-circuit conditions at the output. After charging the output capacitor to the input voltage the device starts switching. Until the output voltage is reached, the boost switch current limit is set to 40% of its nominal value to avoid high peak currents at the battery during startup. When the output voltage is reached, the regulator takes control and the switch current limit is set back to 100%.

9.3.5 LDO Enable

The LDO can be separately enabled and disabled by using the LDOEN pin in the same way as the EN pin at the DC-DC converter stage described above. This is completely independent of the status of the EN pin. The voltage levels of the logic signals which need to be applied at LDOEN are related to LDOIN.

Feature Description (continued)

9.3.6 Power Good

The PGOOD pin stays high impedance when the DC-DC converter delivers an output voltage within a defined voltage window. So it can be used to enable any connected circuitry such as cascaded converters (LDO) or to reset microprocessor circuits.

9.3.7 Low Battery Detector Circuit—LBI/LBO

The low-battery detector circuit is typically used to supervise the battery voltage and to generate an error flag when the battery voltage drops below a user-set threshold voltage. The function is active only when the device is enabled. When the device is disabled, the LBO pin is high-impedance. The switching threshold is 500 mV at LBI. During normal operation, LBO stays at high impedance when the voltage, applied at LBI, is above the threshold. It is active low when the voltage at LBI goes below 500 mV.

The battery voltage, at which the detection circuit switches, can be programmed with a resistive divider connected to the LBI pin. The resistive divider scales down the battery voltage to a voltage level of 500 mV, which is then compared to the LBI threshold voltage. The LBI pin has a built-in hysteresis of 10 mV. See the *Programming the LBI/LBO Threshold Voltage* section for more details about the programming of the LBI threshold. If the low-battery detection circuit is not used, the LBI pin should be connected to GND (or to VBAT) and the LBO pin can be left unconnected. Do not let the LBI pin float.

9.3.8 Low-EMI Switch

The device integrates a circuit that removes the ringing that typically appears on the SW node when the converter enters discontinuous current mode. In this case, the current through the inductor ramps to zero and the rectifying PMOS switch is turned off to prevent a reverse current flowing from the output capacitors back to the battery. Due to the remaining energy that is stored in parasitic components of the semiconductor and the inductor, a ringing on the SW pin is induced. The integrated antiringing switch clamps this voltage to VBAT and therefore dampens ringing.

9.4 Device Functional Modes

9.4.1 Power Save Mode

The SKIPEN pin can be used to select different operation modes. To enable the Power save mode, SKIPEN must be set high. Power save mode is used to improve efficiency at light loads. In power save mode, the converter only operates when the output voltage trips below a set threshold voltage. It ramps up the output voltage with several pulses, and goes again into power save mode once the output voltage exceeds the set threshold voltage. The skip mode can be disabled by setting the SKIPEN to GND.

10 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

10.1 Application Information

The TPS6112x DC-DC converters are intended for systems powered by a dual or triple cell NiCd or NiMH battery with a typical terminal voltage between 1.8 V and 5.5 V. They can also be used in systems powered by one-cell Li-Ion with a typical stack voltage between 2.5 V and 4.2 V. Additionally, two or three primary and secondary alkaline battery cells can be the power source in systems where the TPS6112x is used.

The built-in LDO can be used to generate a second output voltage derived from the DC-DC converter output, from the battery, or from another power source like an ac adapter or a USB power rail. The maximum programmable output voltage at the LDO is 5.5 V.

10.2 Typical Applications

10.2.1 Solution for Maximum Output Power

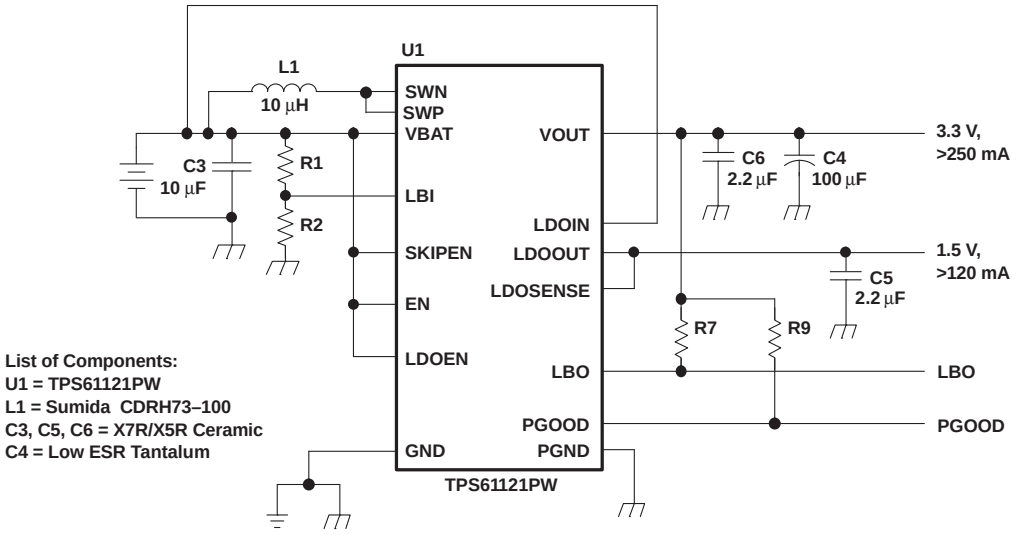


Figure 17. Solution for Maximum Output Power

10.2.1.1 Design Requirements

For this design example, use the parameters listed in Table 3.

Table 3. TPS6112x 5 V Output Design Parameters

DESIGN PARAMETERS	EXAMPLE VALUES
Input voltage range	1.8 V to 3.3 V
Output voltage boost	3.3 V
Output voltage LDO	1.5 V
Output voltage ripple	±3% V_O
Transient response	±10% V_O
Input voltage ripple	±200 mV

10.2.1.2 Detailed Design Procedure

The TPS6112x DC-DC converters are intended for systems powered by a dual or triple cell NiCd or NiMH battery with a typical terminal voltage between 1.8 V and 5.5 V. They can also be used in systems powered by one-cell Li-Ion with a typical stack voltage between 2.5 V and 4.2 V. Additionally, two or three primary and secondary alkaline battery cells can be the power source in systems where the TPS6112x is used.

10.2.1.2.1 Programming the Output Voltage

10.2.1.2.1.1 DC-DC Converter

The output voltage of the TPS61120 DC-DC converter section can be adjusted with an external resistor divider. The typical value of the voltage on the FB pin is 500 mV. The maximum allowed value for the output voltage is 5.5 V. The current through the resistive divider should be about 100 times greater than the current into the FB pin. The typical current into the FB pin is 0.01 µA and the voltage across R6 is typically 500 mV. Based on those two values, the recommended value for R6 should be lower than 500 kΩ, in order to set the divider current at 1 µA or higher. Because of internal compensation circuitry the value for this resistor should be in the range of 200 kΩ. From that, the value of resistor R3, depending on the needed output voltage (V_O), can be calculated using Equation 1:

$$R3 = R6 \times \left(\frac{V_O}{V_{FB}} - 1\right) = 180\ k\Omega \times \left(\frac{V_O}{500\ mV} - 1\right) \quad (1)$$

If as an example, an output voltage of 3.3 V is needed, a 1-MΩ resistor should be chosen for R3. If for any reason the value for R6 is chosen significantly lower than 200 kΩ additional capacitance in parallel to R3 is recommended. The required capacitance value can be easily calculated using Equation 2.

$$C_{parR3} = 20\ pF \times \left(\frac{200\ k\Omega}{R6} - 1\right) \quad (2)$$

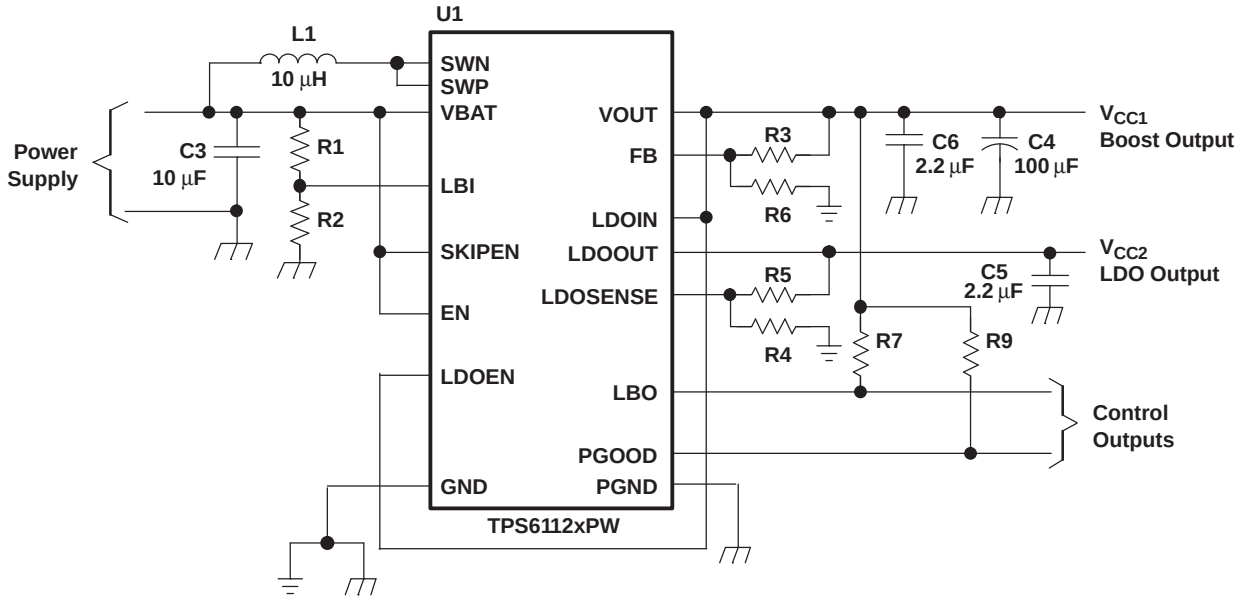


Figure 18. Typical Application Circuit for Adjustable Output Voltage Option

10.2.1.2.1.2 LDO

Programming the output voltage at the LDO follows almost the same rules as in the DC-DC converter section. The maximum programmable output voltage at the LDO is 5.5 V. Since reference and internal feedback circuitry are similar, as they are at the boost converter section, R4 also should be in the 200-kΩ range. The calculation of the value of R5 can be done using the following Equation 3:

$$R5 = R4 \times \left(\frac{V_O}{V_{FB}} - 1\right) = 180\ k\Omega \times \left(\frac{V_O}{500\ mV} - 1\right) \quad (3)$$

If as an example, an output voltage of 1.5 V is needed, a 360 kΩ-resistor should be chosen for R5.

10.2.1.2.2 Programming the LBI/LBO Threshold Voltage

The current through the resistive divider should be about 100 times greater than the current into the LBI pin. The typical current into the LBI pin is 0.01 µA, and the voltage across R2 is equal to the LBI voltage threshold that is generated on-chip, which has a value of 500 mV. The recommended value for R2is therefore in the range of 500 kΩ. From that, the value of resistor R1, depending on the desired minimum battery voltage $V_{BAT,}$ can be calculated using Equation 4.

$$R1 = R2 \times \left(\frac{V_{BAT}}{V_{LBI-threshold}} - 1\right) = 390\ k\Omega \times \left(\frac{V_{BAT}}{500\ mV} - 1\right) \quad (4)$$

The output of the low battery supervisor is a simple open-drain output that goes active low if the dedicated battery voltage drops below the programmed threshold voltage on LBI. The output requires a pullup resistor with a recommended value of 1 MΩ. The maximum voltage which is used to pull up the LBO outputs should not exceed the output voltage of the DC-DC converter. If not used, the LBO pin can be left floating or tied to GND.

10.2.1.2.3 Inductor Selection

A boost converter normally requires two main passive components for storing energy during the conversion. A boost inductor and a storage capacitor at the output are required. To select the boost inductor, it is recommended to keep the possible peak inductor current below the current limit threshold of the power switch in the chosen configuration. For example, the current limit threshold of the TPS6112x's switch is 1600 mA at an output voltage of 3.3 V. The highest peak current through the inductor and the switch depends on the output load, the input (V_{BAT}), and the output voltage (V_{OUT}). Estimation of the maximum average inductor current can be done using Equation 5:

$$I_L = I_{OUT} \times \frac{V_{OUT}}{V_{BAT} \times 0.8} \quad (5)$$

For example, for an output current of 250 mA at 3.3 V, at least 575 mA of current flows through the inductor at a minimum input voltage of 1.8 V.

The second parameter for choosing the inductor is the desired current ripple in the inductor. Normally, it is advisable to work with a ripple in the range of 20% of the average inductor current. A smaller ripple reduces the magnetic hysteresis losses in the inductor, as well as output voltage ripple and EMI. But in the same way, regulation time at load changes rises. In addition, a larger inductor increases the total system costs. With those parameters, it is possible to calculate the value for the inductor by using Equation 6:

$$L = \frac{V_{BAT} \times \left(V_{OUT} - V_{BAT}\right)}{\Delta I_L \times f \times V_{OUT}} \quad (6)$$

Parameter *f* is the switching frequency and ΔI_L is the ripple current in the inductor, that is, 20% × I_L. In this example, the desired inductor value is in the range of 14 µH. In typical applications a 10 µH inductor is recommended. The minimum possible inductor value is 4.7 µH. With the calculated inductance value and current, it is possible to choose a suitable inductor. Care must be taken that load transients and losses in the circuit can lead to higher currents as estimated in Equation 5. Also, the losses in the inductor caused by magnetic hysteresis losses and copper losses are a major parameter for total circuit efficiency.

The following inductor series from different suppliers have been used with the TPS6112x converters:

Table 4. List of Inductors

VENDOR	RECOMMENDED INDUCTOR SERIES
Sumida	CDRH5D18
	CDRH6D28
Wurth Electronik	7447789___
	7447779___
Coiltronics	DR73
	DR74
TDK	SLF 7032
EPCOS	B82462G

10.2.1.2.4 Capacitor Selection

10.2.1.2.4.1 Input Capacitor

An input capacitor with a value of at least a 10 µF is recommended to improve transient behavior of the regulator and EMI behavior of the total power supply circuit. A ceramic capacitor or a tantalum capacitor with a 100-nF ceramic capacitor in parallel, placed close to the IC, is recommended.

10.2.1.2.4.2 Output Capacitor DC-DC Converter

The major parameter necessary to define the output capacitor is the maximum allowed output voltage ripple of the converter. This ripple is determined by two parameters of the capacitor, the capacitance and the ESR. Calclating the minimum capacitance required to define the ripple is possible, supposing that the ESR is zero, by using Equation 7:

$$C_{min} = \frac{I_{OUT} \times \left(V_{OUT} - V_{BAT}\right)}{f \times \Delta V \times V_{OUT}} \quad (7)$$

Parameter f is the switching frequency and ΔV is the maximum allowed ripple.

With a chosen ripple voltage of 10 mV, a minimum capacitance of 22 µF is needed. The total ripple is larger due to the ESR of the output capacitor. This additional component of the ripple can be calculated using Equation 8:

$$\Delta V_{ESR} = I_{OUT} \times R_{ESR} \quad (8)$$

An additional ripple of 20 mV is the result of using a tantalum capacitor with a low ESR of 80 mΩ. The total ripple is the sum of the ripple caused by the capacitance and the ripple caused by the ESR of the capacitor. In this example, the total ripple is 30 mV. Additional ripple is caused by load transients. This means that the output capacitance needs to be larger than calculated above to meet the total ripple requirements. The output capacitor has to completely supply the load during the charging phase of the inductor. A reasonable value of the output capacitance depends on the speed of the load transients and the load current during the load change. In typical applications a 100 µF capacitance is recommended. For economical reasons this usually is a tantalum capacitor. Because of this the control loop has been optimized for using output capacitors with an ESR of above 30 mΩ. The minimum value for the output capacitor is 22 µF.

10.2.1.2.4.2.1 Small Signal Stability

When using output capacitors with lower ESR, like ceramics, it is recommended to use the adjustable voltage version. The missing ESR can be easily compensated there in the feedback divider. Typically a capacitor in the range of 10 pF in parallel with R3 helps to obtain small signal stability, with the lowest ESR output capacitors. For more detailed analysis the small signal transfer function of the error amplifier and regulator, which is given in Equation 9, can be used.

$$A_{REG} = \frac{d}{V_{FB}} = \frac{10 \times (R3 + R6)}{R6 \times (1 + i \times \omega \times 1.6\,\mu s)} \quad (9)$$

10.2.1.2.4.3 Output Capacitor LDO

To ensure stable output regulation, it is required to use an output capacitor at the LDO output. Ceramic capacitors in the range from 1 µF up to 4.7 µF is recommended. Using the standard ESR tantalum is recommended at capacitance of 4.7 µF and above. There is no maximum capacitance value.

10.2.1.3 Application Curves

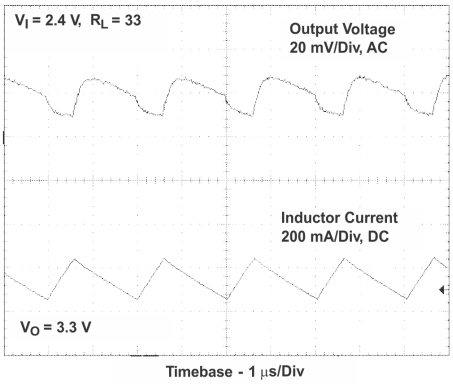


Figure 19. TPS61121 Boost Converter Output Voltage in Continuous Mode

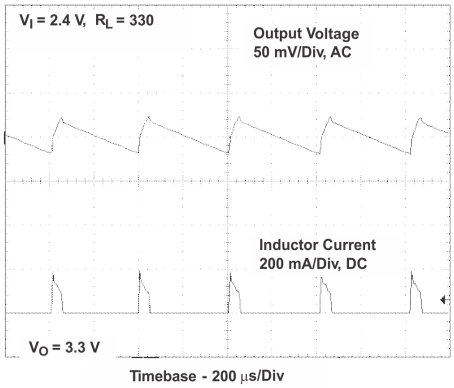


Figure 20. TPS61121 Boost Converter Output Voltage in Power Save Mode

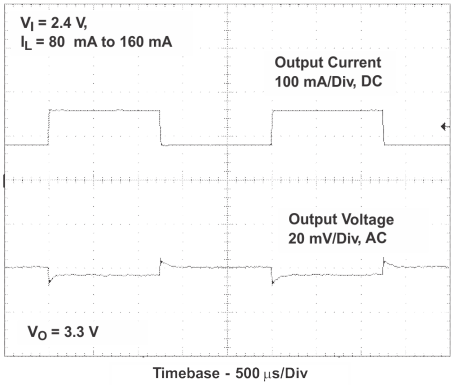


Figure 21. TPS61121 Boost Converter Load Transient Response

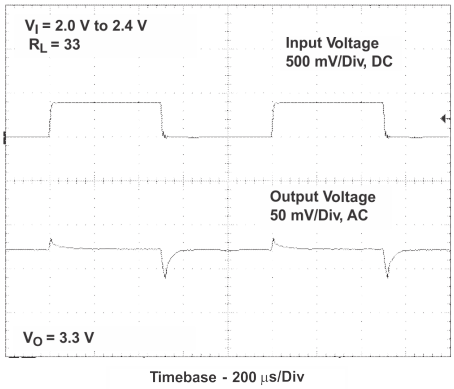


Figure 22. TPS61121 Boost Converter Line Transient Response

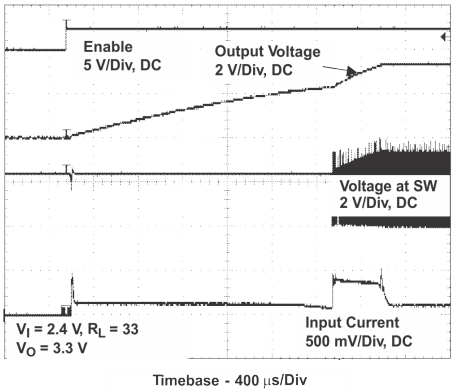


Figure 23. TPS61121 Boost Converter Start-up After Enable

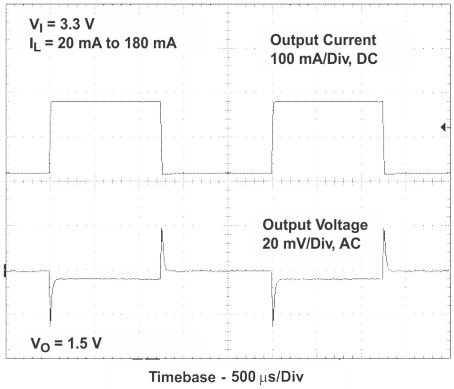


Figure 24. TPS61121 LDO Load Transient Response

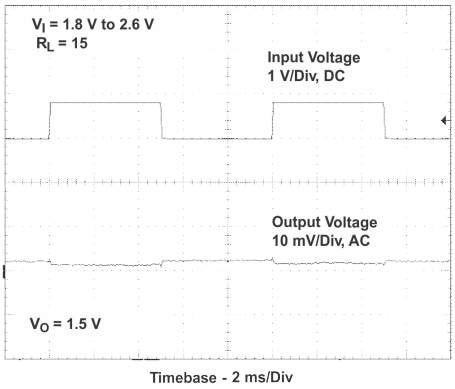


Figure 25. TPS61121 LDO Line Transient Response

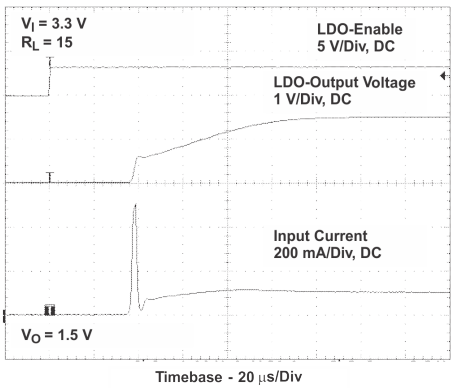


Figure 26. TPS61121 LDO Start-up After Enable

10.2.2 Low Profile Solution, Maximum Height 1.8 mm

The TPS6112x boost converter with LDO features two independent output voltages. An efficient synchronous boost converter provides a 3.3-V V_{OUT1} with output currents up to 500 mA. A 200-mA LDO regulator generates a 1.5-V V_{OUT2}. The two outputs can be used independently from each other. TPS6112x supports the lower profile of inductor with maximum height 1.8 mm.

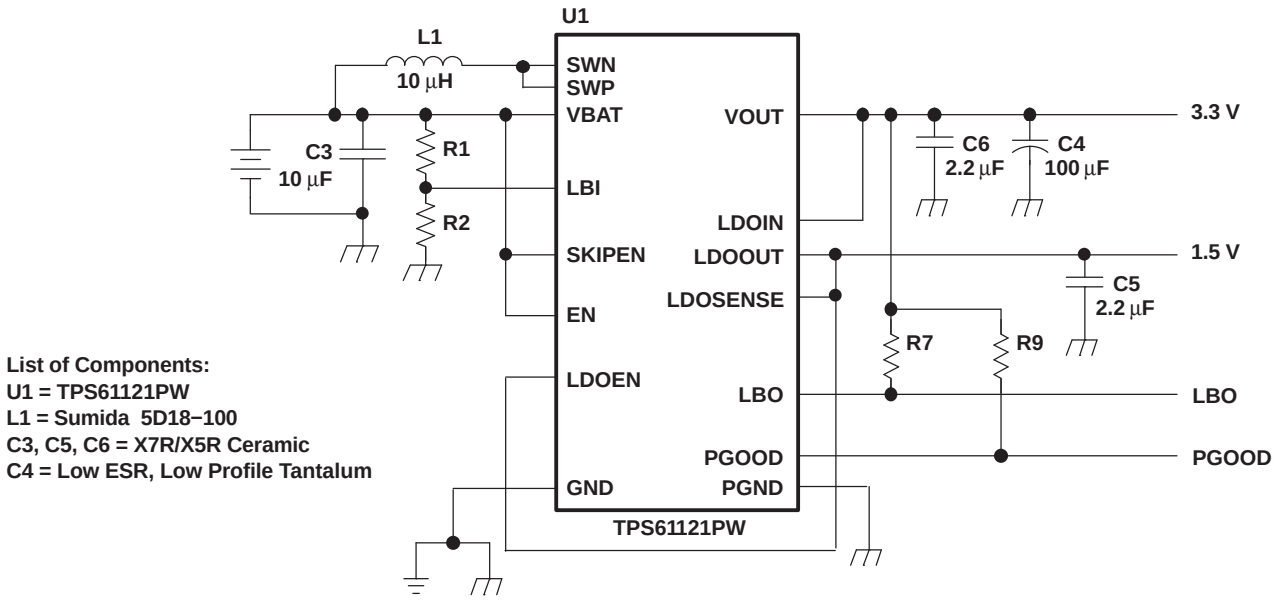


Figure 27. Low Profile Solution, Maximum Height 1.8 mm

10.2.3 Dual Power Supply With Auxiliary Positive Output Voltage

The TPS6112x boost converter with LDO features multiple output voltages. An efficient synchronous boost converter provides Vout1 3.3 V with output currents up to 500mA. A 200-mA LDO regulator generates Vout2 1.5 V. Another rail provides 6 V with discrete charge pump added.

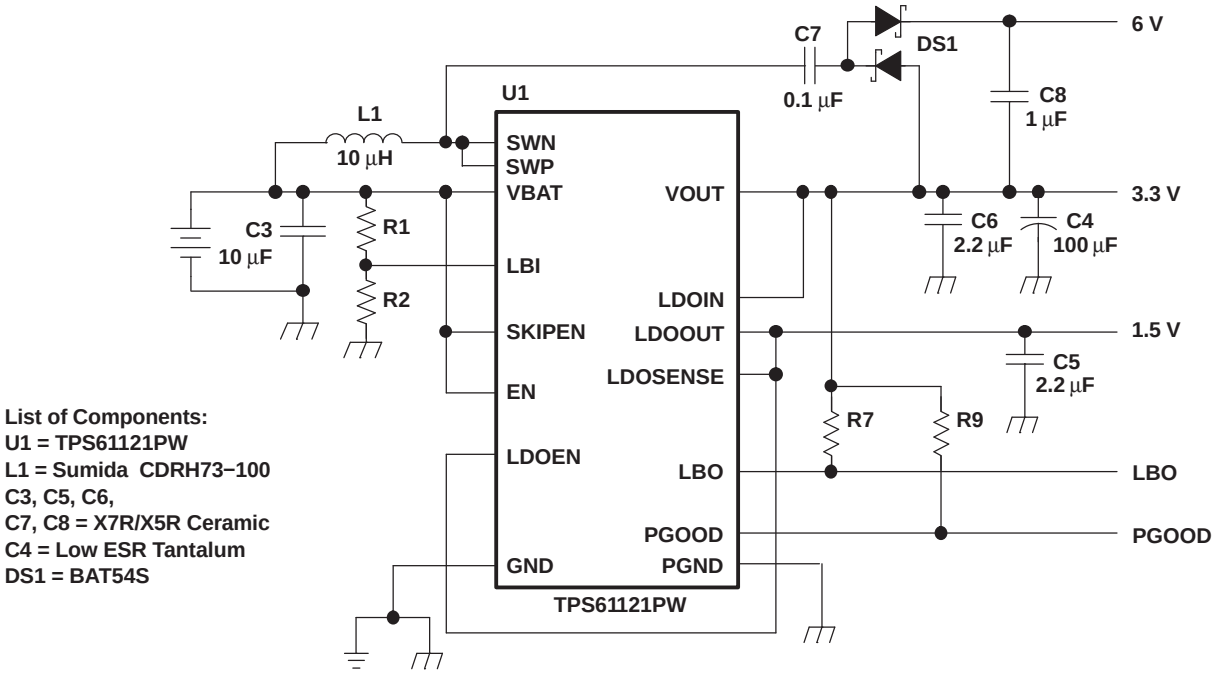


Figure 28. Dual Power Supply With Auxiliary Positive Output Voltage

10.2.4 Dual Power Supply With Auxiliary Negative Output Voltage

The TPS6112x boost converter with LDO features multiple output voltages. An efficient synchronous boost converter provides Vout1 3.3 V with output currents up to 500 mA. A 200-mA LDO regulator generates Vout2 1.5 V. Another rail provides –3 V with discrete charge pump added.

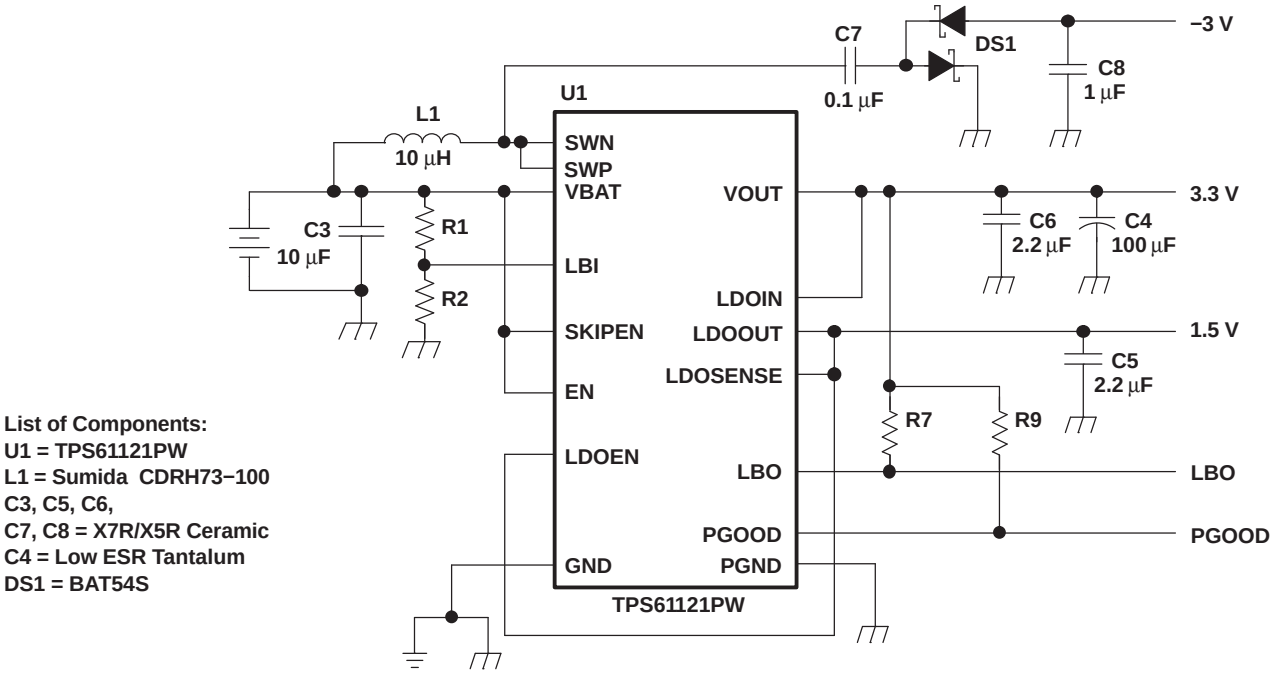


Figure 29. Dual Power Supply With Auxiliary Negative Output Voltage

10.2.5 Single Output Using LDO as Filter

The TPS6112x could provide a linear output of 3.3 V with the input from the output of the boost converter, and deliver 200-mA output current.

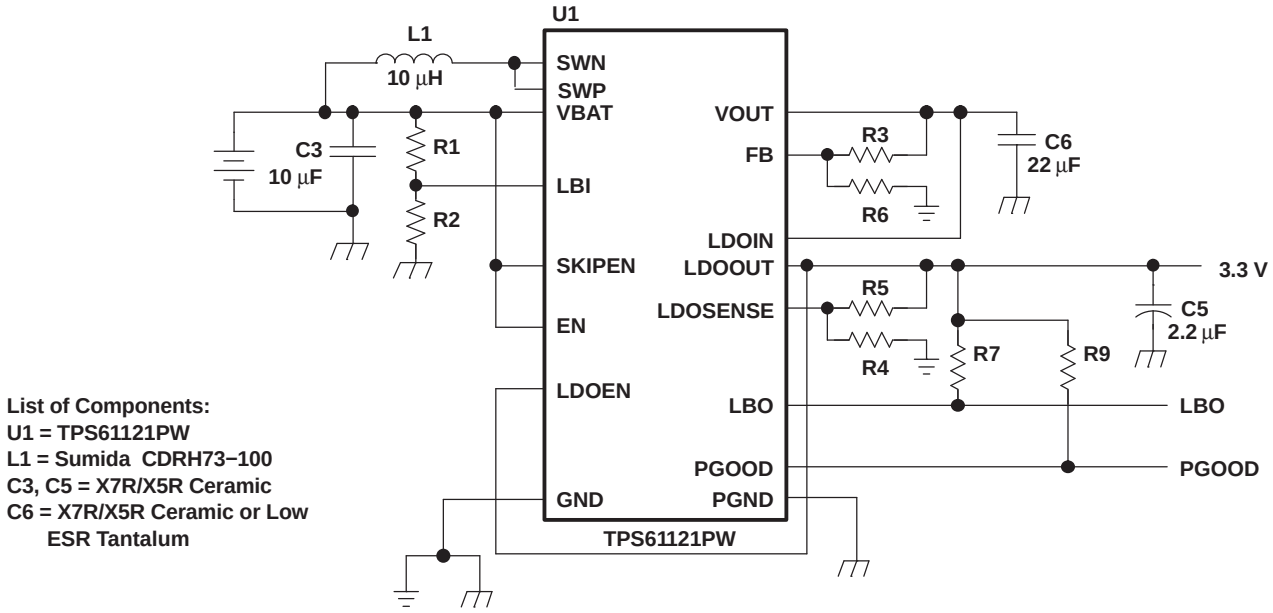


Figure 30. Single Output Using LDO as Filter

10.2.6 Dual Input Power Supply Solution

The TPS6112x boost converter can support dual input power supply, one input for boost converter to generate a 3.3 Vout with 500-mA output current, while the other input for LDO to generate the second 3.3 Vout with 200-mA output current.

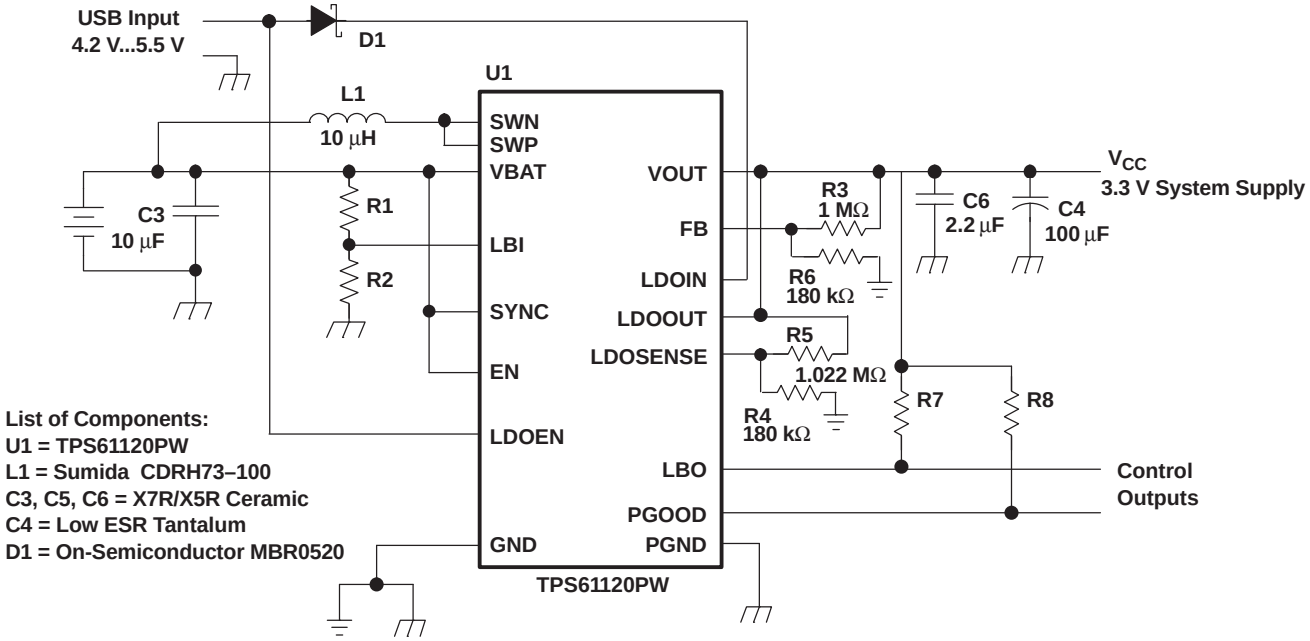


Figure 31. Dual Input Power Supply Solution

11 Power Supply Recommendations

The device is designed to operate from an input voltage supply range between 1.8 V and 5.5 V. This input supply must be well regulated. If the input supply is located more than a few inches from the converter, additional bulk capacitance may be required in addition to the ceramic bypass capacitors. An electrolytic or tantalum capacitor with a value of 47 µF is a typical choice.

12 Layout

12.1 Layout Guidelines

As for all switching power supplies, the layout is an important step in the design, especially at high peak currents and high switching frequencies. If the layout is not carefully done, the regulator could show stability problems as well as EMI problems. Therefore, use wide and short traces for the main current path and for the power ground tracks. The input capacitor, output capacitor, and the inductor should be placed as close as possible to the IC. Use a common ground node for power ground and a different one for control ground to minimize the effects of ground noise. Connect these ground nodes at any place close to one of the ground pins of the IC.

The feedback divider should be placed as close as possible to the control ground pin of the device. To lay out the control ground, using short traces is also recommended, separated from the power ground traces. This avoids ground shift problems, which can occur due to superimposition of power ground current and control ground current.

12.2 Layout Example

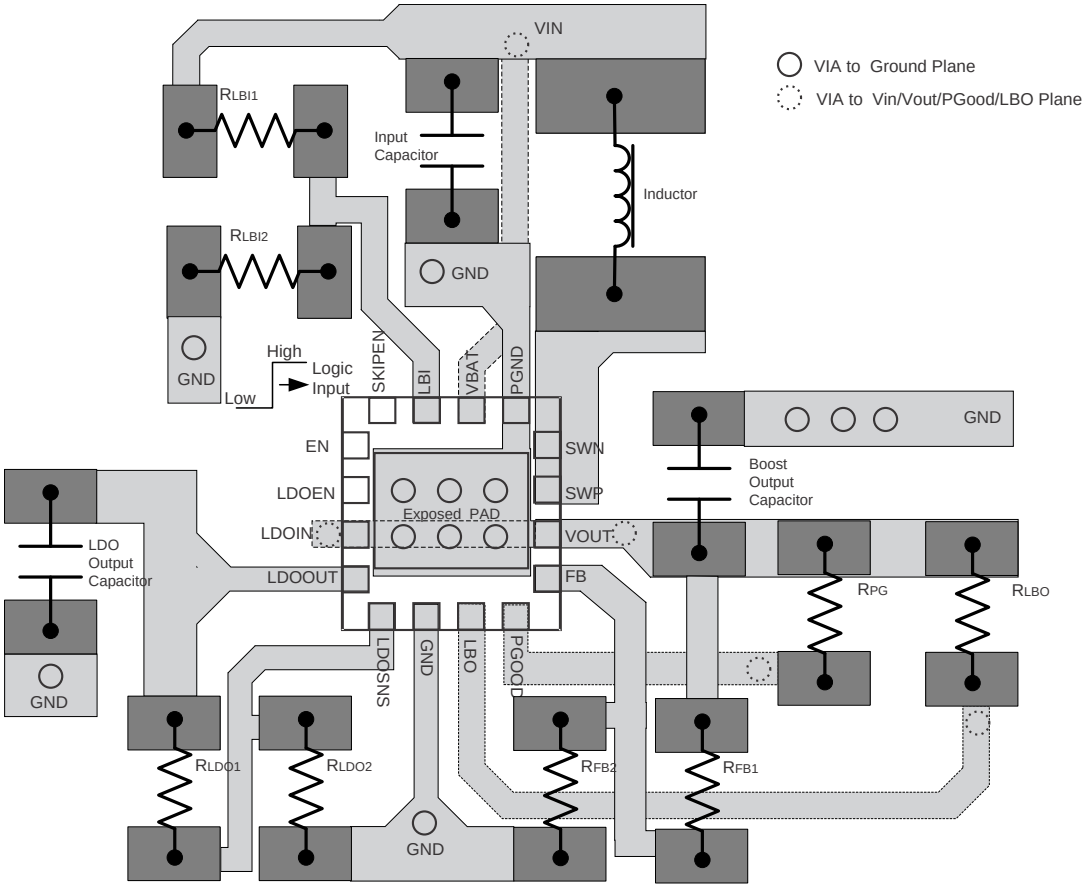


Figure 32. Layout Example

12.3 Thermal Considerations

Implementation of integrated circuits in low-profile and fine-pitch surface-mount packages typically requires special attention to power dissipation. Many system-dependent issues such as thermal coupling, airflow, added heat sinks and convection surfaces, and the presence of other heat-generating components affect the power-dissipation limits of a given component.

Three basic approaches for enhancing thermal performance are listed below.

- Improving the power dissipation capability of the PCB design
- Improving the thermal coupling of the component to the PCB
- Introducing airflow in the system

The maximum junction temperature (T_J) of the TPS6112x devices is 150 °C. The thermal resistance of the 16-pin TSSOP package (PW) is $R_{\Theta JA}$ = 100.5°C/W. The 16-pin QFN (RSA) has a thermal resistance of $R_{\Theta JA}$ = 33.9°C/W, if the thermal pad is soldered and the board layout is optimized. Specified regulator operation is assured to a maximum ambient temperature T_A of 85°C. Therefore, the maximum power dissipation is about 647 mW for the TSSOP (PW) package and 1917 mW for the QFN (RSA) package; see Equation 10. More power can be dissipated if the maximum ambient temperature of the application is lower.

$$P_{D(MAX)} = \frac{T_{J(MAX)} - T_A}{R_{\theta JA}} \tag{10}$$

If designing for a lower junction temperature of 125°C, which is recommended, maximum heat dissipation is lower. Using the above Equation 10 results in 1180 mW power dissipation for the RSA package and 400 mW for the PW package.

13 Device and Documentation Support

13.1 Device Support

13.1.1 Third-Party Products Disclaimer

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13.2 Community Resources

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

TI E2E™ Online Community ***TI's Engineer-to-Engineer (E2E) Community.*** Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

Design Support ***TI's Design Support*** Quickly find helpful E2E forums along with design support tools and contact information for technical support.

13.3 Trademarks

E2E is a trademark of Texas Instruments.
All other trademarks are the property of their respective owners.

13.4 Electrostatic Discharge Caution

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

13.5 Glossary

SLYZ022 — *TI Glossary*.

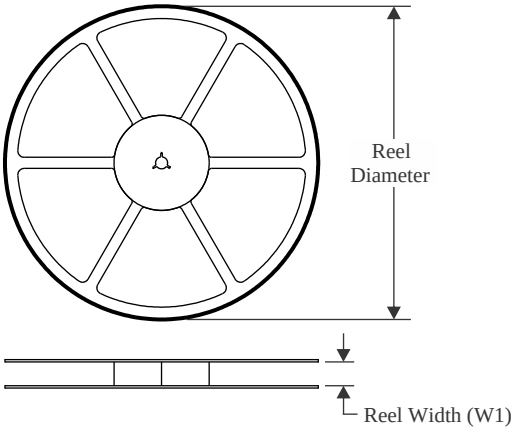
This glossary lists and explains terms, acronyms, and definitions.

14 Mechanical, Packaging, and Orderable Information

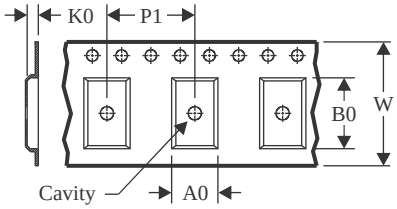
The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

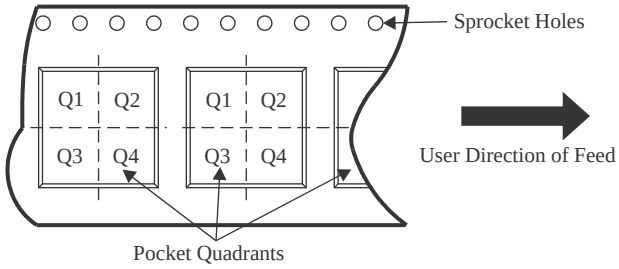


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

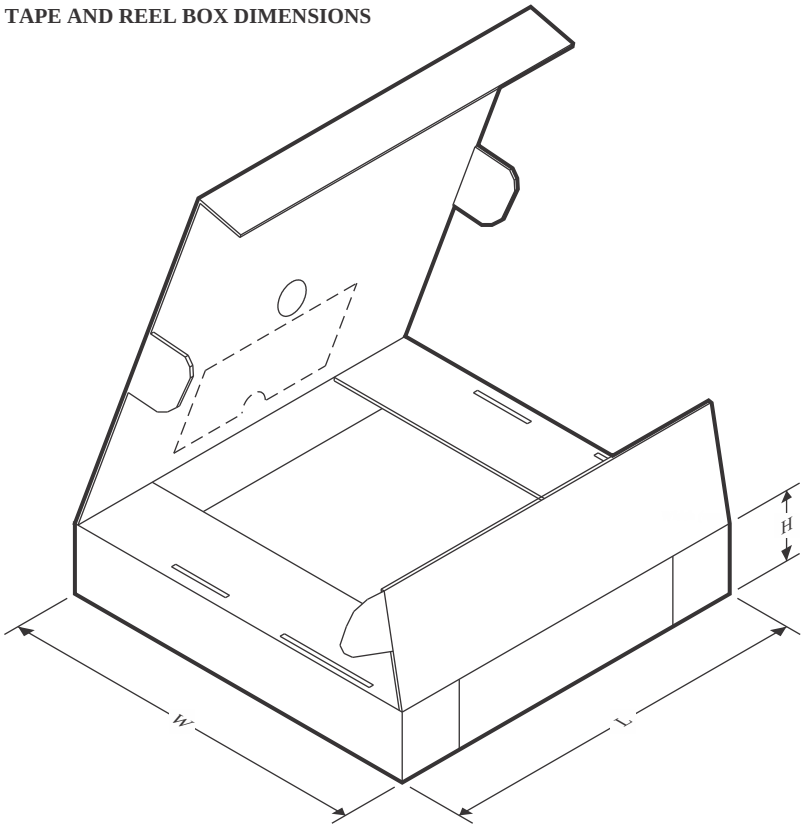
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPS61120PWR	TSSOP	PW	16	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
TPS61120RSAR	QFN	RSA	16	3000	330.0	12.4	4.3	4.3	1.5	8.0	12.0	Q2

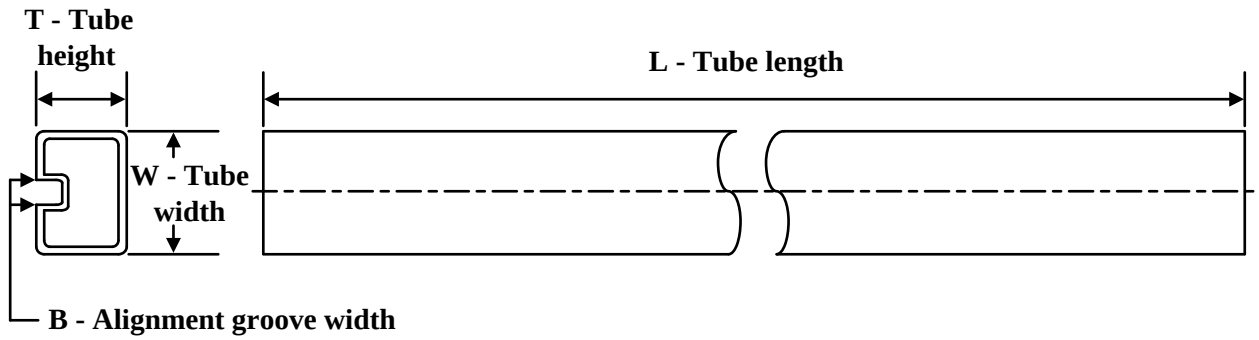
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPS61120PWR	TSSOP	PW	16	2000	350.0	350.0	43.0
TPS61120RSAR	QFN	RSA	16	3000	350.0	350.0	43.0

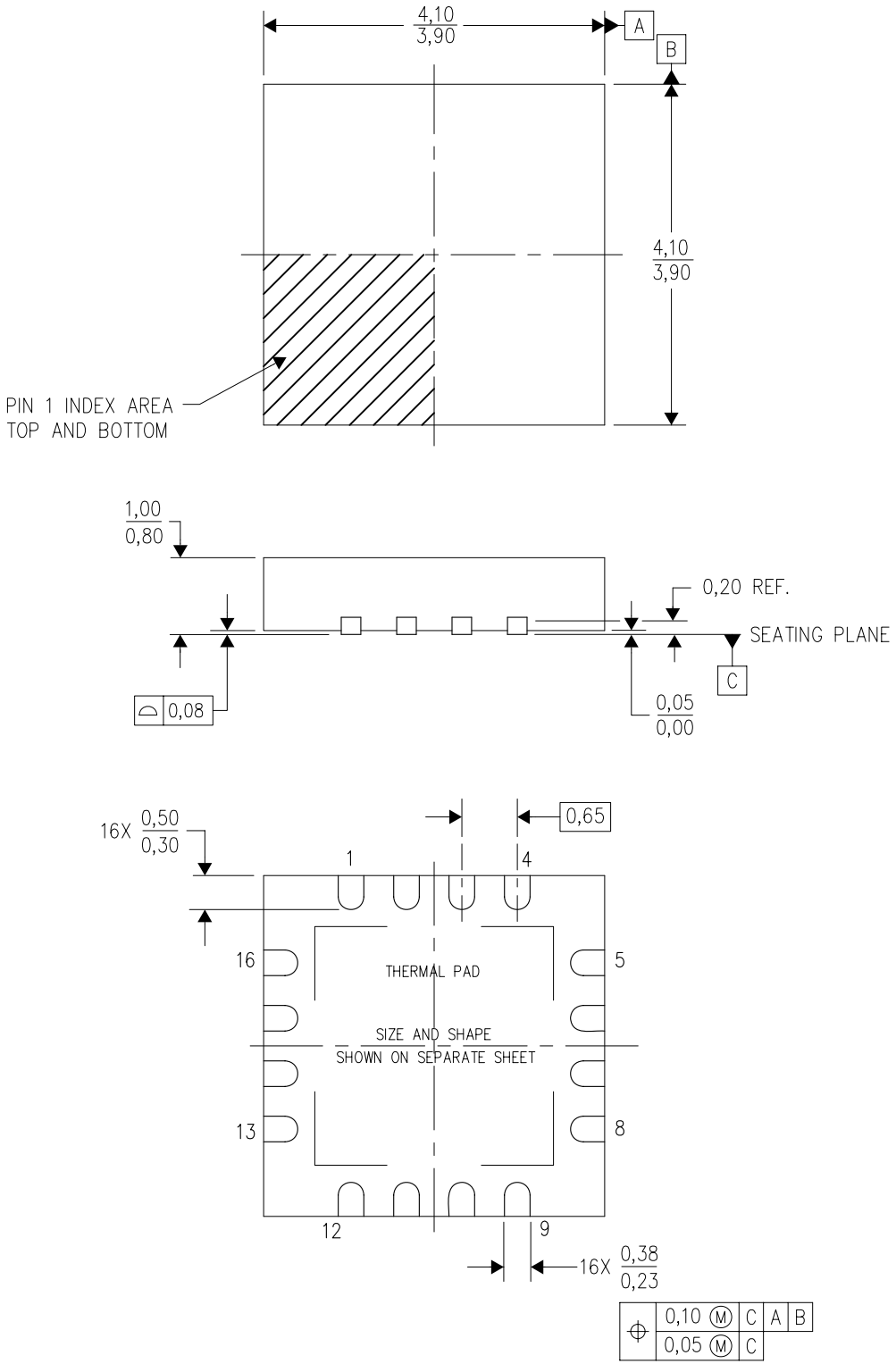
TUBE



*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (µm)	B (mm)
TPS61120PW	PW	TSSOP	16	90	530	10.2	3600	3.5
TPS61120PWG4	PW	TSSOP	16	90	530	10.2	3600	3.5
TPS61121PW	PW	TSSOP	16	90	530	10.2	3600	3.5
TPS61122PW	PW	TSSOP	16	90	530	10.2	3600	3.5

RSA (S–PVQFN–N16) PLASTIC QUAD FLATPACK NO–LEAD



NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. Quad Flatpack, No–leads (QFN) package configuration.
D. The package thermal pad must be soldered to the board for thermal and mechanical performance.
E. See the additional figure in the Product Data Sheet for details regarding the exposed thermal pad features and dimensions.
F. Falls within JEDEC MO–220.

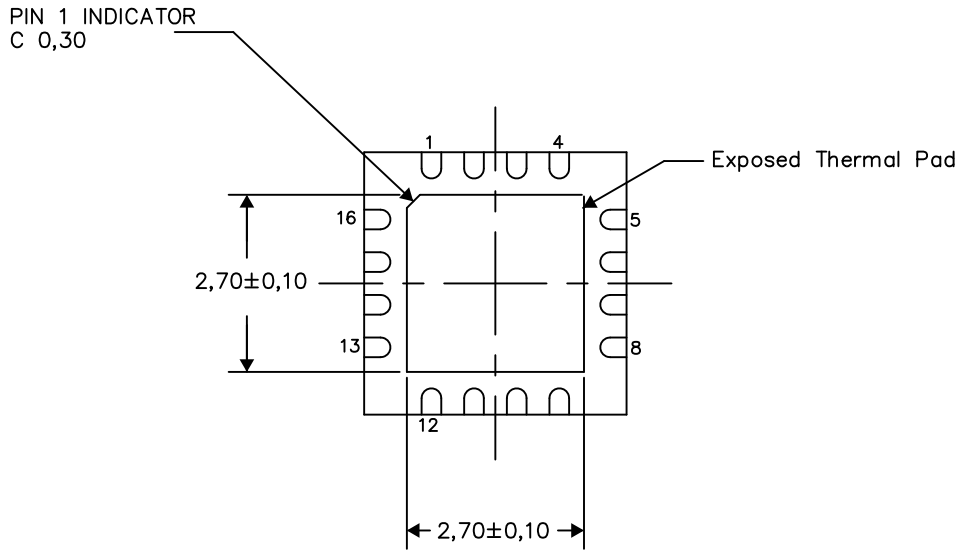
RSA (S–PVQFN–N16) PLASTIC QUAD FLATPACK NO–LEAD

THERMAL INFORMATION

This package incorporates an exposed thermal pad that is designed to be attached directly to an external heatsink. The thermal pad must be soldered directly to the printed circuit board (PCB). After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For information on the Quad Flatpack No–Lead (QFN) package and its advantages, refer to Application Report, QFN/SON PCB Attachment, Texas Instruments Literature No. SLUA271. This document is available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.



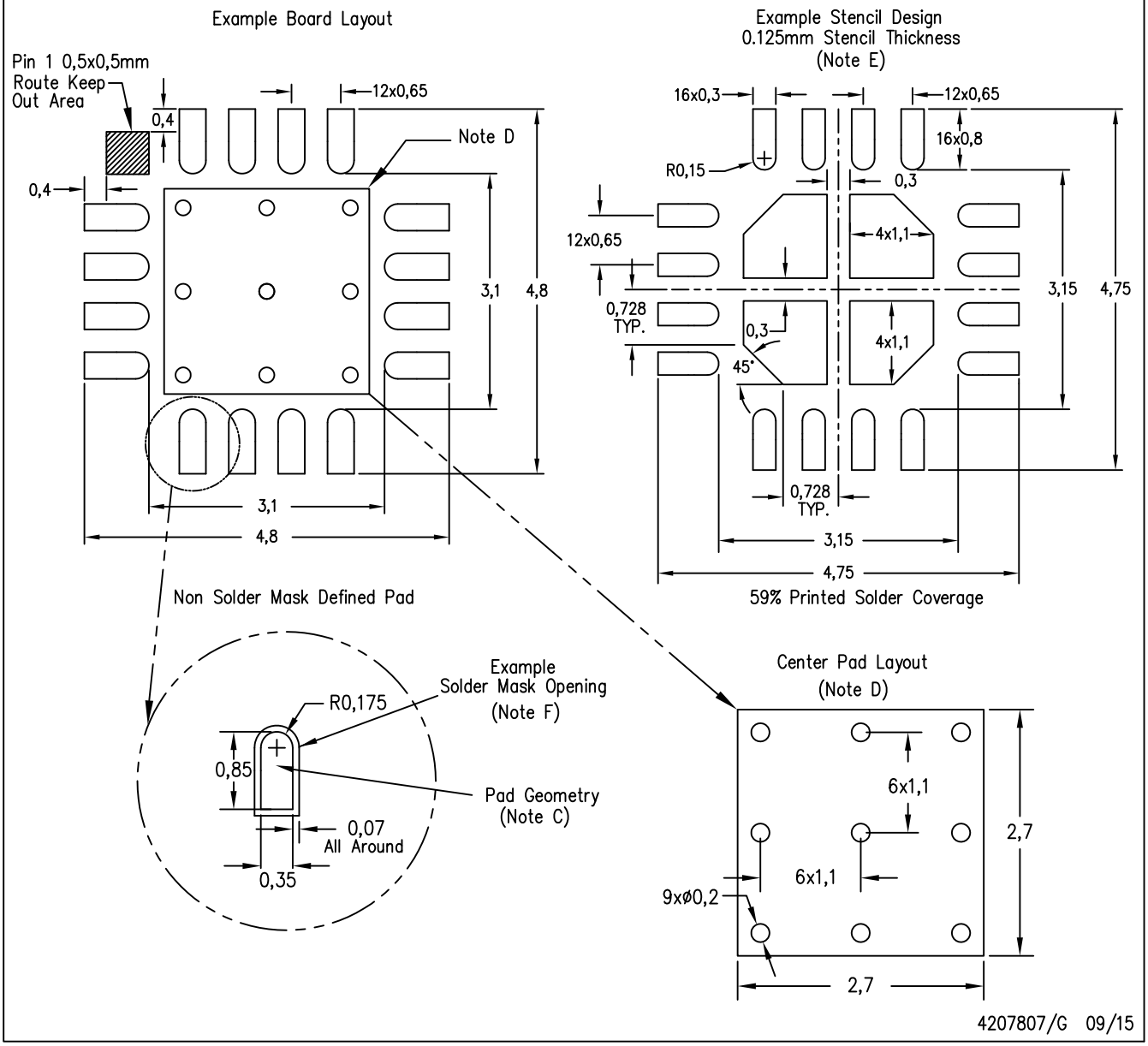
Bottom View

Exposed Thermal Pad Dimensions

4206364–2/0 09/15

NOTES:
A. All linear dimensions are in millimeters

RSA (S–PVQFN–N16) PLASTIC QUAD FLATPACK NO–LEAD



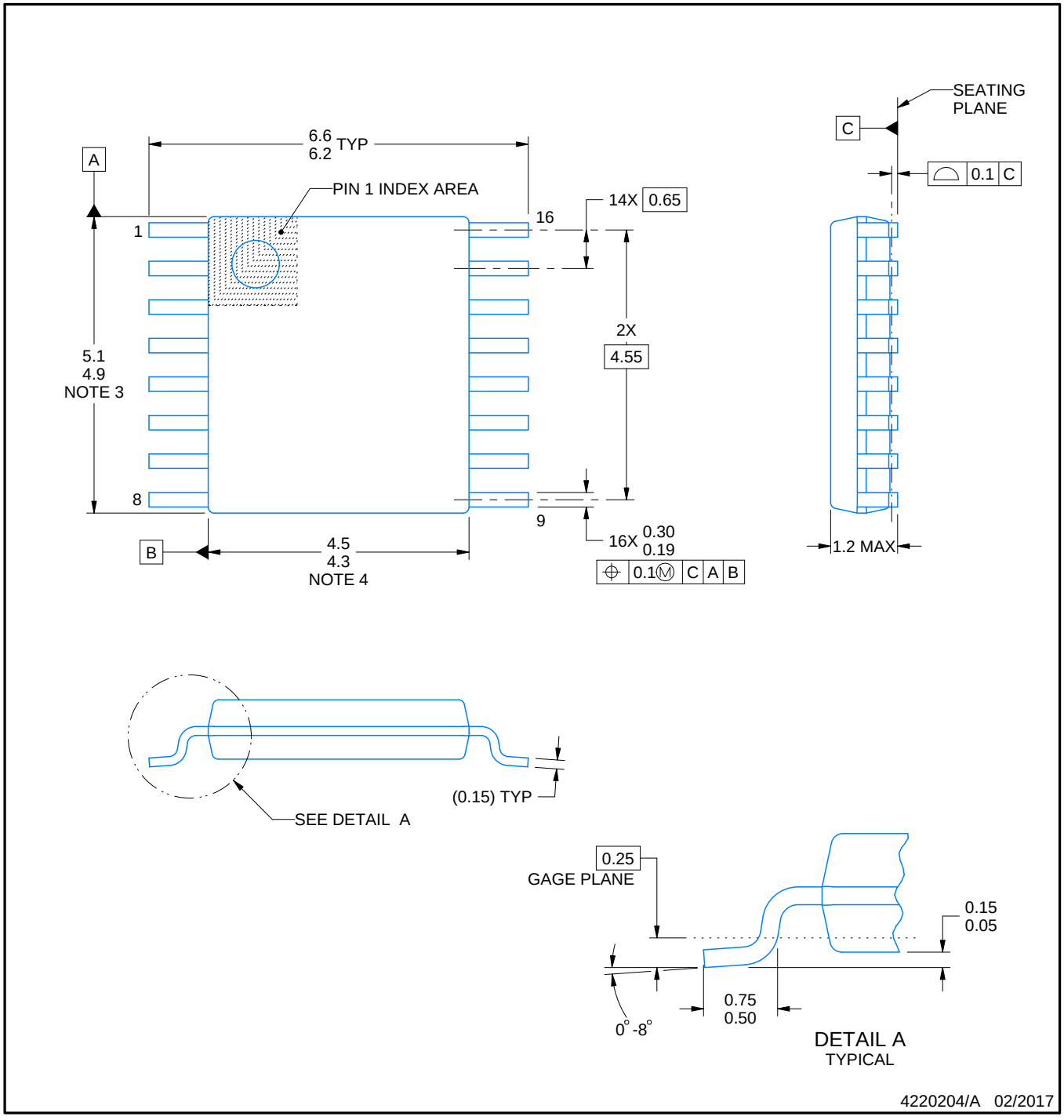
NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. This package is designed to be soldered to a thermal pad on the board. Refer to Application Note, QFN Packages, Texas Instruments Literature No. SLUA271, and also the Product Data Sheets for specific thermal information, via requirements, and recommended board layout. These documents are available at www.ti.com <http://www.ti.com>.
E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC 7525 for stencil design considerations.
F. Customers should contact their board fabrication site for solder mask tolerances.

PACKAGE OUTLINE

PW0016A

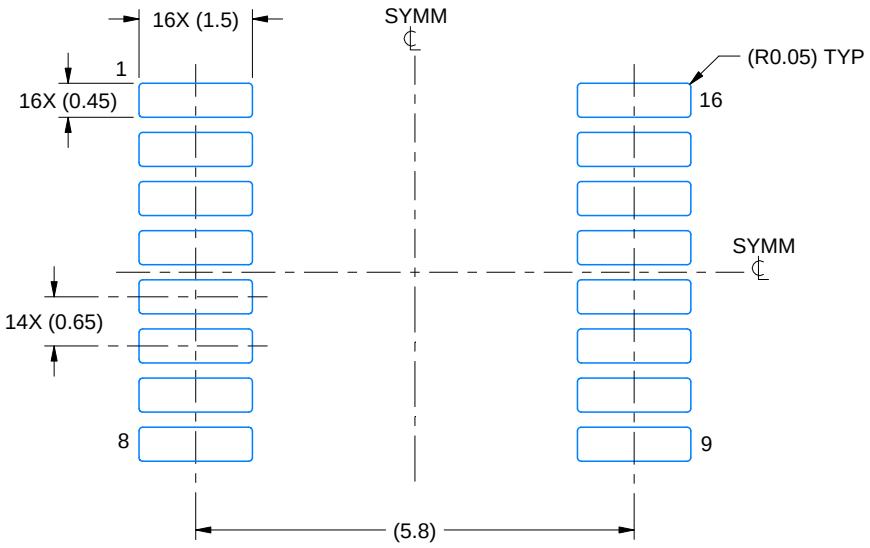
TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE

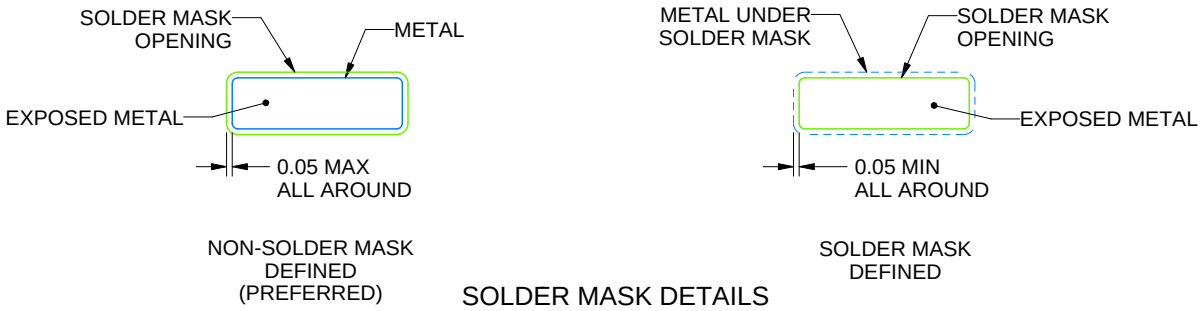


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-153.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 10X



SOLDER MASK DETAILS

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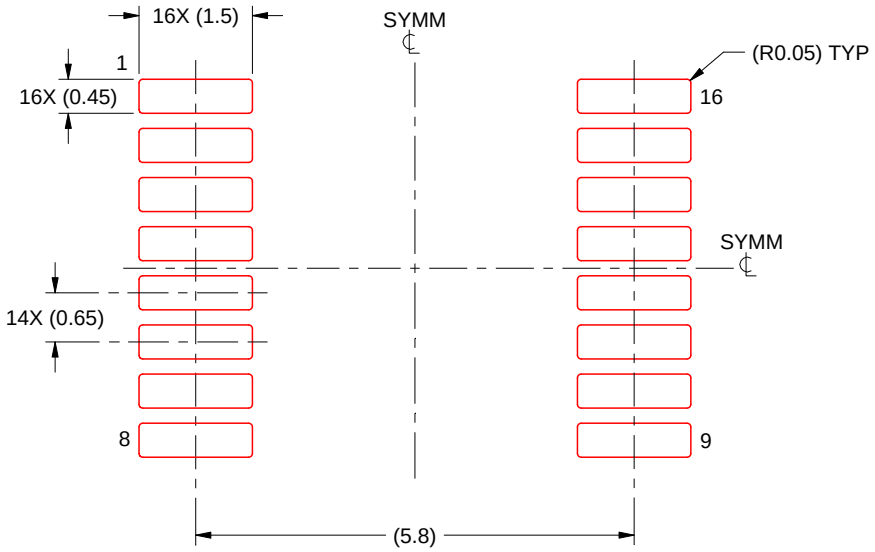
NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 10X

4220204/A 02/2017

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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