REVISIONS			
LTR	DESCRIPTION	DATE (YR-MO-DA)	APPROVED
A	Update vendor's part number. Change to military drawing format. Editorial changes throughout.	1987 JULY 7	M.A. Frye
B	Made technical changes to table I. Added device types 07, 08, and 09 for vendor CAGE 34335. Changes to figures 4, 5, and 6. Changes to 4.3.2 and 6.4. Corrected CAGE code on front page. Editorial changes throughout.	1989 JUNE 13	M.A. Frye

CURRENT CAGE CODE 67268

REV																									
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REV STATUS OF SHEETS	REV	B	B	B	B	B	B	B	B	B	B	B	B	B	B	B	B								
	SHEET	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15									

PMIC N/A

STANDARDIZED MILITARY DRAWING

THIS DRAWING IS AVAILABLE FOR USE BY ALL DEPARTMENTS AND AGENCIES OF THE DEPARTMENT OF DEFENSE

AMSC N/A

PREPARED BY: Steve Duncan

CHECKED BY: Ray Monnin

APPROVED BY: M.A. Frye

DRAWING APPROVAL DATE: 25 MARCH 1986

REVISION LEVEL: B

DEFENSE ELECTRONICS SUPPLY CENTER
DAYTON, OHIO 45444

MICROCIRCUITS, MEMORY, 64-BIT SCHOTTKY BIPOLAR RAM, MONOLITHIC SILICON

SIZE	CAGE CODE	
A	14933	86051

SHEET 1 OF 15

DESC FORM 193-1
SEP 87

* U.S. GOVERNMENT PRINTING OFFICE: 1987 — 748-129/60912

5962-E1322

1. SCOPE

1.1 Scope. This drawing describes device requirements for class B microcircuits in accordance with 1.2.1 of MIL-STD-883, "Provisions for the use of MIL-STD-883 in conjunction with compliant non-JAN devices".

1.2 Part number. The complete part number shall be as shown in the following example:

86051	01	E	X
Drawing number	Device type (1.2.1)	Case outline (1.2.2)	Lead finish per MIL-M-38510

1.2.1 Device types. The device types shall identify the circuit function as follows:

Device type	Generic number	Circuit	Access time
01	27S02	64-Bit Schottky bipolar RAM, open collector outputs	50
02	27S02A	64-Bit Schottky bipolar RAM, open collector outputs	30
03	27LS02	64-Bit Low power schottky bipolar RAM, open collector outputs	65
04	27S03	64-Bit Schottky bipolar RAM, three-state outputs	50
05	27S03A	64-Bit Schottky bipolar RAM, three-state outputs	30
06	27LS03	64-Bit Low power schottky bipolar RAM, three-state outputs	65
07	27S02-20	64-Bit Schottky bipolar RAM, open collector outputs	20
08	27S03-20	64-Bit Schottky bipolar RAM, three-state outputs	20
09	27LS03-30	64-Bit Low power Schottky bipolar RAM, three-state outputs	30

1.2.2 Case outlines. The case outlines shall be as designated in appendix C of MIL-M-38510, and as follows:

Outline letter	Case outline
E	D-2 (16-lead, .840" x .310" x .200"), dual-in-line package
F	F-5 (16-lead, .440" x .285" x .085"), flat package
2	C-2 (20-terminal, .358" x .358" x .100"), square chip carrier package

1.3 Absolute maximum ratings.

Supply voltage range	-0.5 V dc to +7.0 V dc
Input voltage range	-0.5 V dc to +5.5 V dc
Storage temperature range	-65°C to +150°C
Maximum power dissipation (P_D) 1/	1.6 W
Lead temperature (soldering, 10 seconds)	+300°C
Thermal resistance, junction-to-case (θ_{JC}):	
Cases E, F and 2	See MIL-M-38510, appendix C
Junction temperature (T_J)	+175°C
DC input current	-30 mA to +5 mA

1/ Must withstand the added P_D due to short circuit test; e.g., I_{OS}.

1.4 Recommended operating conditions.

Supply voltage range (V_{CC}) - - - - - - - - - - - -	4.5 V dc minimum to 5.5 V dc maximum
Minimum high-level input voltage (V_{IH}) - - - - - -	2.0 V dc
Maximum low-level input voltage (V_{IL})- - - - - - -	0.8 V dc
Case operating temperature range (T_C)- - - - - - -	-55°C to +125°C

2. APPLICABLE DOCUMENTS

2.1 Government specification and standard. Unless otherwise specified, the following specification and standard, of the issue listed in that issue of the Department of Defense Index of Specifications and Standards specified in the solicitation, form a part of this drawing to the extent specified herein.

SPECIFICATION

MILITARY

MIL-M-38510 - Microcircuits, General Specification for.

STANDARD

MILITARY

MIL-STD-883 - Test Methods and Procedures for Microelectronics.

(Copies of the specification and standard required by manufacturers in connection with specific acquisition functions should be obtained from the contracting activity or as directed by the contracting activity.)

2.2 Order of precedence. In the event of a conflict between the text of this drawing and the references cited herein, the text of this drawing shall take precedence.

3. REQUIREMENTS

3.1 Item requirements. The individual item requirements shall be in accordance with 1.2.1 of MIL-STD-883, "Provisions for the use of MIL-STD-883 in conjunction with compliant non-JAN devices" and as specified herein.

3.2 Design, construction, and physical dimensions. The design, construction, and physical dimensions shall be as specified in MIL-M-38510 and herein.

3.2.1 Terminal connections. The terminal connections shall be as specified on figure 1.

3.2.2 Truth table. The truth table shall be as specified on figure 2.

3.2. Logic diagram. The logic diagram shall be as specified on figure 3.

3.2. Case outlines. The case outlines shall be in accordance with 1.2.2 herein.

3.3 Electrical performance characteristics. Unless otherwise specified, the electrical performance characteristics are as specified in table I and apply over the full case operating temperature range.

3.4 Marking. Marking shall be in accordance with MIL-STD-883 (see 3.1 herein). The part shall be marked with the part number listed in 1.2 herein. In addition, the manufacturer's part number may also be marked as listed in 6.4 herein.

TABLE I. Electrical performance characteristics.

Test	Symbol	Conditions $-55°C \le T_C \le +125°C$ $4.5\ V\ dc \le V_{CC} \le 5.5\ V\ dc$ unless otherwise specified		Group A subgroups	Device type	Limits Min	Limits Max	Unit
Output high voltage	V_{OH}	V_{CC} = min. $V_{IN} = V_{IH}$ or V_{IL}	I_{OH} = -2.0 mA	1,2,3	ALL	2.4		V
Output low voltage	V_{OL}	V_{CC} = min. $V_{IN} = V_{IH}$ or V_{IL}	I_{OL} = 16 mA	1,2,3	01,02, 04,05, 07,08		450	mV
			I_{OL} = 20 mA		01,02, 04,05, 07,08		500	
			I_{OL} = 10 mA		03,06, 09		500	
			I_{OL} = 8 mA		03,06, 09		450	
Input high level voltage	V_{IH}	Guaranteed input logical high voltage for all inputs 1/		1,2,3	All	2.0		V
Input low level voltage	V_{IL}	Guaranteed input logical low voltage for all inputs 1/		1,2,3	All		0.8	V
Input low current	I_{IL}	V_{CC} = max V_{IN} = 0.40 V	$\overline{WE}$, D_0-D_3, A_0-A_3, $\overline{CS}$	1,2,3	All		-250	µA
Input high current	I_{IH}	V_{CC} = max, V_{IN} = 2.7 V		1,2,3	All		10	µA
Output short circuit current	I_{OS}	V_{CC} = max V_{OUT} = 0.0 V 2/		1,2,3	ALL	-20	-90	mA
Power supply current	I_{CC}	All inputs = GND V_{CC} = max		1,2,3	01,02, 04,05, 07,08		105	mA
					03,06 09		38	
Input clamp voltage	V_{CL}	V_{CC} = min, I_{IN} = -18 mA		1,2,3	All		-1.2	V

See footnotes at end of table.

TABLE-I. Electrical performance characteristics - Continued.

Test	Symbol	Conditions $-55°C \le T_C \le +125°C$ 4.5 V dc $\le V_{CC} \le$ 5.5 V dc unless otherwise specified	Group A sub-groups	Device type	Limits		Unit
					Min	Max	
Output leakage current	I_{CEX}	$V_{\overline{CS}} = V_{IH}$ or $V_{\overline{WE}} = V_{IL}$ V_{OUT} = 2.4 V	1,2,3	All		40	µA
		$V_{\overline{CS}} = V_{IH}$ or $V_{\overline{WE}} = V_{IL}$ V_{OUT} = 0.4 V		ALL	-40		
Delay from address to output	$t_{PLH(A)}$ $t_{PHL(A)}$	See figures 4 and 6 3/	9,10,11	01,04		50	ns
				02,05 09		30	
				03,06		65	
				07,08		20	
Delay from chip select (LOW) to active output and correct data	$t_{PZH(\overline{CS})}$ $t_{PZL(\overline{CS})}$	See figures 4 and 6 4/ 5/	9,10,11	01,04		25	ns
				02,05, 07,08, 09		20	
				03,06		35	
Delay from write enable (HIGH) to active output and correct data (write recovery) 6/	$t_{PZH(\overline{WE})}$ $t_{PZL(\overline{WE})}$	See figures 4 and 5 4/ 5/	9,10,11	01,04		40	ns
				02,05		25	
				03,06		35	
				07,08, 09		15	
Setup time address (prior to initiation of write)	$t_{s(A)}$	See figures 4 and 5	9,10,11	All	0		ns
Hold time address (after termination of write)	$t_{h(A)}$	See figures 4 and 5	9,10,11	All	0		ns
Setup time data input (prior to termination of write)	$t_{s(DI)}$	See figures 4 and 5	9,10,11	09	30		ns
				01,02, 04,05	25		
				03,06	55		
				07,08	20		
Hold time data input (after termination of write)	$t_{h(DI)}$	See figures 4 and 5	9,10,11	All	0		ns

See footnotes at end of table.

TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Conditions $-55°C \le T_C \le +125°C$ 4.5 V dc $\le V_{CC} \le$ 5.5 V dc unless otherwise specified	Group A subgroups	Device type	Limits Min	Limits Max	Unit
Min write enable pulse width to insure write	$t_{pw(\overline{WE})}$	See figures 4 and 5	9,10,11	09	30		ns
				01,02,04,05	25		
				03,06	55		
				07,08	20		
Delay from chip select (HIGH) to inactive output (HI-Z)	$t_{PHZ(\overline{CS})}$ $t_{PLZ(\overline{CS})}$	See figures 4 and 6 4/ 5/	9,10,11	01,04,09		25	ns
				02,05,07,08		20	
				03,06		35	
Delay from write enable (LOW) to inactive output (HI-Z)	$t_{PLZ(\overline{WE})}$ $t_{PHZ(\overline{WE})}$	See figures 4 and 5 4/ 5/	9,10,11	01,03,04,06		35	ns
				02,05,09		25	
				07,08		20	

1/ These are absolute voltages with respect to device ground pin and include all overshoots due to system and/or tester noise. Do not attempt to test these values without suitable equipment.

2/ Not more than one output should be shorted at a time. Duration of the short circuit should not be more than one second.

3/ Parameters $t_{PLH(A)}$ and $t_{PHL(A)}$ are tested with S1 closed and CL = 30 pF with both input and output timing referenced to 1.5 V.

4/ For open collector, all delays from Write Enable ($\overline{WE}$) or Chip Select ($\overline{CS}$) inputs to the Data Output (D_{OUT}), $t_{PLZ(\overline{WE})}$, $t_{PLZ(\overline{CS})}$, $t_{PZL(\overline{WE})}$, and $t_{PZL(\overline{CS})}$ are measured with S1 closed and C1 = 30 pF; and with both the input and output timing referenced to 1.5 V.

5/ For 3-state output, $t_{PZH(\overline{WE})}$ and $t_{PZH(\overline{CS})}$ are measured with S1 open, CL = 30 pF and with both the input and output timing referenced to 1.5 V. Parameters $t_{PZL(\overline{WE})}$ and $t_{PZL(\overline{CS})}$ are measured with S1 closed, CL = 30 pF and with both the input and output timing referenced to 1.5 V. Parameters $t_{PHZ(\overline{WE})}$ and $t_{PHZ(\overline{CS})}$ are measured with S1 open and CL $\le$ 5 pF and are measured between the 1.5 V level on the input and the V_{OH} = -500 mV level on the output. Parameters $t_{PLZ(\overline{WE})}$ and $t_{PLZ(\overline{CS})}$ are measured with S1 closed CL $\le$ 5 pF and are measured between the 1.5 V level on the input and the V_{OL} = +500 mV level on the output.

6/ Output is preconditioned to data in (inverted) during write to ensure correct data is present on all outputs when write is terminated. (No write recovery glitch).

3.5 Certificate of compliance. A certificate of compliance shall be required from a manufacturer in order to be listed as an approved source of supply in 6.4. The certificate of compliance submitted to DESC-ECS prior to listing as an approved source of supply shall state that the manufacturer's product meets the requirements of MIL-STD-883 (see 3.1 herein) and the requirements herein.

3.6 Certificate of conformance. A certificate of conformance as required in MIL-STD-883 (see 3.1 herein) shall be provided with each lot of microcircuits delivered to this drawing.

3.7 Notification of change. Notification of change to DESC-ECS shall be required in accordance with MIL-STD-883 (see 3.1 herein).

3.8 Verification and review. DESC, DESC's agent, and the acquiring activity retain the option to review the manufacturer's facility and applicable required documentation. Offshore documentation shall be made available onshore at the option of the reviewer.

4. QUALITY ASSURANCE PROVISIONS

4.1 Sampling and inspection. Sampling and inspection procedures shall be in accordance with section 4 of MIL-M-38510 to the extent specified in MIL-STD-883 (see 3.1 herein).

4.2 Screening. Screening shall be in accordance with method 5004 of MIL-STD-883, and shall be conducted on all devices prior to quality conformance inspection. The following additional criteria shall apply:

a. Burn-in test, method 1015 of MIL-STD-883.

(1) Test condition A, B, C, or D using the circuit submitted with the certificate of compliance (see 3.5 herein).

(2) T_A = +125°C, minimum.

b. Interim and final electrical test parameters shall be as specified in table II herein, except interim electrical parameter tests prior to burn-in are optional at the discretion of the manufacturer.

4.3 Quality conformance inspection. Quality conformance inspection shall be in accordance with method 5005 of MIL-STD-883 including groups A, B, C, and D inspections. The following additional criteria shall apply.

4.3.1 Group A inspection.

a. Tests shall be as specified in table II herein.

b. Subgroups 5 and 6 in table I, method 5005 of MIL-STD-883 shall be omitted.

c. Subgroup 4 (C_{IN} and C_{OUT} measurements) shall be measured only for the initial process or design changes which may affect capacitance. Sample size is 15 devices with no failures, and all input and output terminals tested.

TABLE II. Electrical test requirements.

MIL-STD-883 test requirements	Subgroups (per method 5005, table I)
Interim electrical parameters (method 5004)	---
Final electrical test parameters (method 5004)	1*,2,3,7,8,9, 10**,11**
Group A test requirements (method 5005)	1,2,3,4***,7,8, 9,10**,11**
Groups C and D end-point electrical parameters (method 5005)	1,2,3

* PDA applies to subgroup 1.
** Subgroups 10 and 11, if not tested, shall be guaranteed to the specified limits in table I.
*** For subgroup 4 see 4.3.1c.

4.3.2 Groups C and D inspections.

a. End-point electrical parameters shall be as specified in table II herein.

b. Steady-state life test conditions, method 1005 of MIL-STD-883.

(1) Test condition A, B, C, or D using the circuit submitted with the certificate of compliance (see 3.5 herein).

(2) T_A = +125°C, minimum.

(3) Test duration: 1,000 hours, except as permitted by method 1005 of MIL-STD-883.

5. PACKAGING

5.1 Packaging requirements. The requirements for packaging shall be in accordance with MIL-M-38510.

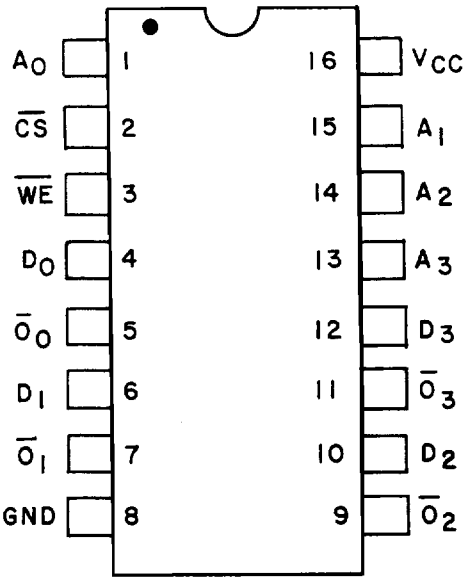
6. NOTES

6.1 Intended use. Microcircuits conforming to this drawing are intended for use when military specifications do not exist and qualified military devices that will perform the required function are not available for OEM application. When a military specification exists and the product covered by this drawing has been qualified for listing on QPL-38510, the device specified herein will be inactivated and will not be used for new design. The QPL-38510 product shall be the preferred item for all applications.

6.2 Replaceability. Microcircuits covered by this drawing will replace the same generic device covered by a contractor-prepared specification or drawing.

6.3 Comments. Comments on this drawing should be directed to DESC-ECS, Dayton, Ohio 45444, or telephone 513-296-5375.

Cases E and F



Case 2

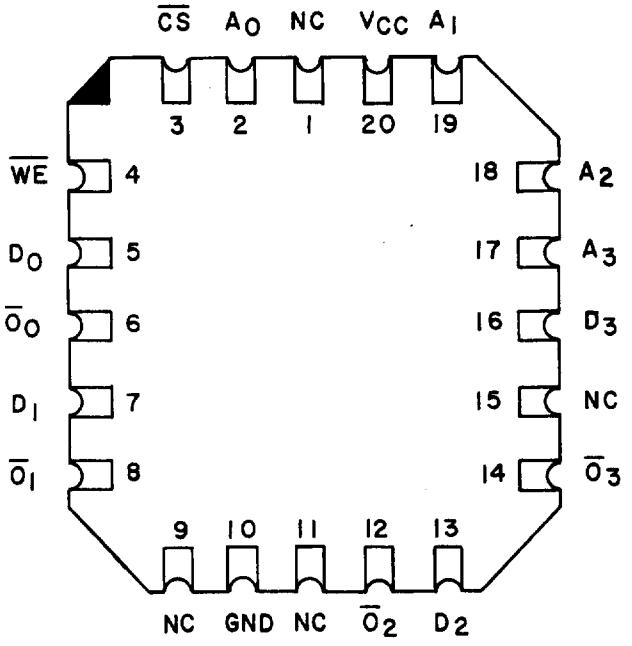


FIGURE 1. Terminal connections.

Input		Data output status $\overline{O}_0$-$\overline{O}_3$	Mode
$\overline{CS}$	$\overline{WE}$		
L	L	Output disabled	Write
L	H	Selected word (inverted)	Read
H	X	Output disabled	Deselect

H = HIGH
L = LOW
X = Don't Care

FIGURE 2. Truth table.

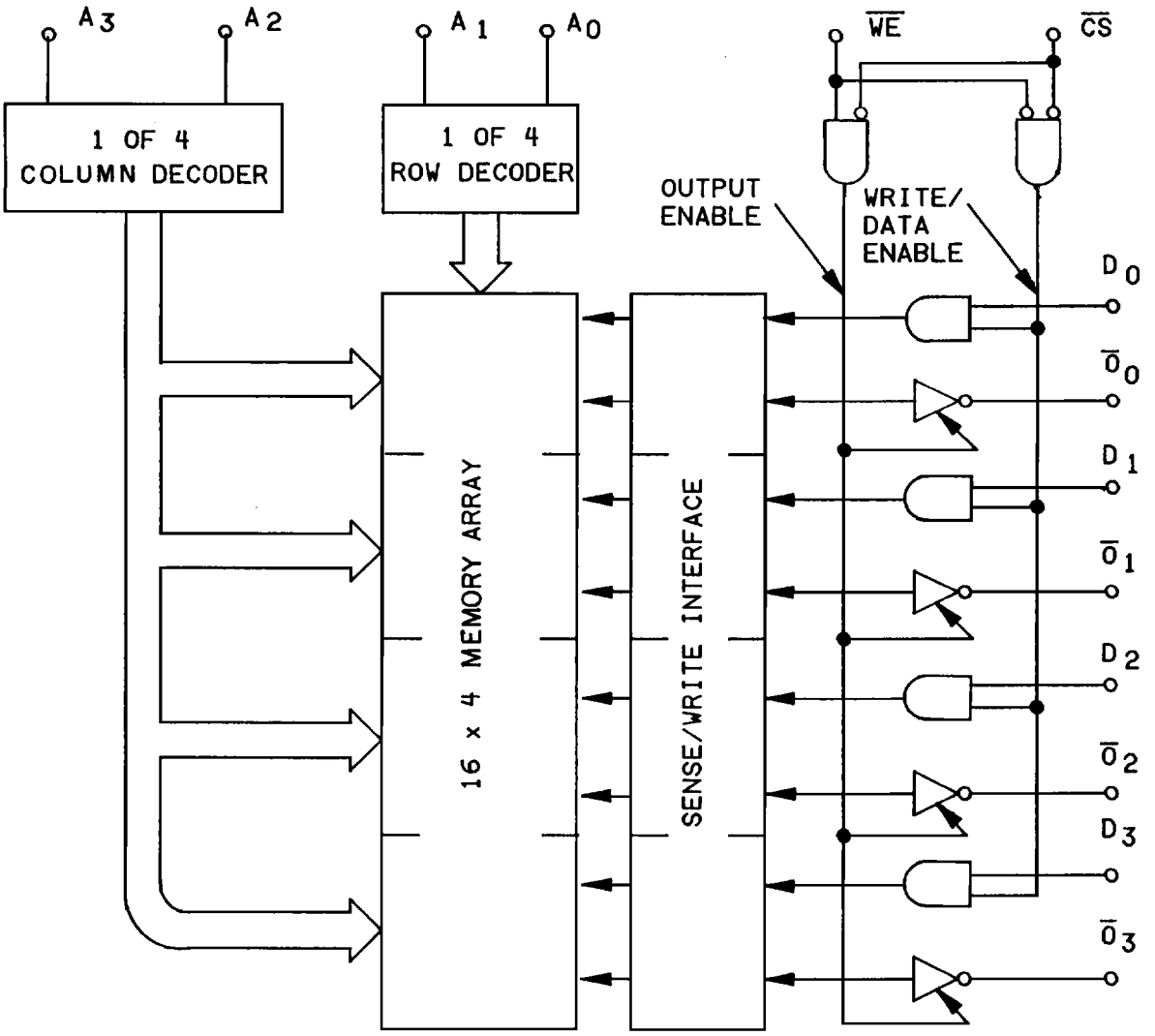
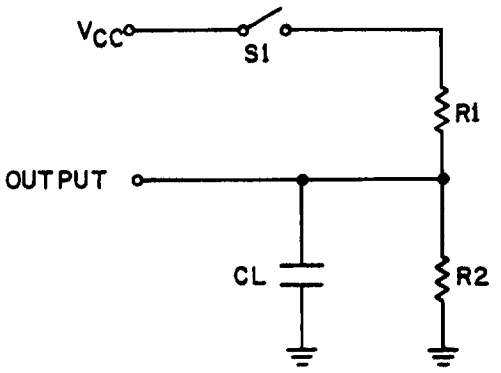
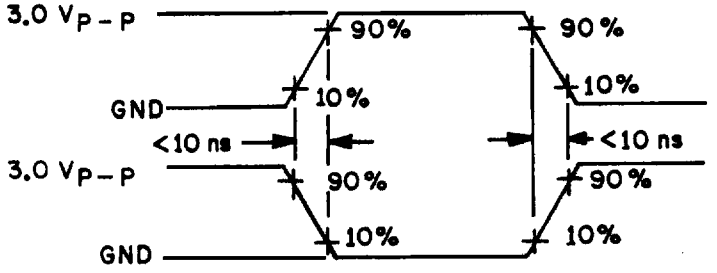


FIGURE 3. Logic diagram.

SWITCHING TEST
CIRCUIT

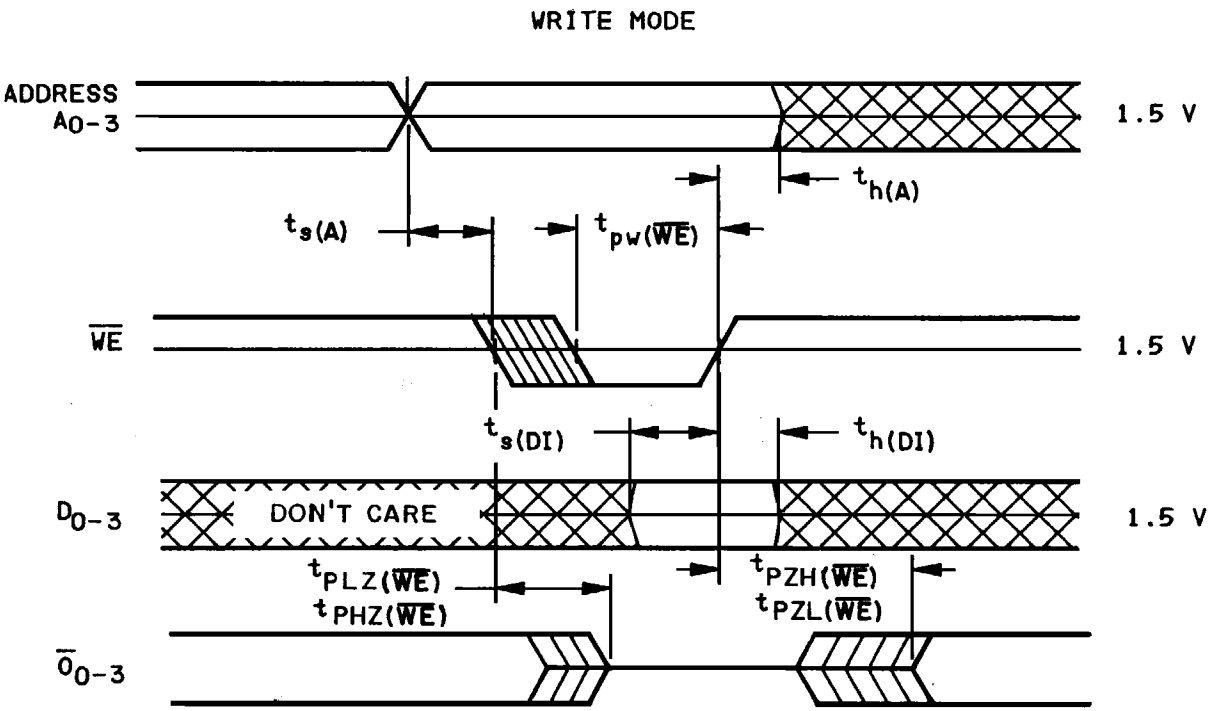


SWITCHING TEST
WAVEFORM



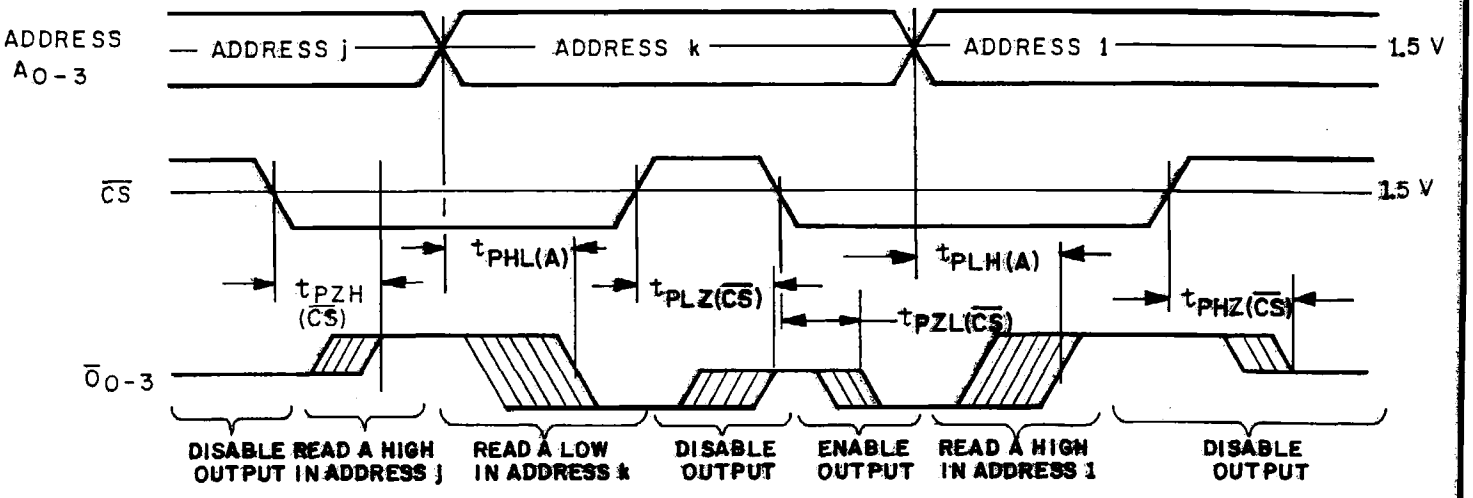
Device	R1	R2
01, 02 04, 05 07, 08	300Ω	600Ω
03, 06, 09	600Ω	1200Ω

FIGURE 4. Switching test circuit and waveform.



NOTE: Write cycle timing. The cycle is initiated by an address change. After $t_{s(A)}$ minimum the write enable may begin. The chip select must also be LOW for writing. Following the write pulse, $t_{h(A)}$ minimum must be allowed before the address may be changed again. The output will be inactive (floating for the 04, 05, 06, 08, and 09) while the write enable is LOW.

FIGURE 5. Write mode switching waveform.



NOTE: Switching delays from address and chip select inputs to the data output. For the 04, 05, 06, 08, and 09 device types disabled output is "OFF", represented by a single center line. For the 01, 02, 03, and 07 device types a disable output is HIGH.

FIGURE 6. Read mode switching waveform.

6.4 Approved source of supply. An approved source of supply is listed herein. Additional sources will be added as they become available. The vendor listed herein has agreed to this drawing and a certificate of compliance (see 3.5) has been submitted to DESC-ECS.

Military drawing part number	Vendor CAGE number	Vendor similar part number 1/
8605101EX	34335	AM27S02/BEA
8605101FX	34335	AM27S02/BFA
86051012X	34335	AM27S02/B2A
8605102EX	34335	AM27S02A/BEA
8605102FX	34335	AM27S02A/BFA
86051022X	34335	AM27S02A/B2A
8605103EX	2/	AM27LS02/BEA
8605103FX	2/	AM27LS02/BFA
86051032X	2/	AM27LS02/B2A
8605104EX	34335	AM27S03/BEA
8605104FX	34335	AM27S03/BFA
86051042X	34335	AM27S03/B2A
8605105EX	34335	AM27S03A/BEA
8605105FX	34335	AM27S03A/BFA
86051052X	34335	AM27S03A/B2A
8605106EX	34335	AM27LS03/BEA
8605106FX	34335	AM27LS03/BFA
86051062X	34335	AM27LS03/B2A
8605107EX	34335	AM27S02-20/BEA
8605107FX	34335	AM27S02-20/BFA
86051072X	34335	AM27S02-20/B2A
8605108EX	34335	AM27S03-20/BEA
8605108FX	34335	AM27S03-20/BFA
86051082X	34335	AM27S03-20/B2A
8605109EX	34335	AM27LS03-30/BEA
8605109FX	34335	AM27LS03-30/BFA
86051092X	34335	AM27LS03-30/B2A

1/ CAUTION. Do not use this number for item acquisition. Items acquired to this number may not satisfy the performance requirements of this drawing.

2/ Not available from approved source.

Vendor CAGE number	Vendor name and address
34335	Advanced Micro Devices, Incorporated 901 Thompson Place P.O. Box 3453 Sunnyvale, CA 94088

☆ U.S. GOVERNMENT PRINTING OFFICE: 1988—549-904