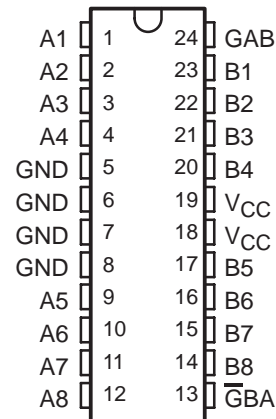


74ACT11623 OCTAL BUS TRANSCEIVER WITH 3-STATE OUTPUTS

SCAS059A – D2957, JULY 1987 – REVISED APRIL 1993

- Local Bus-Latch Capability
- Inputs Are TTL-Voltage Compatible
- Flow-Through Architecture Optimizes PCB Layout
- Center-Pin V_{CC} and GND Configurations Minimize High-Speed Switching Noise
- EPIC™ (Enhanced-Performance Implanted CMOS) 1- μ m Process
- 500-mA Typical Latch-Up Immunity at 125°C
- Package Options Include Plastic Small-Outline Packages and Standard Plastic 300-mil DIPs

DW OR NT PACKAGE
(TOP VIEW)



description

The 74ACT11623 is designed for asynchronous two-way communication between data buses. The control function implementation allows for maximum flexibility in timing.

The device allows data transmission from the A bus to the B bus or from the B bus to the A bus depending upon the logic levels at the enable inputs ($\overline{G}BA$ and GAB). The enable inputs can be used to disable the device so that the buses are effectively isolated.

The dual-enable configuration gives these devices the capability to store data by simultaneous enabling of $\overline{G}BA$ and GAB. Each output reinforces its input in this transceiver configuration. Thus, when both control inputs are enabled and all other data sources to the two sets of bus lines are at high impedance, both sets of bus lines (16 in all) will remain at their last states. The 8-bit codes appearing on the two sets of buses will be identical for the 74ACT11623.

The 74ACT11623 is characterized for operation from -40°C to 85°C .

FUNCTION TABLE

ENABLE INPUTS		OPERATION
$\overline{G}BA$	GAB	
L	L	B data to A bus
H	H	A data to B bus
H	L	Isolation
L	H	B data to A bus, A data to B bus

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PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.



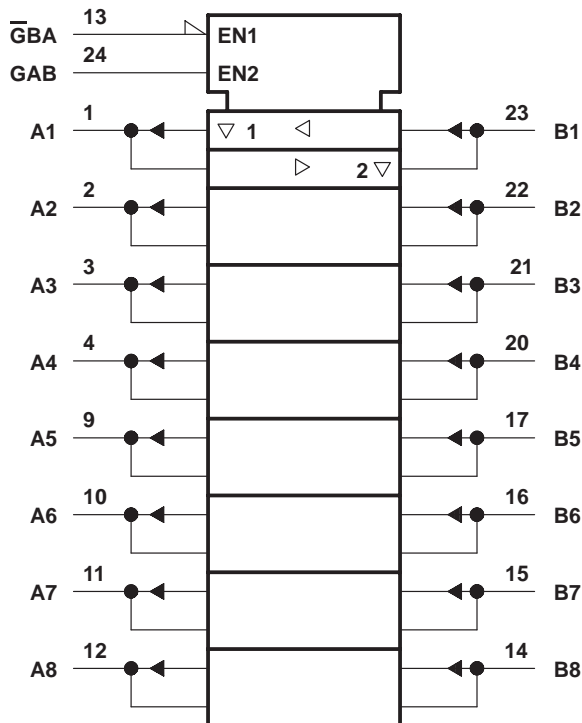
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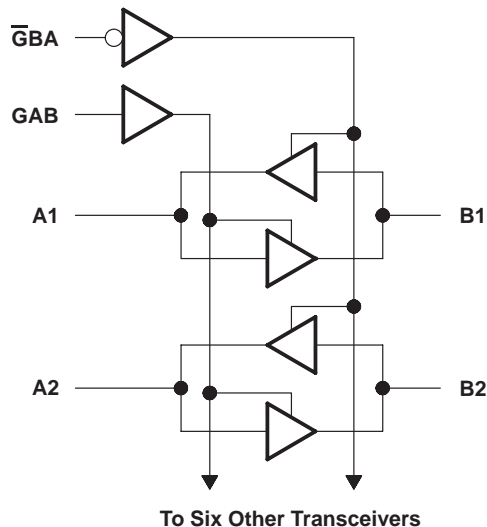
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logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

logic diagram (positive logic)



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)‡

Supply voltage range, V_{CC}	-0.5 V to 7 V
Input voltage range, V_I (see Note 1)	-0.5 V to $V_{CC} + 0.5$ V
Output voltage range, V_O (see Note 1)	-0.5 V to $V_{CC} + 0.5$ V
Input clamp current, I_{IK} ($V_I < 0$ or $V_I > V_{CC}$)	± 20 mA
Output clamp current, I_{OK} ($V_O < 0$ or $V_O > V_{CC}$)	± 50 mA
Continuous output current, I_O ($V_O = 0$ to V_{CC})	± 50 mA
Continuous current through V_{CC} or GND	± 200 mA
Storage temperature range	-65°C to 150°C

‡ Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

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recommended operating conditions

		MIN	MAX	UNIT
V_{CC}	Supply voltage	4.5	5.5	V
V_{IH}	High-level input voltage	2		V
V_{IL}	Low-level input voltage		0.8	V
V_I	Input voltage	0	V_{CC}	V
V_O	Output voltage	0	V_{CC}	V
I_{OH}	High-level output current		-24	mA
I_{OL}	Low-level output current		24	mA
$\Delta t/\Delta v$	Input transition rise or fall rate	0	10	ns/V
T_A	Operating free-air temperature	-40	85	°C

electrical characteristics over recommended operating free-air temperature range

PARAMETER	TEST CONDITIONS	V_{CC}	$T_A = 25^\circ\text{C}$			MIN	MAX	UNIT
			MIN	TYP	MAX			
V_{OH}	$I_{OH} = -50 \mu\text{A}$	4.5 V	4.4		4.4		V	
		5.5 V	5.4		5.4			
	$I_{OH} = -24 \text{ mA}$	4.5 V	3.94		3.8			
		5.5 V	4.94		4.8			
	$I_{OH} = -75 \text{ mA}^\dagger$	5.5 V			3.85			
	V_{OL}	$I_{OL} = 50 \mu\text{A}$	4.5 V			0.1		0.1
5.5 V					0.1	0.1		
$I_{OL} = 24 \text{ mA}$		4.5 V			0.36	0.44		
		5.5 V			0.36	0.44		
$I_{OL} = 75 \text{ mA}^\dagger$		5.5 V				1.65		
I_{OZ}		A or B ports [‡]	$V_O = V_{CC}$ or GND	5.5 V		± 0.5	± 5	μA
I_I	$\overline{\text{G}}\text{BA}$ or GAB	$V_I = V_{CC}$ or GND	5.5 V		± 0.1	± 1	μA	
I_{CC}		$V_I = V_{CC}$ or GND, $I_O = 0$	5.5 V		4	40	μA	
ΔI_{CC}^\S		One input at 3.4 V, Other inputs at GND or V_{CC}	5.5 V		0.9	1	mA	
C_i	$\overline{\text{G}}\text{BA}$ or GAB	$V_I = V_{CC}$ or GND	5 V		4		pF	
C_{io}	A or B ports	$V_O = V_{CC}$ or GND	5 V		20		pF	

[†] Not more than one output should be tested at a time, and the duration of the test should not exceed 10 ms.

[‡] For I/O ports, the parameter I_{OZ} includes the input leakage.

[§] This is the increase in supply current for each input that is at one of the specified TTL voltage levels rather than 0 V or V_{CC} .

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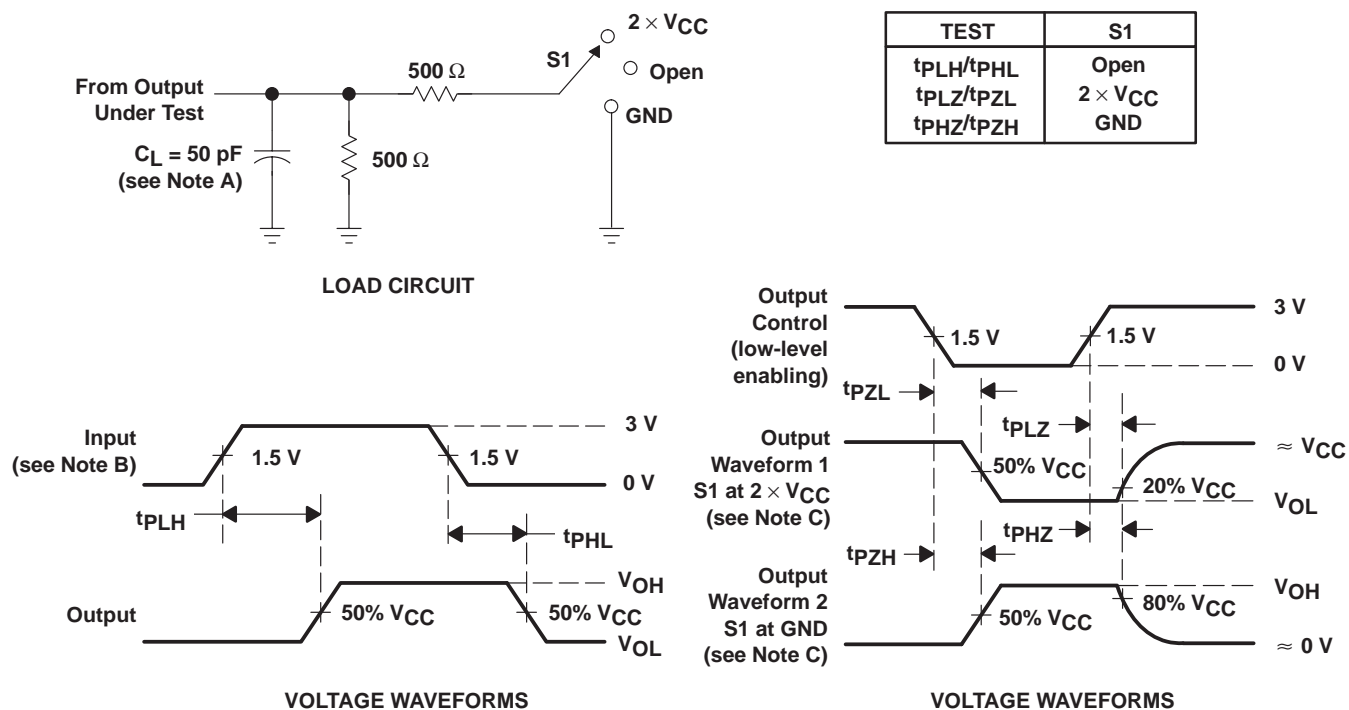
switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	T _A = 25°C			MIN	MAX	UNIT
			MIN	TYP	MAX			
t _{PLH}	A or B	B or A	1.5	6	7.5	1.5	8.5	ns
t _{PHL}			1.5	5.5	7.2	1.5	7.9	
t _{PZH}	$\overline{\text{G}}\text{BA}$	A	1.5	6.9	8.6	1.5	9.7	ns
t _{PZL}			1.5	6.9	9	1.5	10	
t _{PHZ}	$\overline{\text{G}}\text{BA}$	A	1.5	8.1	10	1.5	10.9	ns
t _{PLZ}			1.5	8.5	10.5	1.5	11.5	
t _{PZH}	GAB	B	1.5	7.7	9.3	1.5	10.7	ns
t _{PZL}			1.5	7.7	9.7	1.5	10.9	
t _{PHZ}	GAB	B	1.5	7.1	8.8	1.5	9.5	ns
t _{PLZ}			1.5	7.3	9.2	1.5	10	

operating characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER		TEST CONDITIONS		TYP	UNIT
C _{pd}	Power dissipation capacitance per transceiver	Outputs enabled	C _L = 50 pF, f = 1 MHz	41	pF
		Outputs disabled		8	

PARAMETER MEASUREMENT INFORMATION



- NOTES: A. C_L includes probe and jig capacitance.
 B. All input pulses are supplied by generators having the following characteristics: $PRR \leq 10 \text{ MHz}$, $Z_O = 50 \Omega$, $t_r = 3 \text{ ns}$, $t_f = 3 \text{ ns}$.
 C. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
 D. The outputs are measured one at a time with one input transition per measurement.

Figure 1. Load Circuit and Voltage Waveforms

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
74ACT11623DWR	ACTIVE	SOIC	DW	24	2000	Green (RoHS & no Sb/Br)	NIPDAU	Level-1-260C-UNLIM	-40 to 85	ACT11623	Samples

(1) The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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TAPE AND REEL INFORMATION



QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
74ACT11623DWR	SOIC	DW	24	2000	330.0	24.4	10.75	15.7	2.7	12.0	24.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
74ACT11623DWR	SOIC	DW	24	2000	350.0	350.0	43.0

DW (R-PDSO-G24)

PLASTIC SMALL OUTLINE



- NOTES:
- A. All linear dimensions are in inches (millimeters). Dimensioning and tolerancing per ASME Y14.5M-1994.
 - B. This drawing is subject to change without notice.
 - C. Body dimensions do not include mold flash or protrusion not to exceed 0.006 (0,15).
 - D. Falls within JEDEC MS-013 variation AD.

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