User Guide
EVB-ATEK252N3-01

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Revisions

Revision No	Revision Date	Revision Reason	Section / Page No
1.0	08.07.2021	Initial Version	
1.1	08.01.2022	Format and Content Fixed	
1.2	16.04.2022	Format and Content Fixed	

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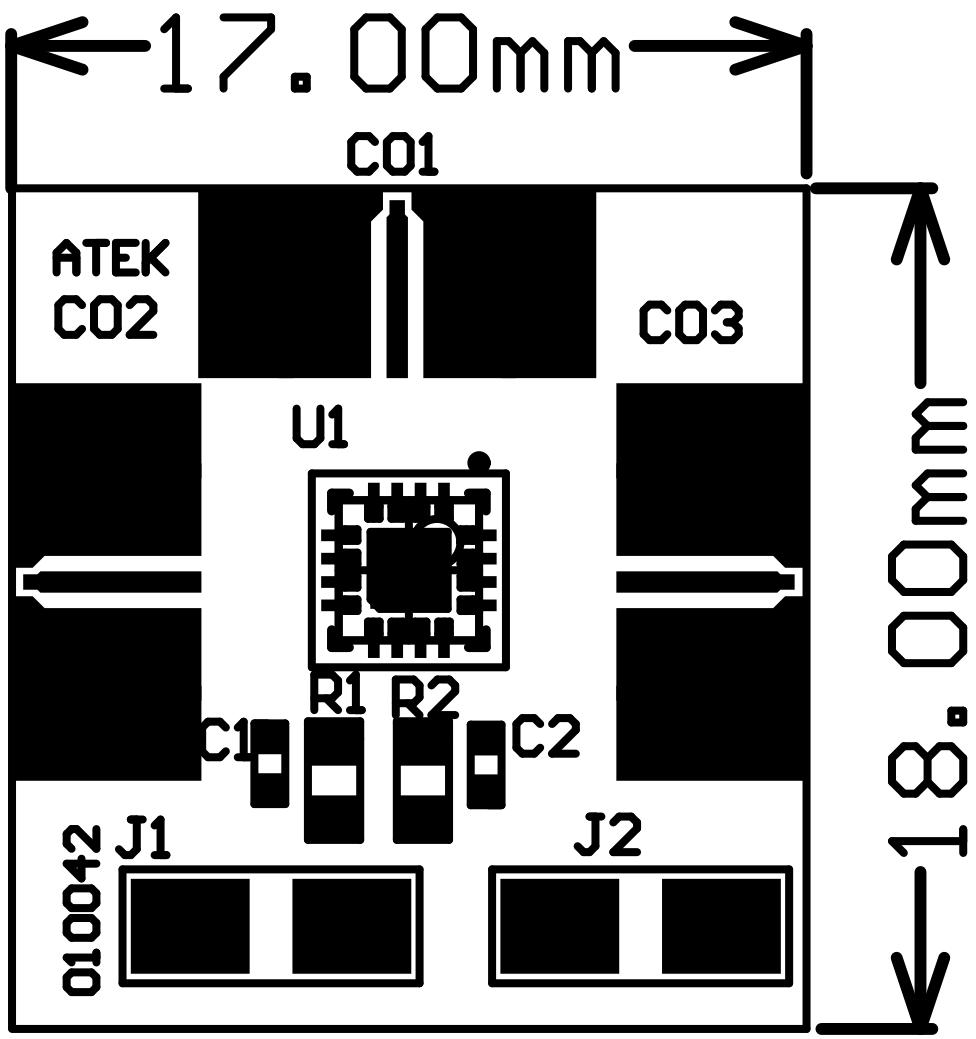
1 GENERAL INFORMATION



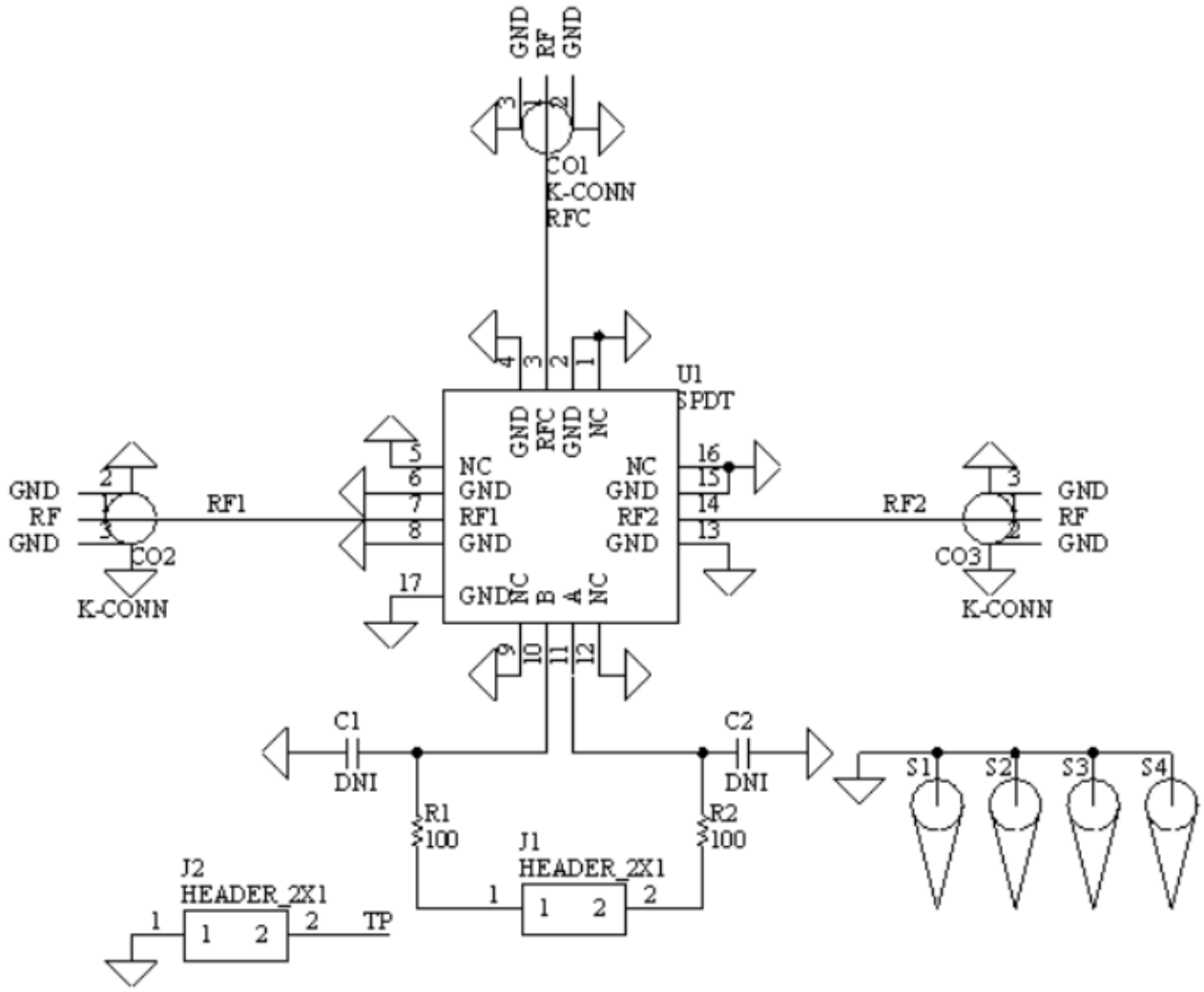
PIN Name	Definition	Comment
CO1	RF IN	K Connector
CO2, CO3	RF OUT	K Connector
J1 Left	CTRL B	2.54mm Header
J1 Right	CTRL A	2.54mm Header
J2 Left	N/A	2.54mm Header
J2 Right	GND	2.54mm Header

Notes:

1. VDD Voltage is detailed in Datasheet.
2. Control Voltage is detailed in Datasheet.
3. The definition of up, down, right, and left is valid for this view of PCB.

2 DESIGN INFORMATION

2.1 SCHEMATIC



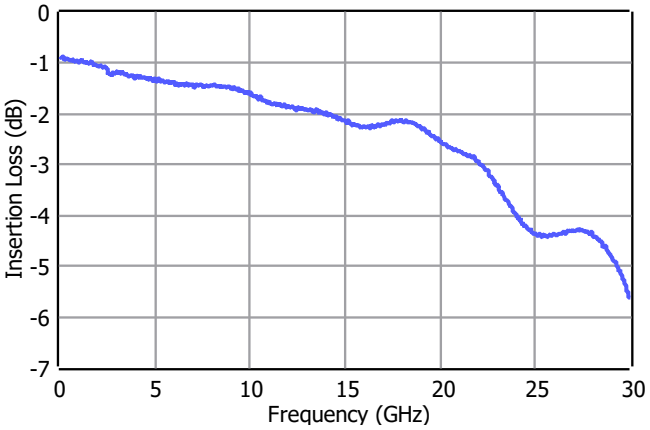
2.2 BOM

Designator	Footprint	Qty	Comment	PN
C1, C2	0402	2	DNP	
CO1, CO2, CO3	K Connector	3	K Connector	
J1, J2	2x1 Header	2	2x1 Header	
R1, R2	0603	2	0R	
U1	ATEKQ3316	1	SPDT	ATEK252N3

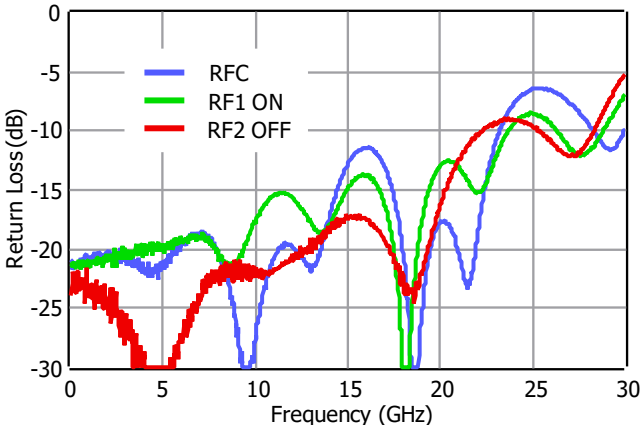
3 TYPICAL PERFORMANCE PLOTS

Conditions unless otherwise specified: V_{CTRL} =0/-5 V, T = 25 C, CW. For details, please refer to the datasheet.

Insertion Loss



Return Loss



Isolation from RFC to RF2