

N-channel 650 V, 0.425 Ω typ., 11 A MDmesh™ II Power MOSFET
in DPAK, TO-220FP, I²PAKFP and TO-220 packages

Datasheet - production data

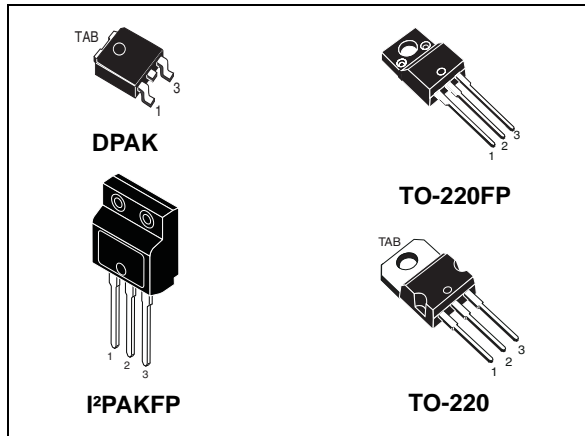
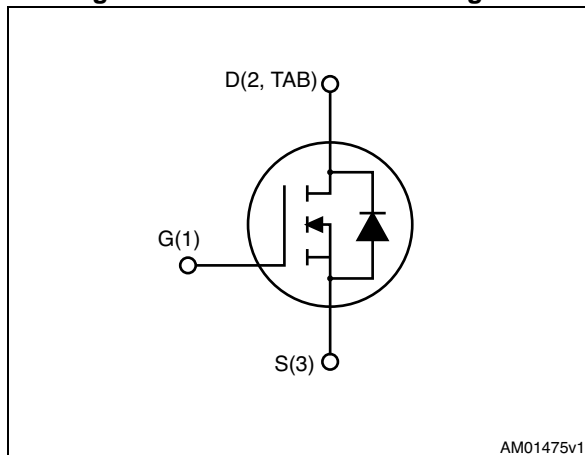


Figure 1. Internal schematic diagram



Features

Order codes	V_{DSS} @ T_{Jmax}	$R_{DS(on)}$ max	I_D
STD11NM65N	710 V	< 0.455 Ω	11 A
STF11NM65N			
STFI11NM65N			
STP11NM65N			

- 100% avalanche tested
- Low input capacitance and gate charge
- low gate input resistance

Applications

- Switching applications

Description

These devices are N-channel Power MOSFETs developed using the second generation of MDmesh™ technology. This revolutionary Power MOSFET associates a vertical structure to the company's strip layout to yield one of the world's lowest on-resistance and gate charge. It is therefore suitable for the most demanding high efficiency converters.

Table 1. Device summary

Order codes	Marking	Packages	Packaging
STD11NM65N	11NM65N	DPAK	Tape and reel
STF11NM65N		TO-220FP	Tube
STFI11NM65N		I ² PAKFP	
STP11NM65N		TO-220	

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1 Electrical ratings

Table 2. Absolute maximum ratings

Symbol	Parameter	Value		Unit
		TO-220, DPAK	TO-220FP I ² PAKFP	
V _{DS}	Drain-source voltage	650		V
V _{GS}	Gate-source voltage	± 25		V
I _D	Drain current (continuous) at T _C = 25 °C	11	11 ⁽¹⁾	A
I _D	Drain current (continuous) at T _C = 100 °C	7	7 ⁽¹⁾	A
I _{DM} ⁽²⁾	Drain current (pulsed)	44	44 ⁽¹⁾	A
P _{TOT}	Total dissipation at T _C = 25 °C	110	25	W
I _{AR}	Avalanche current, repetitive or not-repetitive (pulse width limited by T _j max)	3		A
E _{AS}	Single pulse avalanche energy (starting T _j = 25 °C, I _D = I _{AR} , V _{DD} = 50 V)	147		mJ
dv/dt ⁽³⁾	Peak diode recovery voltage slope	15		V/ns
V _{ISO}	Insulation withstand voltage (RMS) from all three leads to external heat sink (t = 1 s; T _C = 25 °C)		2500	V
T _{stg}	Storage temperature	- 55 to 150		°C
T _j	Max. operating junction temperature	150		°C

1. Limited by maximum junction temperature.
2. Pulse width limited by safe operating area.
3. I_{SD} ≤ 11 A, di/dt ≤ 400 A/μs; V_{Peak} < V_{(BR)DSS}, V_{DD} ≤ 80% V_{(BR)DSS}

Table 3. Thermal data

Symbol	Parameter	Value				Unit
		DPAK	TO-220FP	I ² PAKFP	TO-220	
R _{thj-case}	Thermal resistance junction-case max	1.14	5		1.14	°C/W
R _{thj-amb}	Thermal resistance junction-ambient max		62.5			°C/W
R _{thj-pcb} ⁽¹⁾	Thermal resistance junction-pcb max	50				°C/W

1. When mounted on 1inch² FR-4 board, 2 oz Cu

2 Electrical characteristics

($T_C = 25\text{ °C}$ unless otherwise specified)

Table 4. On /off states

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$V_{(BR)DSS}$	Drain-source breakdown voltage	$I_D = 1\text{ mA}$, $V_{GS} = 0$	650			V
I_{DSS}	Zero gate voltage drain current ($V_{GS} = 0$)	$V_{DS} = 650\text{ V}$ $V_{DS} = 650\text{ V}$, $T_C = 125\text{ °C}$			1 100	μA μA
I_{GSS}	Gate-body leakage current ($V_{DS} = 0$)	$V_{GS} = \pm 25\text{ V}$			± 100	nA
$V_{GS(th)}$	Gate threshold voltage	$V_{DS} = V_{GS}$, $I_D = 250\text{ }\mu\text{A}$	2	3	4	V
$R_{DS(on)}$	Static drain-source on-resistance	$V_{GS} = 10\text{ V}$, $I_D = 5.5\text{ A}$		0.425	0.455	Ω

Table 5. Dynamic

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
C_{iss}	Input capacitance	$V_{DS} = 50\text{ V}$, $f = 1\text{ MHz}$, $V_{GS} = 0$	-	800	-	pF pF pF
C_{oss}	Output capacitance		-	50	-	pF
C_{riss}	Reverse transfer capacitance		-	2.9	-	pF
$C_{oss\text{ eq.}}^{(1)}$	Equivalent output capacitance	$V_{DS} = 0\text{ to }520\text{ V}$, $V_{GS} = 0$	-	133	-	pF
R_G	Intrinsic gate resistance	$f = 1\text{ MHz}$ open drain	-	4.2	-	Ω
Q_g	Total gate charge	$V_{DD} = 520\text{ V}$, $I_D = 11\text{ A}$, $V_{GS} = 10\text{ V}$ (see Figure 19)	-	29	-	nC
Q_{gs}	Gate-source charge		-	3.9	-	nC
Q_{gd}	Gate-drain charge		-	16	-	nC

1. $C_{oss\text{ eq.}}^{(1)}$ is defined as a constant equivalent capacitance giving the same charging time as C_{oss} when V_{DS} increases from 0 to 80% V_{DSS}

Table 6. Switching times

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$t_{d(on)}$	Turn-on delay time	$V_{DD} = 325\text{ V}$, $I_D = 5.5\text{ A}$, $R_G = 4.7\ \Omega$, $V_{GS} = 10\text{ V}$ (see Figure 20 and Figure 23)	-	15.5	-	ns
t_r	Rise time		-	10.8	-	ns
$t_{d(off)}$	Turn-off delay time		-	11	-	ns
t_f	Fall time		-	47	-	ns

Table 7. Source drain diode

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
I_{SD}	Source-drain current		-		11	A
$I_{SDM}^{(1)}$	Source-drain current (pulsed)				44	A
$V_{SD}^{(2)}$	Forward on voltage	$I_{SD} = 11\text{ A}$, $V_{GS} = 0$	-		1.6	V
t_{rr}	Reverse recovery time	$I_{SD} = 11\text{ A}$, $di/dt = 100\text{ A}/\mu\text{s}$ $V_{DD} = 60\text{ V}$ (see Figure 23)	-	418		ns
Q_{rr}	Reverse recovery charge		-	4.4		μC
I_{RRM}	Reverse recovery current		-	21		A
t_{rr}	Reverse recovery time	$I_{SD} = 11\text{ A}$, $di/dt = 100\text{ A}/\mu\text{s}$ $V_{DD} = 60\text{ V}$, $T_J = 150\text{ }^\circ\text{C}$ (see Figure 23)	-	530		ns
Q_{rr}	Reverse recovery charge		-	5.6		μC
I_{RRM}	Reverse recovery current		-	21		A

1. Pulse width limited by safe operating area
2. Pulsed: pulse duration = 300 μs , duty cycle 1.5%

2.1 Electrical characteristics (curves)

Figure 2. Safe operating area for DPAK

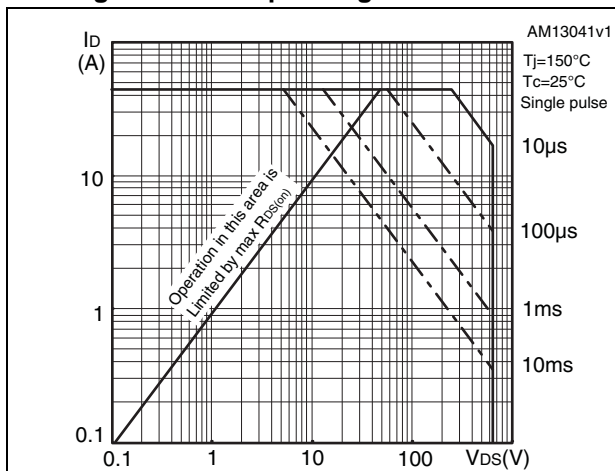


Figure 3. Thermal impedance for DPAK

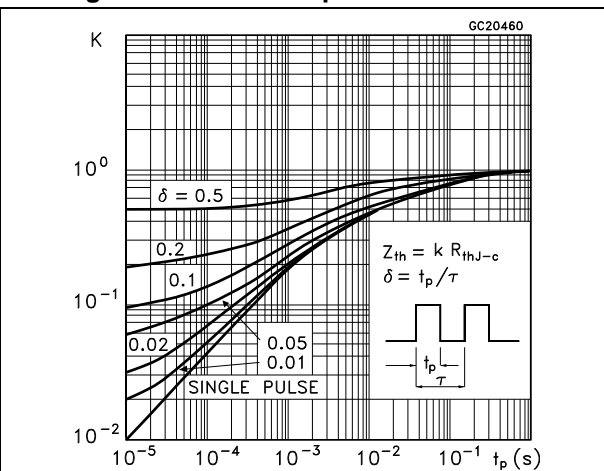


Figure 4. Safe operating area for TO-220FP and I²PAKFP

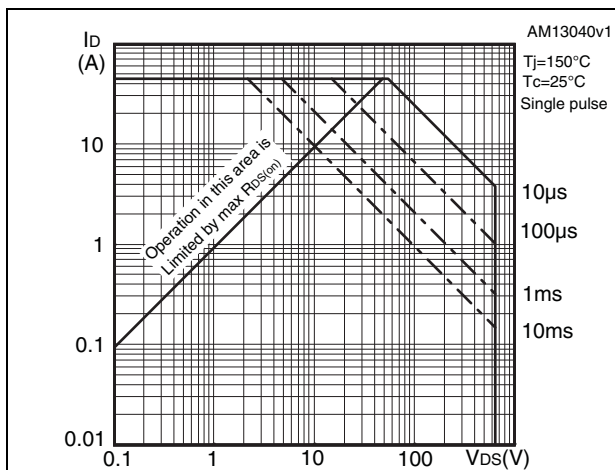


Figure 5. Thermal impedance for TO-220FP and I²PAKFP

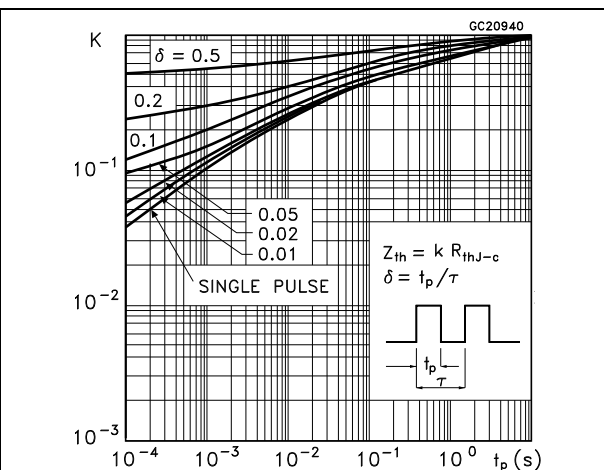


Figure 6. Safe operating area for TO-220

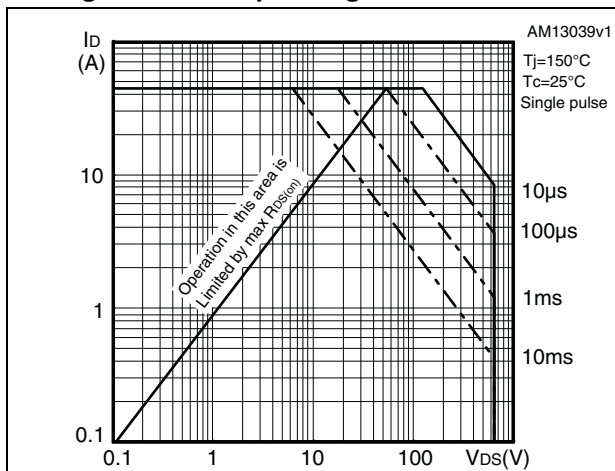


Figure 7. Thermal impedance for TO-220

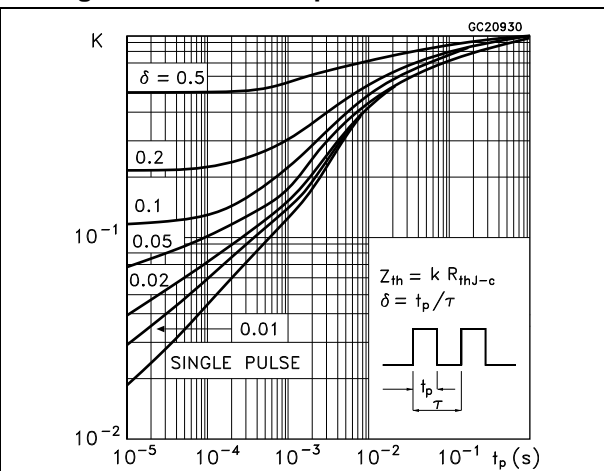


Figure 8. Output characteristics

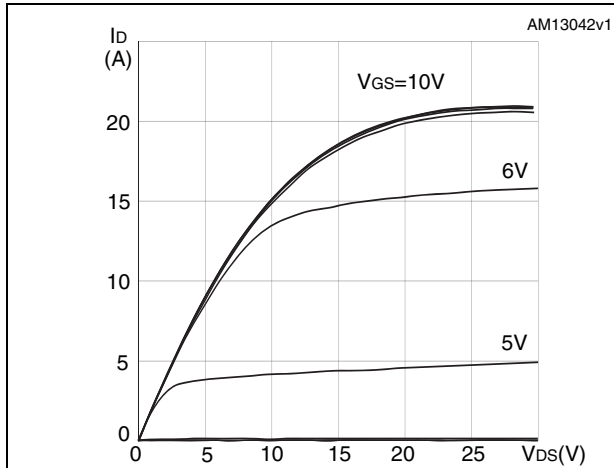


Figure 9. Transfer characteristics

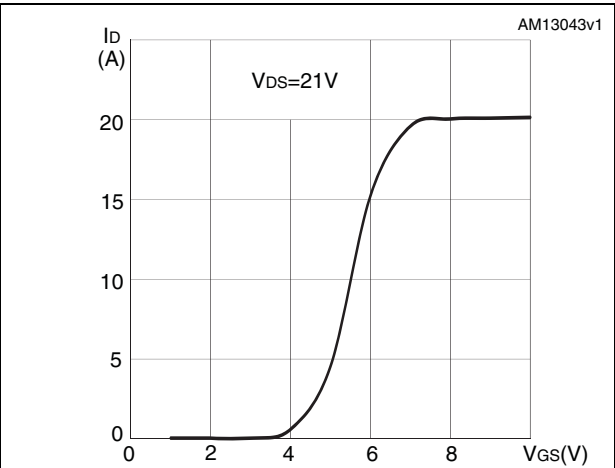


Figure 10. Gate charge vs gate-source voltage

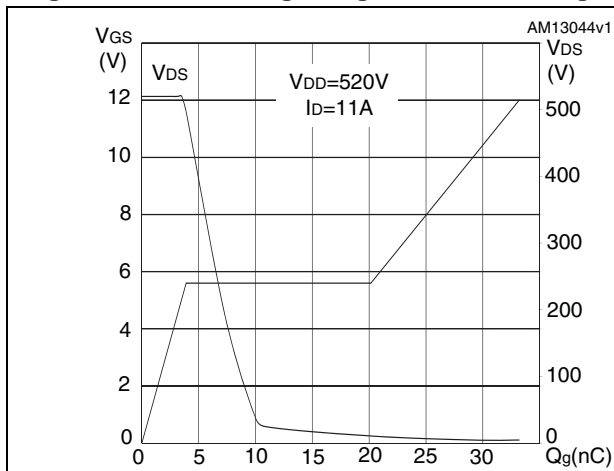


Figure 11. Static drain-source on resistance

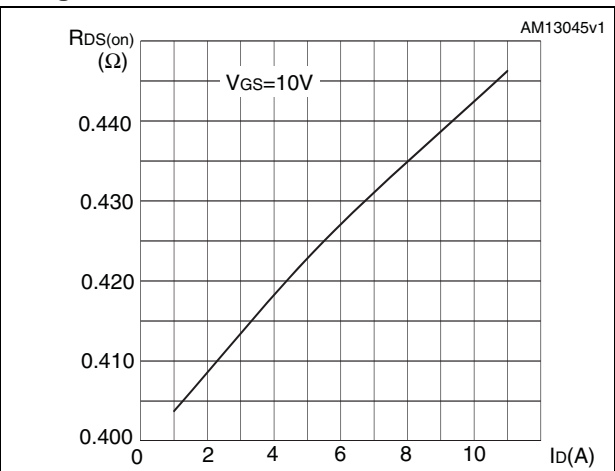


Figure 12. Capacitance variations

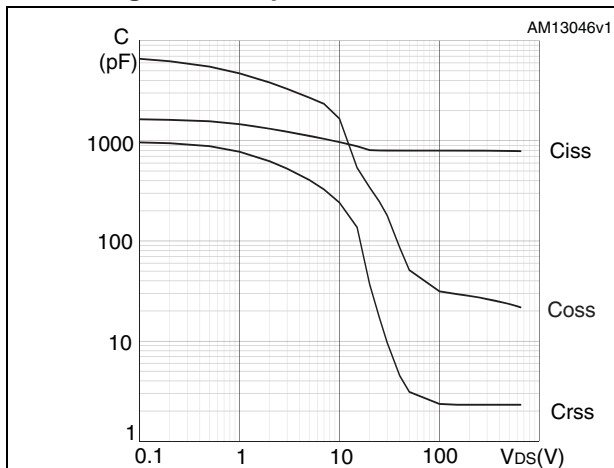


Figure 13. Output capacitance stored energy

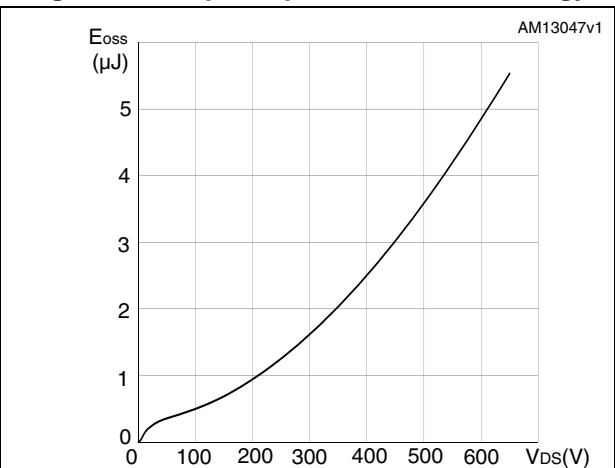


Figure 14. Normalized gate threshold voltage vs temperature

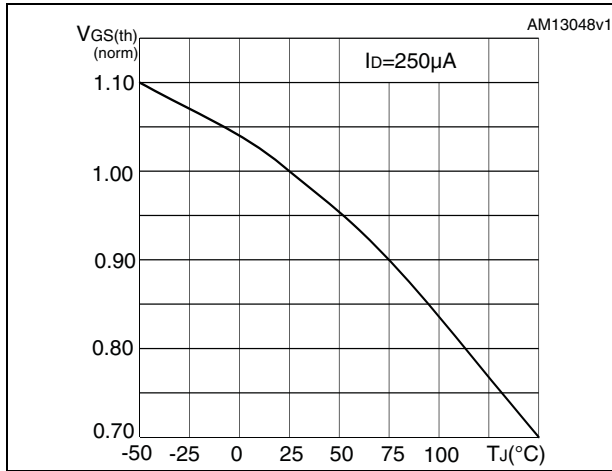


Figure 15. Normalized on-resistance vs temperature

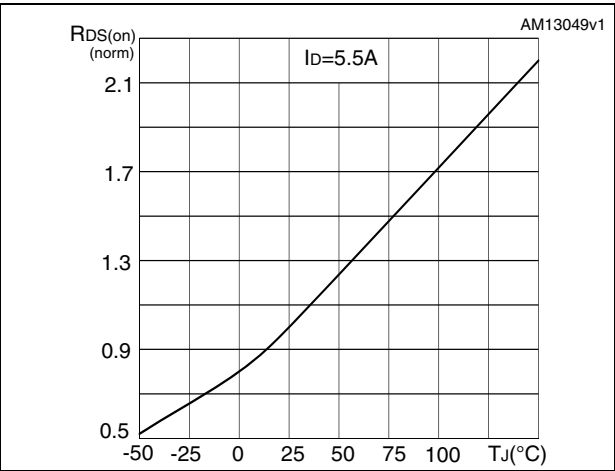


Figure 16. Source-drain diode forward characteristics

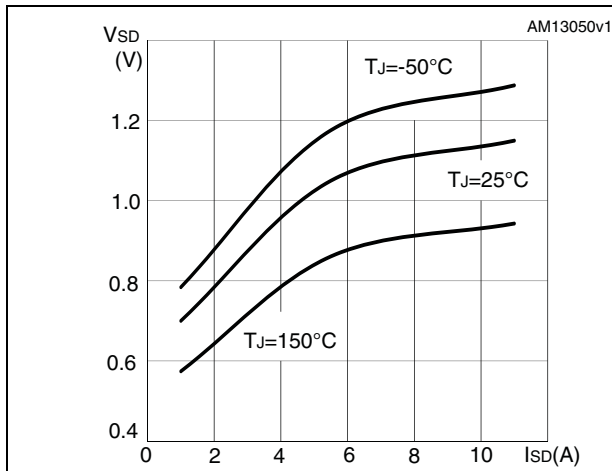
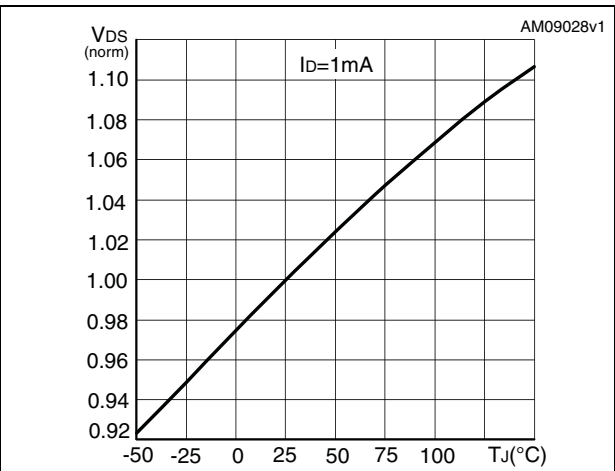


Figure 17. Normalized $B_{V_{DS}}$ vs temperature



3 Test circuits

Figure 18. Switching times test circuit for resistive load



Figure 19. Gate charge test circuit

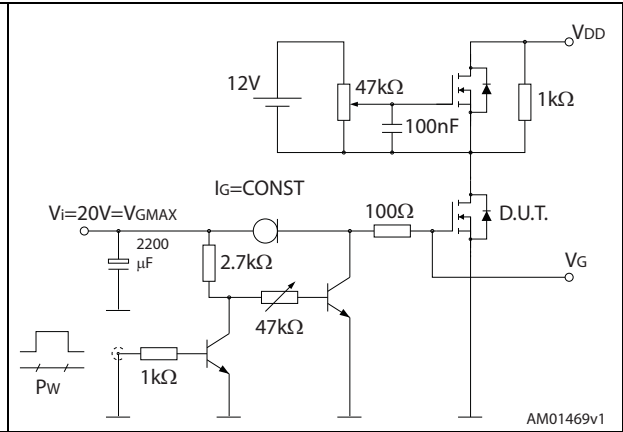


Figure 20. Test circuit for inductive load switching and diode recovery times



Figure 21. Unclamped inductive load test circuit

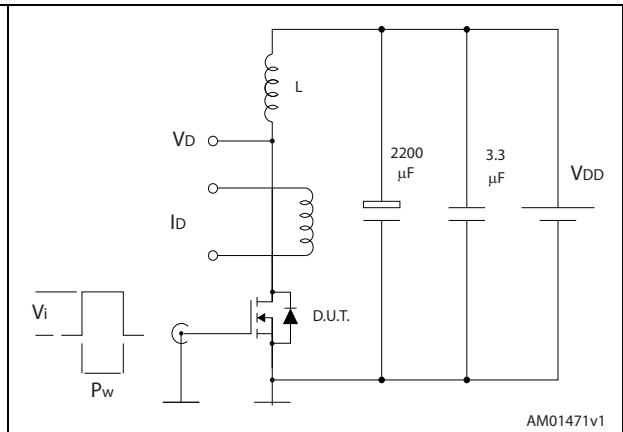
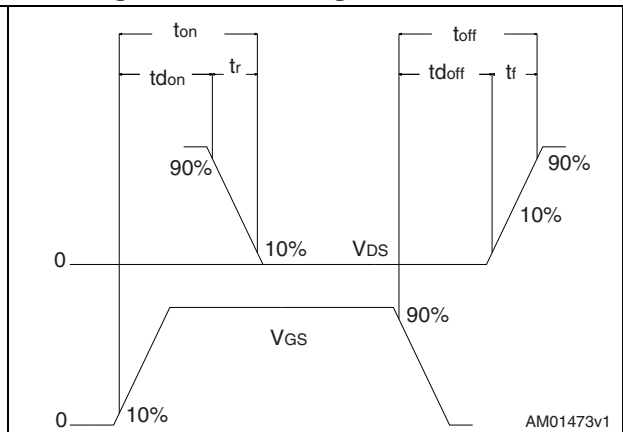


Figure 22. Unclamped inductive waveform



Figure 23. Switching time waveform



4 Package mechanical data

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK[®] packages, depending on their level of environmental compliance. ECOPACK[®] specifications, grade definitions and product status are available at: www.st.com. ECOPACK is an ST trademark.

Table 8. DPAK (TO-252) mechanical data

Dim.	mm		
	Min.	Typ.	Max.
A	2.20		2.40
A1	0.90		1.10
A2	0.03		0.23
b	0.64		0.90
b4	5.20		5.40
c	0.45		0.60
c2	0.48		0.60
D	6.00		6.20
D1		5.10	
E	6.40		6.60
E1		4.70	
e		2.28	
e1	4.40		4.60
H	9.35		10.10
L	1		1.50
L1		2.80	
L2		0.80	
L4	0.60		1
R		0.20	
V2	0°		8°

Figure 24. DPAK (TO-252) drawing

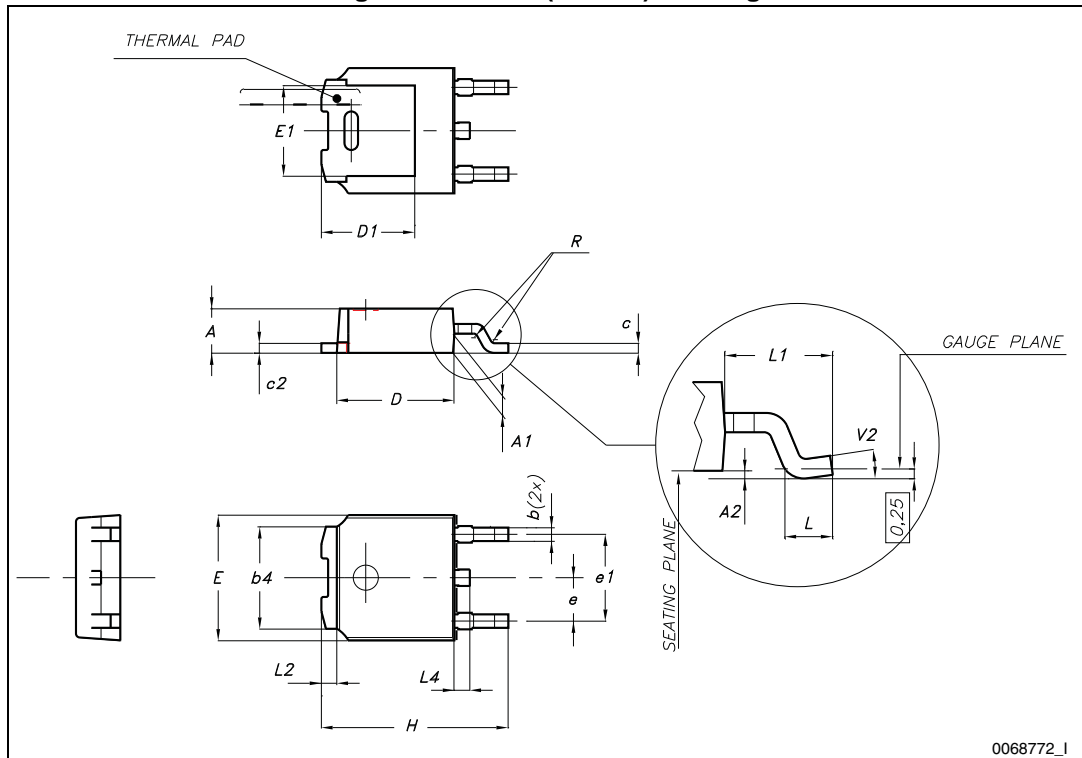
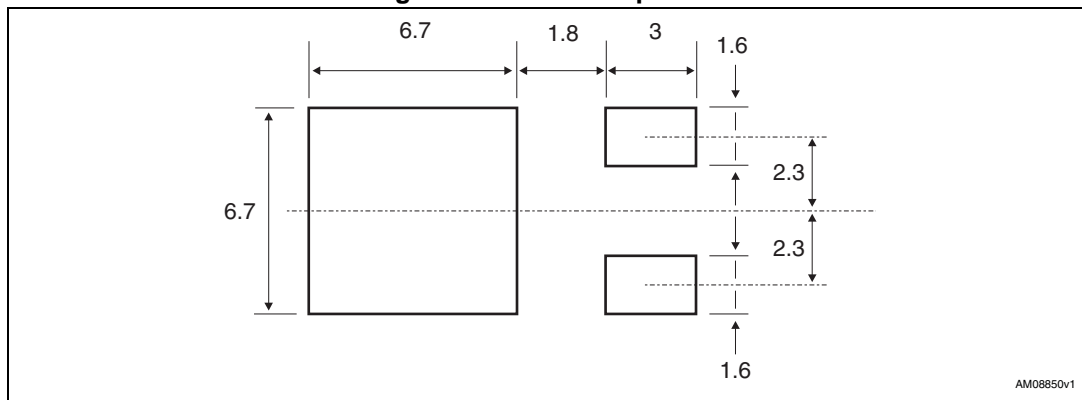


Figure 25. DPAK footprint(a)

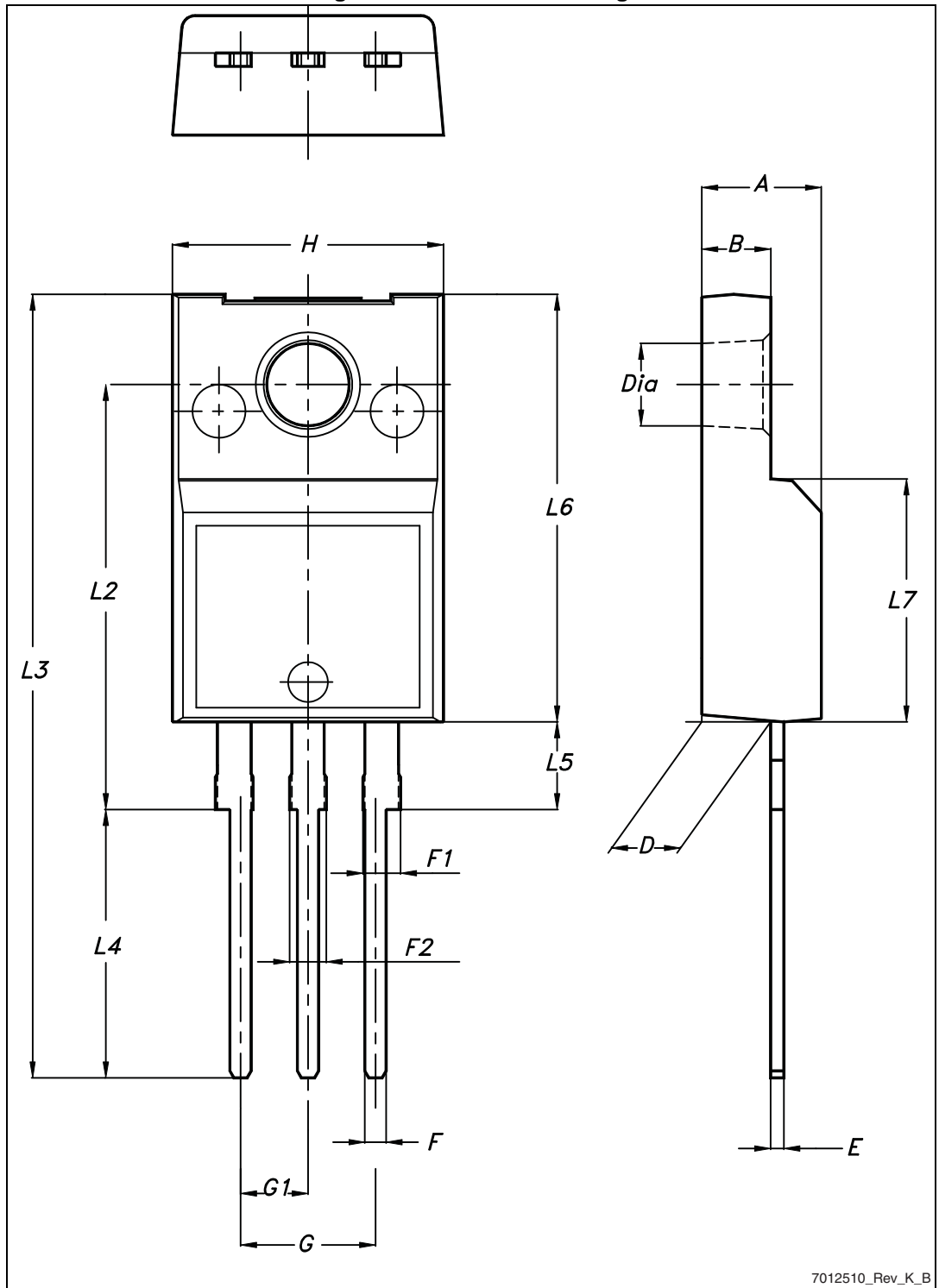


a. All dimension are in millimeters

Table 9. TO-220FP mechanical data

Dim.	mm		
	Min.	Typ.	Max.
A	4.4		4.6
B	2.5		2.7
D	2.5		2.75
E	0.45		0.7
F	0.75		1
F1	1.15		1.70
F2	1.15		1.70
G	4.95		5.2
G1	2.4		2.7
H	10		10.4
L2		16	
L3	28.6		30.6
L4	9.8		10.6
L5	2.9		3.6
L6	15.9		16.4
L7	9		9.3
Dia	3		3.2

Figure 26. TO-220FP drawing



7012510_Rev_K_B

Table 10. I²PAKFP (TO-281) mechanical data

Dim.	mm		
	Min.	Typ.	Max.
A	4.40	-	4.60
B	2.50		2.70
D	2.50		2.75
D1	0.65		0.85
E	0.45		0.70
F	0.75		1.00
F1			1.20
G	4.95		5.20
H	10.00		10.40
L1	21.00		23.00
L2	13.20		14.10
L3	10.55		10.85
L4	2.70		3.20
L5	0.85		1.25
L6	7.30		7.50

Figure 27. I²PAKFP (TO-281) drawing

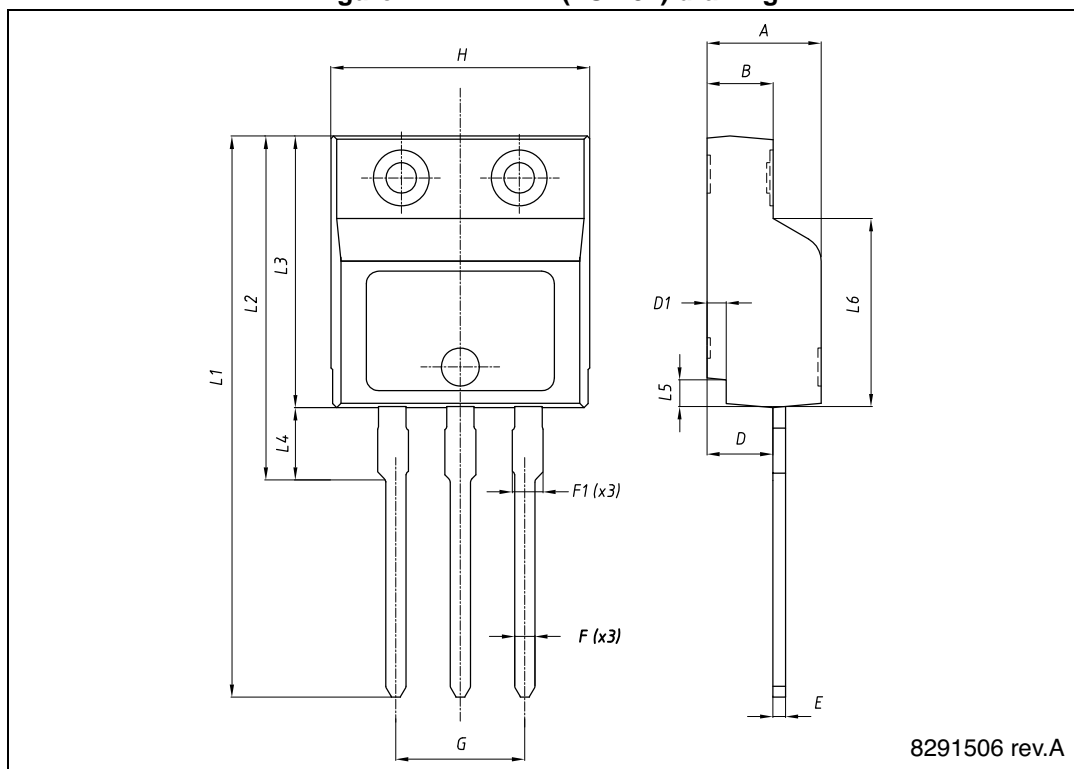
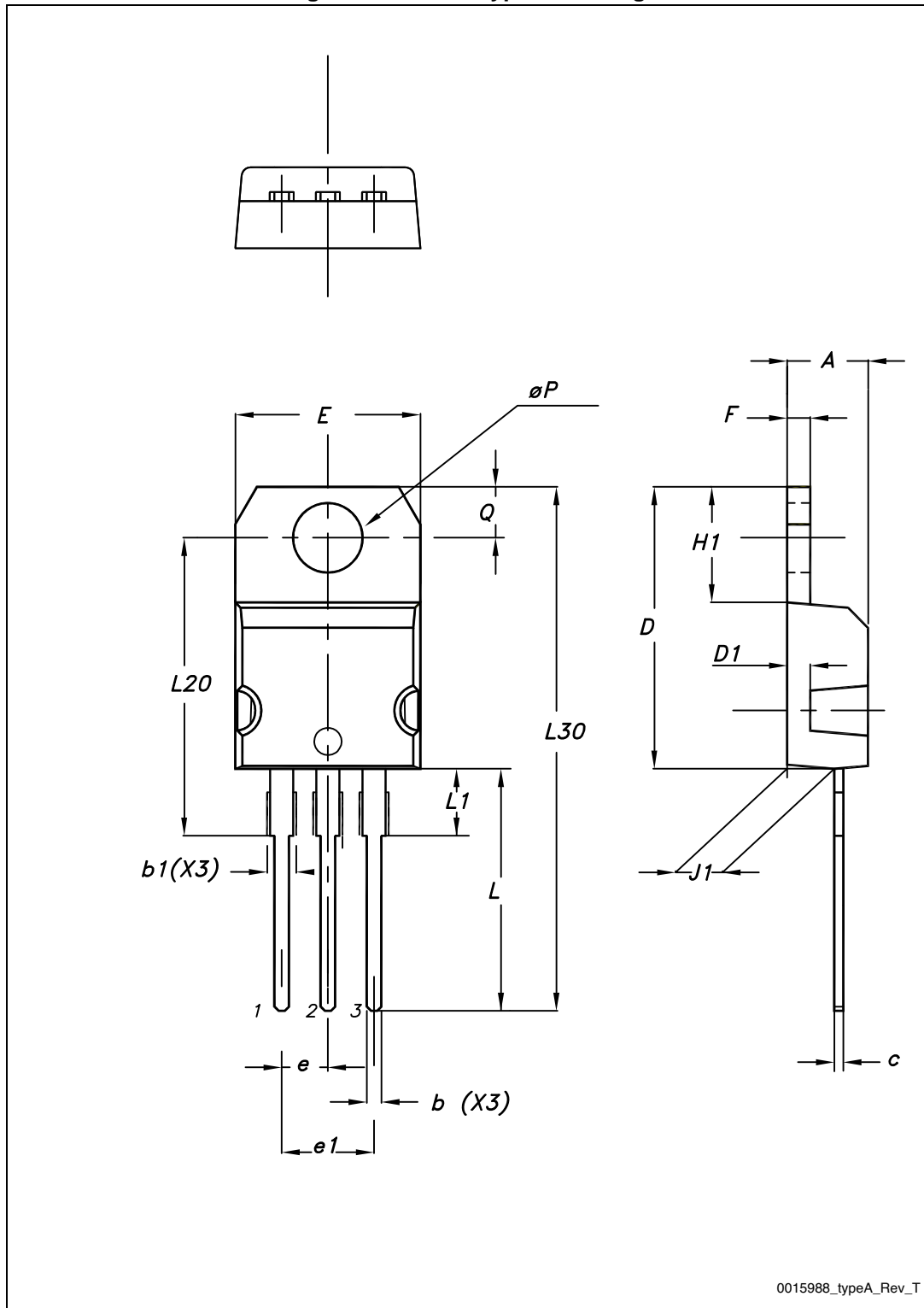


Table 11. TO-220 type A mechanical data

Dim.	mm		
	Min.	Typ.	Max.
A	4.40		4.60
b	0.61		0.88
b1	1.14		1.70
c	0.48		0.70
D	15.25		15.75
D1		1.27	
E	10		10.40
e	2.40		2.70
e1	4.95		5.15
F	1.23		1.32
H1	6.20		6.60
J1	2.40		2.72
L	13		14
L1	3.50		3.93
L20		16.40	
L30		28.90	
ØP	3.75		3.85
Q	2.65		2.95

Figure 28. TO-220 type A drawing



5 Packaging mechanical data

Table 12. DPAK (TO-252) tape and reel mechanical data

Tape			Reel		
Dim.	mm		Dim.	mm	
	Min.	Max.		Min.	Max.
A0	6.8	7	A		330
B0	10.4	10.6	B	1.5	
B1		12.1	C	12.8	13.2
D	1.5	1.6	D	20.2	
D1	1.5		G	16.4	18.4
E	1.65	1.85	N	50	
F	7.4	7.6	T		22.4
K0	2.55	2.75			
P0	3.9	4.1	Base qty.		2500
P1	7.9	8.1	Bulk qty.		2500
P2	1.9	2.1			
R	40				
T	0.25	0.35			
W	15.7	16.3			

Figure 29. Tape

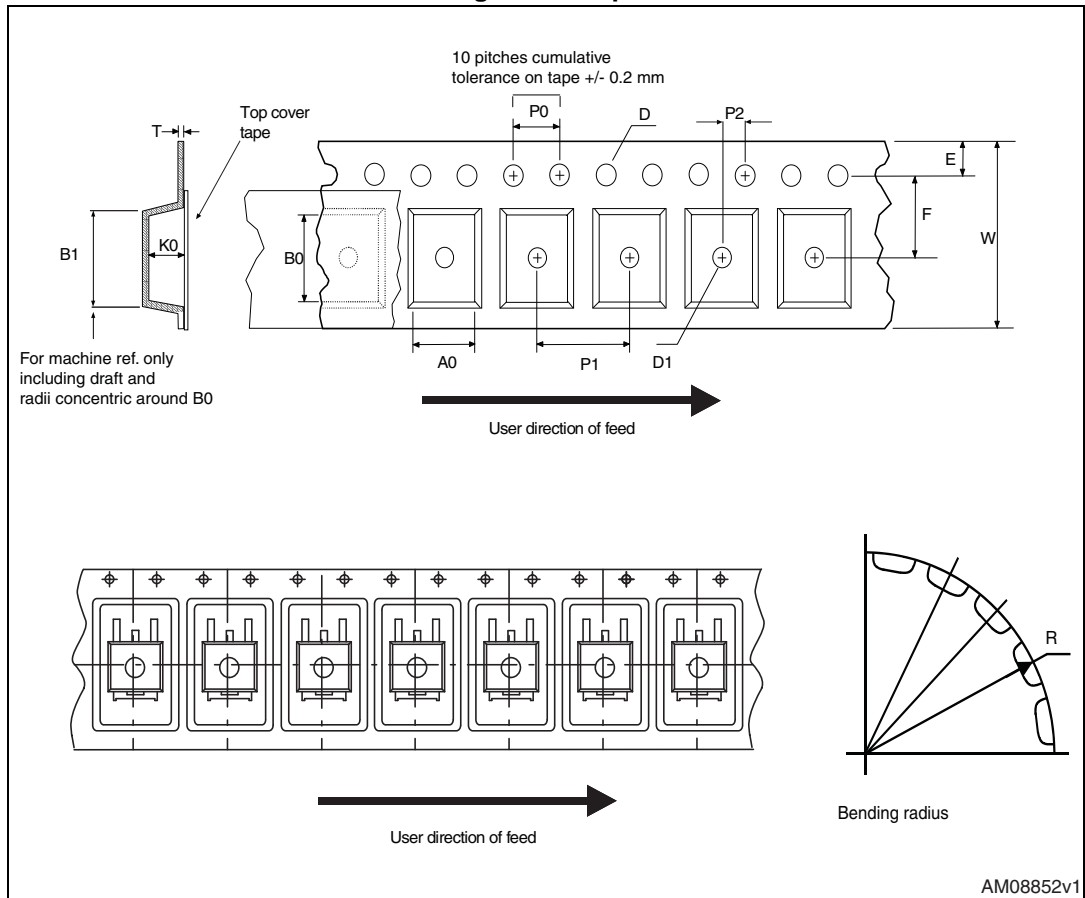
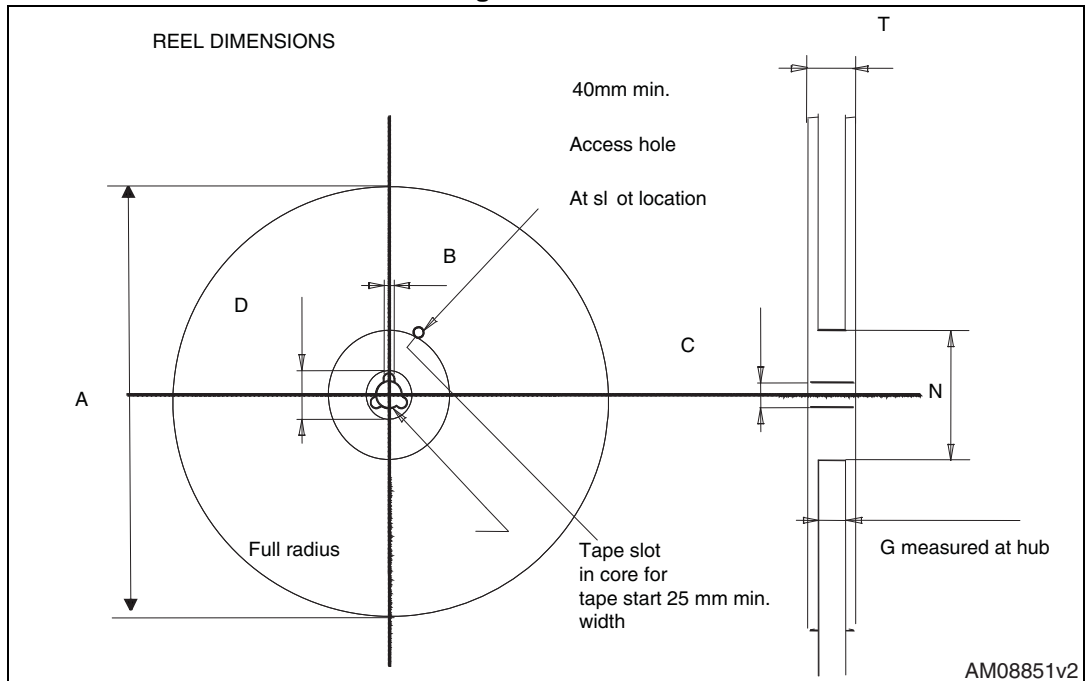


Figure 30. Reel



6 Revision history

Table 13. Document revision history

Date	Revision	Changes
01-Jun-2007	1	First release.
03-Oct-2007	2	Added device in D ² PAK and updated Figure 12: Capacitance variations
20-Jul-2012	3	Document status promoted from preliminary to production data. Updated Section 4: Package mechanical data and Section 5: Packaging mechanical data . Minor text changes.
15-Jul-2013	4	Updated Table 1: Device summary and Section 4: Package mechanical data .

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