

# DATA SHEET

## **PEMD6; PUMD6**

**NPN/PNP resistor-equipped  
transistors;**

**R1 = 4.7 k $\Omega$ , R2 = open**

Product data sheet  
Supersedes data of 2003 Nov 04

2004 Apr 07

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**FEATURES**

- Built-in bias resistors
- Simplified circuit design
- Reduction of component count
- Reduced pick and place costs.

**APPLICATIONS**

- Low current peripheral driver
- Replacement of general purpose transistors in digital applications
- Control of IC inputs.

**DESCRIPTION**

NPN/PNP resistor-equipped transistors (see “\_Data\_Sheet\_Remark Supersedes data of 2003 Nov 04” for package details).

**QUICK REFERENCE DATA**

SYMBOL	PARAMETER	TYP.	MAX.	UNIT
V <sub>CEO</sub>	collector-emitter voltage	–	50	V
I <sub>O</sub>	output current (DC)	–	100	mA
TR1	NPN	–	–	–
TR2	PNP	–	–	–
R1	bias resistor	4.7	–	kΩ
R2	open	–	–	–

**PRODUCT OVERVIEW**

TYPE NUMBER	PACKAGE		MARKING CODE	NPN/PNP COMPLEMENT	PNP/PNP COMPLEMENT
	PHILIPS	EIAJ			
PEMD6	SOT666	–	D6	PEMH7	PEMB3
PUMD6	SOT363	SC-88	D*6 <sup>(1)</sup>	PUMH7	PUMB3

**Note**

- \* = p: Made in Hong Kong.  
\* = t: Made in Malaysia.

**SIMPLIFIED OUTLINE, SYMBOL AND PINNING**

TYPE NUMBER	SIMPLIFIED OUTLINE AND SYMBOL	PINNING	
		PIN	DESCRIPTION
PEMD6; PUMD6	<p>Top view <span style="margin-left: 100px;">MHC028</span></p>	1	emitter TR1
		2	base TR1
		3	collector TR2
		4	emitter TR2
		5	base TR2
		6	collector TR1

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**ORDERING INFORMATION**

TYPE NUMBER	PACKAGE		
	NAME	DESCRIPTION	VERSION
PEMD6	–	plastic surface mounted package; 6 leads	SOT666
PUMD6	–	plastic surface mounted package; 6 leads	SOT363

**LIMITING VALUES**

In accordance with the Absolute Maximum Rating System (IEC 60134).

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
<b>Per transistor; for the PNP transistor with negative polarity</b>					
V <sub>CBO</sub>	collector-base voltage	open emitter	–	50	V
V <sub>CEO</sub>	collector-emitter voltage	open base	–	50	V
V <sub>EBO</sub>	emitter-base voltage	open collector	–	5	V
I <sub>O</sub>	output current (DC)		–	100	mA
I <sub>CM</sub>	peak collector current		–	100	mA
P <sub>tot</sub>	total power dissipation	T <sub>amb</sub> ≤ 25 °C; note 1			
	SOT363	note 1	–	200	mW
	SOT666	notes 1 and 2	–	200	mW
T <sub>stg</sub>	storage temperature		–65	+150	°C
T <sub>j</sub>	junction temperature		–	150	°C
T <sub>amb</sub>	operating ambient temperature		–65	+150	°C
<b>Per device</b>					
P <sub>tot</sub>	total power dissipation	T <sub>amb</sub> ≤ 25 °C; note 1			
	SOT363	note 1	–	300	mW
	SOT666	notes 1 and 2	–	300	mW

**Notes**

1. Transistor mounted on an FR4 printed-circuit board, single-sided copper, standard footprint.
2. Reflow soldering is the only recommended soldering method.

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### THERMAL CHARACTERISTICS

SYMBOL	PARAMETER	CONDITIONS	VALUE	UNIT
<b>Per transistor</b>				
R <sub>th(j-a)</sub>	thermal resistance from junction to ambient	note 1		
	SOT363		625	K/W
	SOT666		625	K/W
<b>Per device</b>				
R <sub>th(j-a)</sub>	thermal resistance from junction to ambient	note 1		
	SOT363		416	K/W
	SOT666		416	K/W

### Note

1. Transistor mounted on an FR4 printed-circuit board, single-sided copper, standard footprint.

### CHARACTERISTICS

T<sub>amb</sub> = 25 °C; unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
<b>Per transistor; for the PNP transistor with negative polarity</b>						
I <sub>CBO</sub>	collector-base cut-off current	V <sub>CB</sub> = 50 V; I <sub>E</sub> = 0	–	–	100	nA
I <sub>CEO</sub>	collector-emitter cut-off current	V <sub>CE</sub> = 30 V; I <sub>B</sub> = 0	–	–	1	$\mu$ A
		V <sub>CE</sub> = 30 V; I <sub>B</sub> = 0; T <sub>j</sub> = 150 °C	–	–	50	$\mu$ A
I <sub>EBO</sub>	emitter-base cut-off current	V <sub>EB</sub> = 5 V; I <sub>C</sub> = 0	–	–	100	nA
h <sub>FE</sub>	DC current gain	V <sub>CE</sub> = 5 V; I <sub>C</sub> = 1 mA	200	–	–	
V <sub>CEsat</sub>	collector-emitter saturation voltage	I <sub>C</sub> = 5 mA; I <sub>B</sub> = 0.25 mA	–	–	100	mV
R1	input resistor		3.3	4.7	6.1	k $\Omega$
C <sub>c</sub>	collector capacitance	I <sub>E</sub> = I <sub>e</sub> = 0; V <sub>CB</sub> = 10 V; f = 1 MHz				
	TR1 (NPN)		–	–	2.5	pF
	TR2 (PNP)	–	–	3	pF	

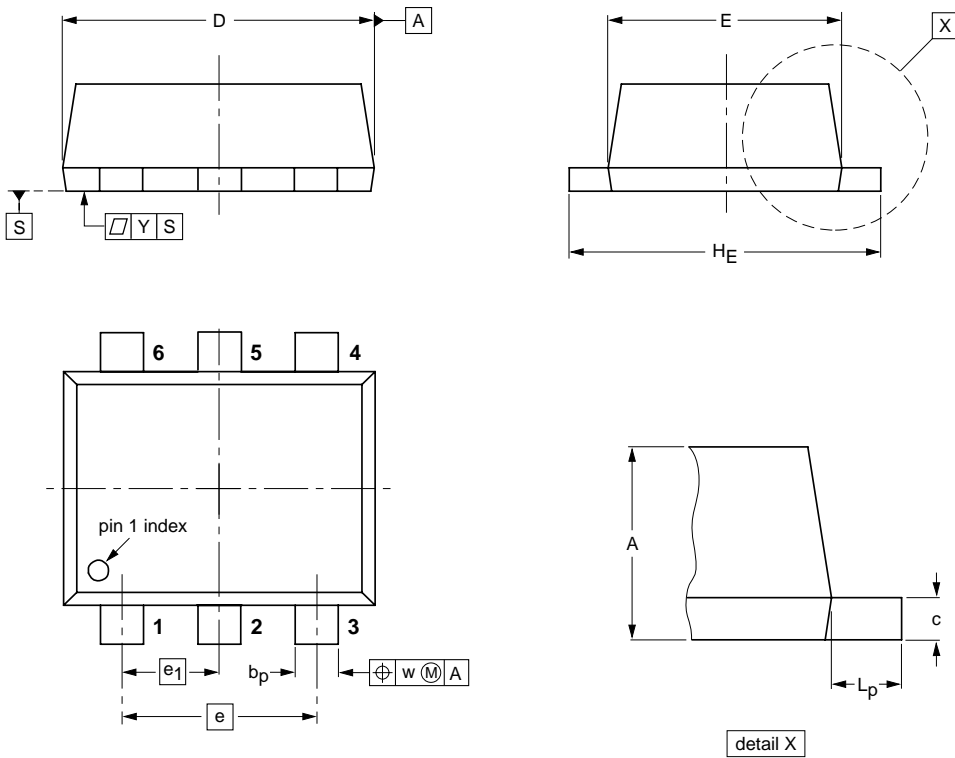
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PACKAGE OUTLINES

Plastic surface-mounted package; 6 leads

SOT666



DIMENSIONS (mm are the original dimensions)

UNIT	A	b <sub>p</sub>	c	D	E	e	e <sub>1</sub>	H <sub>E</sub>	L <sub>p</sub>	w	y
mm	0.6 0.5	0.27 0.17	0.18 0.08	1.7 1.5	1.3 1.1	1.0	0.5	1.7 1.5	0.3 0.1	0.1	0.1

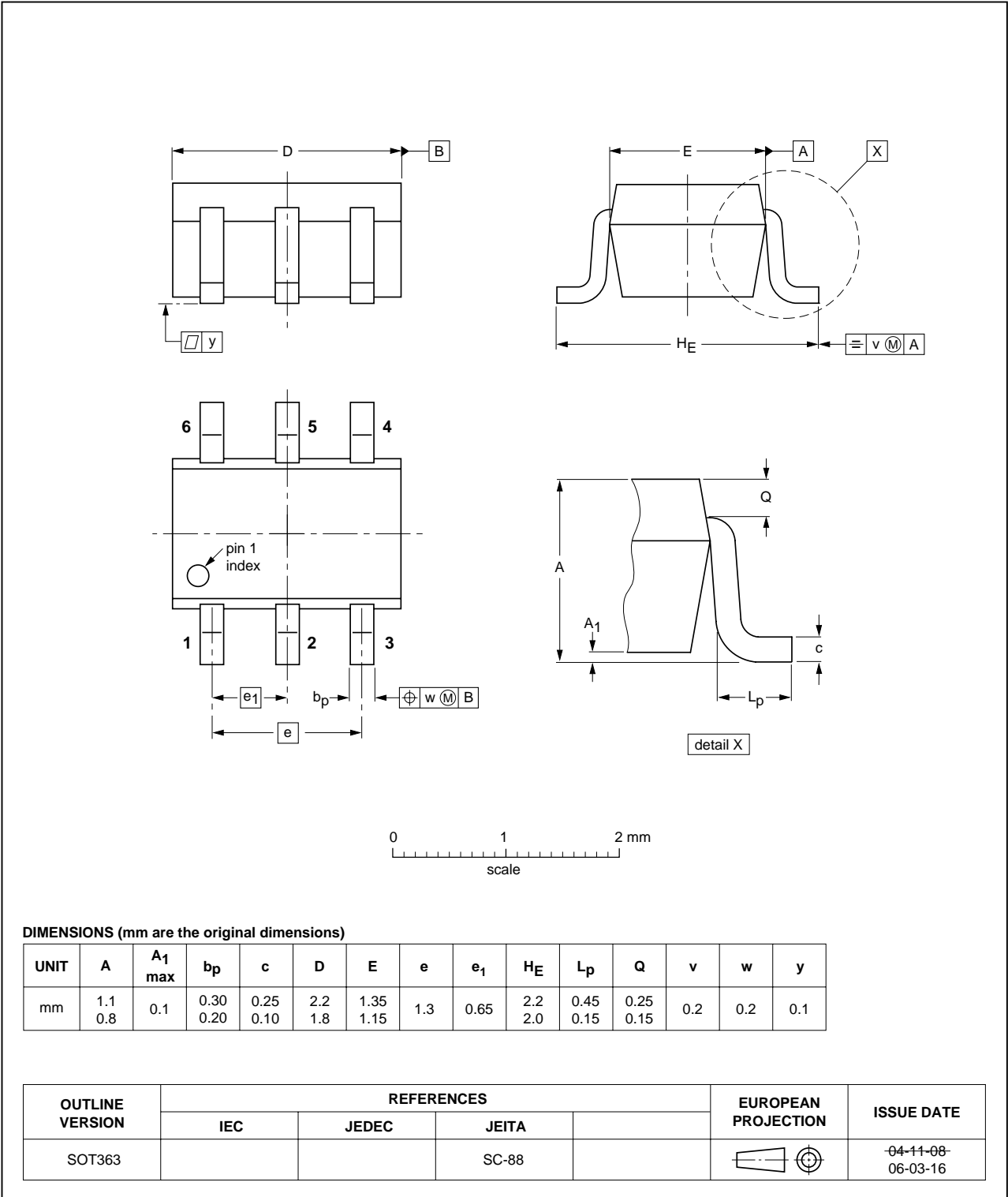
OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT666						04-11-08 06-03-16

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## DATA SHEET STATUS

DOCUMENT STATUS <sup>(1)</sup>	PRODUCT STATUS <sup>(2)</sup>	DEFINITION
Objective data sheet	Development	This document contains data from the objective specification for product development.
Preliminary data sheet	Qualification	This document contains data from the preliminary specification.
Product data sheet	Production	This document contains the product specification.

## Notes

1. Please consult the most recently issued document before initiating or completing a design.
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# ***NXP Semiconductors***

## **Customer notification**

This data sheet was changed to reflect the new company name NXP Semiconductors, including new legal definitions and disclaimers. No changes were made to the technical content, except for package outline drawings which were updated to the latest version.

## **Contact information**

For additional information please visit: <http://www.nxp.com>

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