3.3 V 2.7 Gb/s Limiting Amplifier

Data Sheet

ADN2890

FEATURES

SFP reference design available
Input sensitivity: 3 mV p-p
80 ps rise/fall times
CML outputs: 700 mV p-p differential
Programmable LOS detector: 2 mV to 13 mV
Rx signal strength indicator (RSSI):
SFF-8472 compliant average power measurement
Single-supply operation: 3.3 V
Low power dissipation: 130 mW
Available in space-saving 3 mm × 3 mm 16-lead LFCSP

APPLICATIONS

SFP/SFF/GBIC optical transceivers
OC-3/12/48, GbE, Fibre Channel receivers
10GBASE-LX4 transceivers
WDM transponders

GENERAL DESCRIPTION

The ADN2890 is a high gain, limiting amplifier optimized for use in SONET, Gigabit Ethernet (GbE), and Fibre Channel optical receivers that accept input levels of up to 2.0 V p-p differential and have 3 mV p-p differential input sensitivity. The ADN2890 provides the receiver functions of quantization and loss of signal (LOS) detection. The ADN2890 can easily operate at up to 3.2 Gb/s to support LX4 transceivers.

The limiting amplifier also measures average received power based on a direct measurement of the photodiode current with better than 1 dB of accuracy over the entire input range of the receiver. This eliminates the need for external average Rx power detection circuitry in SFF-8472 compliant optical transceivers.

The ADN2890 limiting amplifier operates from a single 3.3 V supply, has low power dissipation, and is available in a space-saving 3 mm × 3 mm 16-lead lead frame chip scale package (LFCSP).

FUNCTIONAL BLOCK DIAGRAM

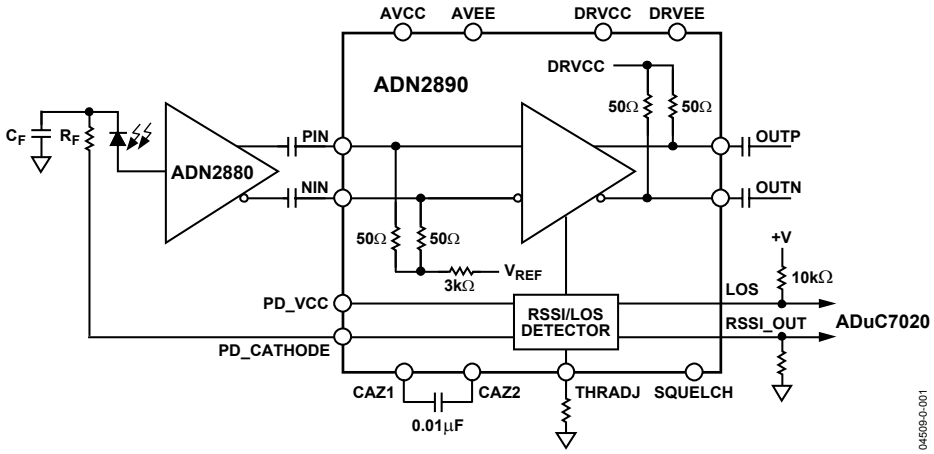

Figure 1.

Document Feedback

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REVISION HISTORY

4/2017—Rev. A to Rev. B

Changed CP-16-27 to CP-16-22 ..... Throughout
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10/2013—Rev. 0 to Rev. A

Change to Output Voltage Swing Parameter, Table 1 3
Change to Figure 2 6
Updated Outline Dimensions 11
Changes to Ordering Guide 11

5/2004—Revision 0: Initial Version

SPECIFICATIONS

VCC = V_{MIN} to V_{MAX}, VEE = 0 V, T_A = T_{MIN} to T_{MAX}, unless otherwise noted.

Table 1.

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
QUANTIZER DC CHARACTERISTICS					
Input Voltage Range	1.8		2.8	V p-p	At PIN or NIN, dc-coupled
Input Common Mode	2.1		2.7	V	DC-coupled
Peak-to-Peak Differential Input Range			2.0	V p-p	PIN − NIN, ac-coupled
Input Sensitivity	4	3		mV p-p	PIN − NIN, BER ≤ 1×10^{-10}
Input Offset Voltage		100		µV	
Input RMS Noise		235		µV rms	
Input Resistance		50		Ω	Single-ended
Input Capacitance		0.65		pF	
QUANTIZER AC CHARACTERISTICS					
Input Data Rate	155		2700	Mb/s	
Small Signal Gain		57		dB	Differential
S11		−10		dB	Differential, f < 2.7 GHz
S22		−10		dB	Differential, f < 2.7 GHz
Random Jitter		2.4	5	ps rms	Input ≥ 10 mV p-p, OC-48, PRBS $2^{23} - 1$
Deterministic Jitter		13.7	19	ps p-p	Input ≥ 10 mV p-p, OC-48, PRBS $2^{23} - 1$
Low Frequency Cutoff		30		kHz	CAZ = Open
		1.0		kHz	CAZ = 0.0 1 µF
Power Supply Rejection		45		dB	100 kHz < f < 10 MHz
LOSS OF SIGNAL DETECTOR (LOS)					
LOS Assert Level	0.5	2.5	4.0	mV p-p	R_{THRADJ} = 100 kΩ
	7.0	12.0	16.0	mV p-p	R_{THRADJ} = 0 Ω
Hysteresis		3.0	6.0	dB	OC-3, PRBS $2^{23} - 1$, R_{THRADJ} = 0 Ω
	2.0	3.0		dB	OC-3, PRBS $2^{23} - 1$, R_{THRADJ} = 10 kΩ
		4.5	7.5	dB	OC-48, PRBS $2^{23} - 1$, R_{THRADJ} = 0 Ω
	2.5	4.5		dB	OC-48, PRBS $2^{23} - 1$, R_{THRADJ} = 100 kΩ
LOS Assert Time		600		ns	DC-coupled
LOS De-Assert Time		100		ns	DC-coupled
RSSI					
Input Current Range	5		1000	µA	
RSSI Output Accuracy			15%		I_{IN} ≤ 20 µA
			10%		I_{IN} > 20 µA
Gain		1.0		mA/mA	I_{RSSI}/I_{PD}
Offset		50		nA	
Compliance Voltage	V_{CC} − 1.05		V_{CC} − 0.3	V	At PD_CATHODE
POWER SUPPLIES					
V_{CC}	3.0	3.3	3.6	V	
I_{CC}		39	54	mA	
OPERATING TEMPERATURE RANGE	−40	+25	+85	°C	T_{MIN} to T_{MAX}
CML OUTPUT CHARACTERISTICS					
Output Impedance		50		Ω	Single-ended
Output Voltage Swing	650	700	800	mV p-p	Differential
Output Rise and Fall Time		80	100	ps	20% to 80%

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
LOGIC INPUTS (SQUELCH)					
V_{IH}, Input High Voltage	2.0			V	
V_{IL}, Input Low Voltage			0.8	V	
Input Current	−100			nA	I_{INH}, V_{IN} = 2.4 V
			100	nA	I_{INL}, V_{IN} = 0.4 V
LOGIC OUTPUTS (LOS)					
V_{OH}, Output High Voltage	2.4			V	Open drain output, 4.7 kΩ – 10 kΩ pull-up resistor to V_{CC}
V_{OL}, Output Low Voltage			0.4	V	Open drain output, 4.7 kΩ – 10 kΩ pull-up resistor to V_{CC}

ABSOLUTE MAXIMUM RATINGS

Table 2.

Parameter	Rating
Supply Voltage	4.2 V
Minimum Input Voltage (All Inputs)	VEE − 0.4 V
Maximum Input Voltage (All Inputs)	VCC + 0.4 V
Storage Temperature	−65°C to +155°C
Operating Temperature Range	−40°C to +85°C
Lead Temperature Range (Soldering 10 s)	300°C
Junction Temperature	125°C

Stresses at or above those listed under Absolute Maximum Ratings may cause permanent damage to the product. This is a stress rating only; functional operation of the product at these or any other conditions above those indicated in the operational section of this specification is not implied. Operation beyond the maximum operating conditions for extended periods may affect product reliability.

THERMAL RESISTANCE

θ_{JA} is specified for 4-layer PCB with exposed paddle soldered to GND.

Table 3.

Package Type	θ_{JA}	Unit
16-Lead 3 mm × 3 mm LFCSP	28	°C/W

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

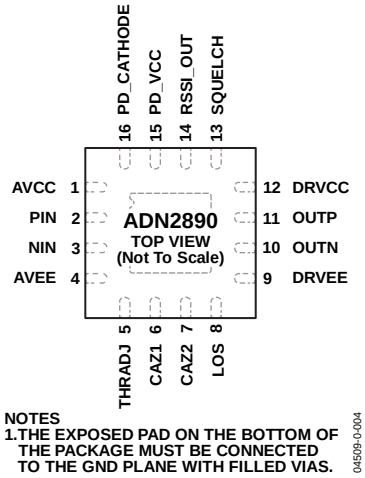

Figure 2. Pin Configuration

Table 4. Pin Function Descriptions

Pin No.	Mnemonic	I/O	Description
1	AVCC	Power	Analog Power
2	PIN	Input	Differential Data Input
3	NIN	Input	Differential Data Input
4	AVEE	Power	Analog Ground
5	THRADJ	Input	LOS Threshold Adjust Resistor
6	CAZ1		Offset Correction Loop Capacitor
7	CAZ2		Offset Correction Loop Capacitor
8	LOS	Output	LOS Detector Output
9	DRVEE	Power	Output Buffer Ground
10	OUTN	Output	Differential Data Output
11	OUTP	Output	Differential Data Output
12	DRVCC	Power	Output Buffer Power
13	SQUELCH	Input	Disable Outputs
14	RSSI_OUT	Output	Average Current Output
15	PD_VCC	Power	Power Input for RSSI Measurement
16	PD_CATHODE	Output	Photodiode Bias Voltage
Exposed Pad	Pad	Power	Connect to Ground

TYPICAL PERFORMANCE CHARACTERISTICS

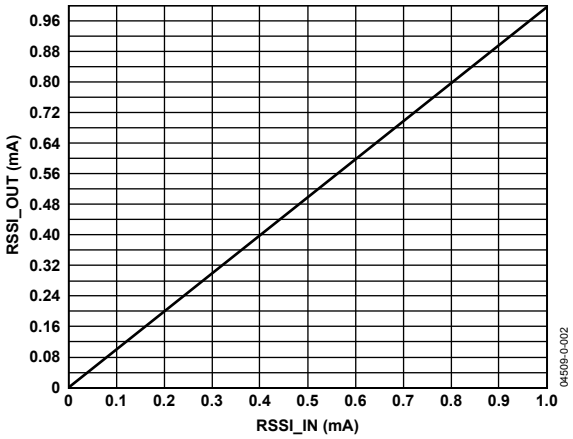

Figure 3. RSSI Output vs. Average PIN Photodiode Current

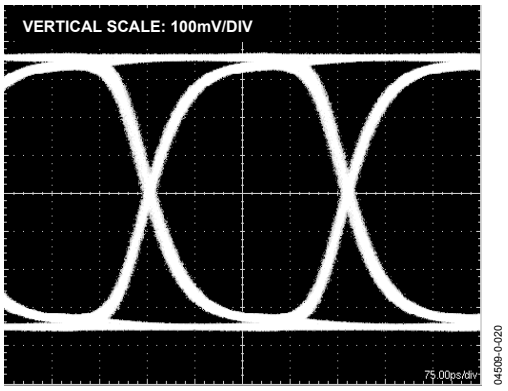

Figure 6. Eye Diagram at 3.2 Gb/s

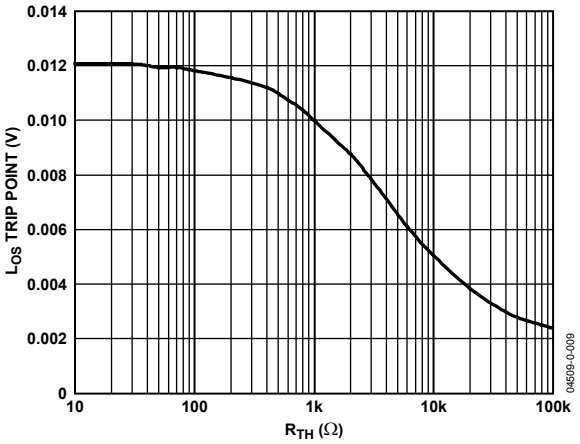

Figure 4. L_{OS} Trip Point vs. Threshold Adjust Resistor

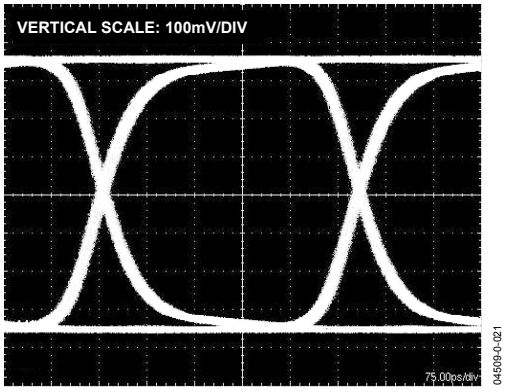

Figure 7. Eye Diagram at 2.488 Gb/s

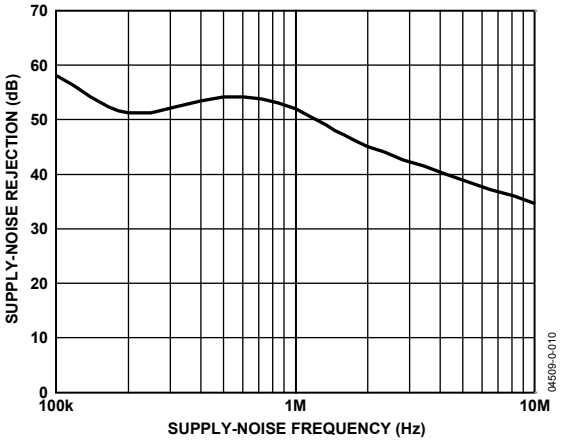

Figure 5. Typical PSRR vs. Supply-Noise Frequency

THEORY OF OPERATION

LIMAMP

Input Buffer

The limiting amplifier has differential inputs (PIN/NIN), with an internal 50 Ω termination. The ROSA (receive optical subassembly) is typically ac-coupled to the ADN2890 inputs, although dc coupling is possible.

An internal offset correction loop requires that a capacitor be connected between the CAZ1 and CAZ2 pins. A 0.01 µF capacitor provides a low frequency cutoff of 2 kHz.

CML Output Buffer

The ADN2890 provides CML outputs, OUTP/OUTN. The outputs are internally terminated with 50 Ω to VCC.

The outputs can be kept at a static voltage by driving the SQUELCH pin to a logic high. The SQUELCH pin can be driven directly by the LOS pin, which automatically disables the LIMAMP outputs in situations with no data input.

LOSS OF SIGNAL (LOS) DETECTOR

The receiver front-end LOS detector circuit indicates when the input signal level has fallen below the user-adjustable threshold. The threshold is set by a resistor connected between the THRADJ pin and V_{EE}. The ADN2890 LOS circuit has a trip point down to <3.0 mV with >3 dB electrical hysteresis to prevent chatter at the LOS output. The LOS output is an open-collector output that must be pulled up externally with a 4.7 kΩ to 10 kΩ resistor.

RECEIVED SIGNAL STRENGTH INDICATOR (RSSI)

The ADN2890 has an on-chip RSSI circuit that automatically detects the average received power based on a direct measurement of the PIN photodiode's current. The photodiode bias is supplied by the ADN2890, which allows a very accurate, on-chip, average power measurement based on the amount of current supplied to the photodiode. The output of the RSSI is a current that is directly proportional to the average amount of PIN photodiode current. Placing a resistor between the RSSI_OUT pin and GND converts the current to a GND referenced voltage. This function eliminates the need for external RSSI circuitry in SFF-8472 compliant optical receivers.

SQUELCH MODE

Driving the SQUELCH input to a logic high disables the limiting amplifier outputs. The SQUELCH input can be connected to the LOS output to keep the limiting amplifier outputs at a static voltage level anytime the input level to the limiting amplifier drops below the programmed LOS threshold.

APPLICATIONS INFORMATION

PCB DESIGN GUIDELINES

Proper RF PCB design techniques must be used for optimal performance.

Power Supply Connections and Ground Planes

Use of one low impedance ground plane is recommended. The VEE pins should be soldered directly to the ground plane to reduce series inductance. If the ground plane is an internal plane and connections to the ground plane are made through vias, multiple vias can be used in parallel to reduce the series inductance, especially on Pin 9, which is the ground return for the output buffers. The exposed pad should be connected to the GND plane using filled vias so that solder does not leak through the vias during reflow. Using filled vias under the package greatly enhances the reliability of the connectivity of the exposed pad to the GND plane during reflow.

Use of a 10 µF electrolytic capacitor between VCC and VEE is recommended at the location where the 3.3 V supply enters the PCB. When using 0.1 µF and 1 nF ceramic chip capacitors, they should be placed between the IC power supply VCC and VEE, as close as possible to the ADN2890 VCC pins.

If connections to the supply and ground are made through vias, the use of multiple vias in parallel helps to reduce series inductance, especially on Pin 12, which supplies power to the high speed OUTP/OUTN output buffers. Refer to the schematic in Figure 8 for recommended connections.

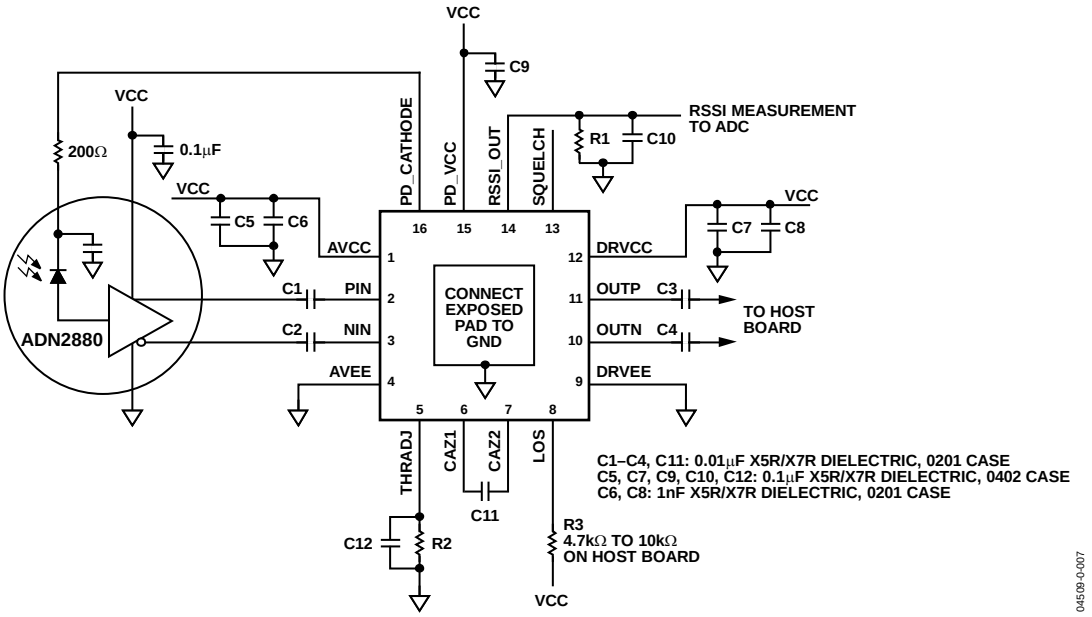

Figure 8. Typical ADN2890 Applications Circuit

PCB Layout

Figure 9 shows a recommended PC board layout. Use of 50 Ω transmission lines is required for all high frequency input and output signals to minimize reflections: PIN, NIN, OUTP and OUTN. It is also necessary for the PIN/NIN input traces to be matched in length, and OUTP/OUTN output traces to be matched in length to avoid skew between the differential traces. C1, C2, C3, and C4 are ac-coupling capacitors in series with the high speed I/O. It is recommended that components be used such that the pad for the capacitor is the same width as the transmission line in order to minimize the mismatch in the 50 Ω transmission line at the capacitor's pads. It is recommended that the transmission lines not change layers through vias, if possible. For supply decoupling, the 1 nF decoupling capacitor should be placed on the same layer as the ADN2890 as close as possible to the VCC pin. The 0.1 µF capacitor can be placed on the bottom of the PCB directly underneath the 1 nF decoupling capacitor. All high speed CML outputs are back-terminated on chip with 50 Ω resistors connected between the output pin and VCC. The high speed inputs, PIN and NIN, are internally terminated with 50 Ω to an internal reference voltage.

As with any high speed mixed-signal design, take care to keep all high speed digital traces away from sensitive analog nodes.

Soldering Guidelines for Chip Scale Package

The lands on the 16 LFCSP are rectangular. The printed circuit board pad for these should be 0.1 mm longer than the package land length and 0.05 mm wider than the package land width. The land should be centered on the pad. This ensures that the solder joint size is maximized. The bottom of the chip scale package has a central exposed pad. The pad on the printed circuit board should be at least as large as this exposed pad. The user must connect the exposed pad to VEE using filled vias so that solder does not leak through the vias during reflow. This ensures a solid connection from the exposed pad to VEE.

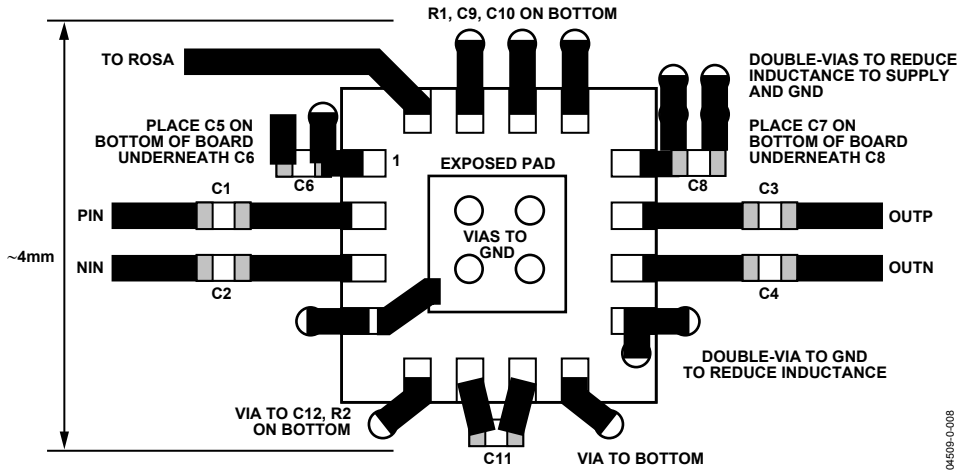

Figure 9. Recommended ADN2890 PCB Layout

OUTLINE DIMENSIONS

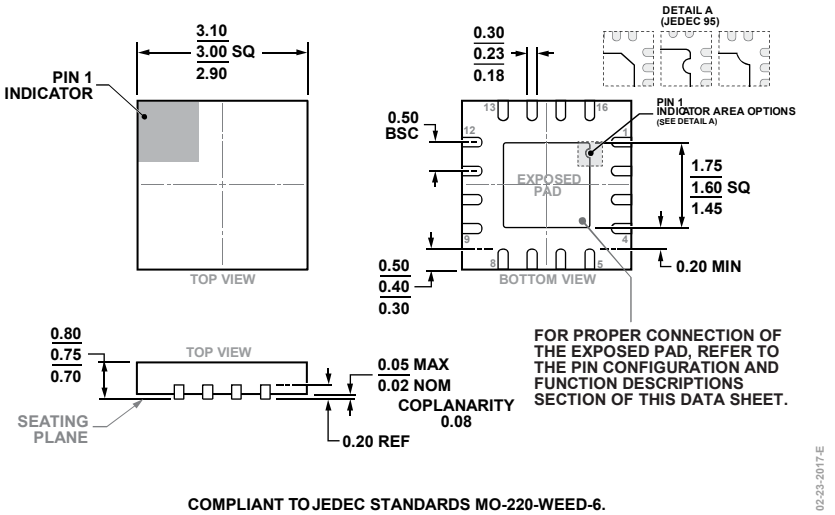

Figure 10. 16-Lead Lead Frame Chip Scale Package [LFCSP]
3 mm × 3 mm Body and 0.75 mm Package Height
(CP-16-22)
Dimensions shown in millimeters

ORDERING GUIDE

Model[1]	Temperature Range	Package Description	Package Option
ADN2890ACPZ-RL	–40°C to +85°C	16-Lead Lead Frame Chip Scale Package [LFCSP]	CP-16-22
ADN2890ACPZ-RL7	–40°C to +85°C	16-Lead Lead Frame Chip Scale Package [LFCSP]	CP-16-22
ADN2890-EVALZ		Evaluation Board	

[1] Z = RoHS Compliant Part.

NOTES

D04509-0-4/17(B)