NCV4266

Regulator with Enable, 150 mA, Low-Dropout Voltage

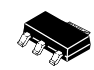
ON Semiconductor®

www.onsemi.com

The NCV4266 is a 150 mA output current integrated low dropout regulator family designed for use in harsh automotive environments. It includes wide operating temperature and input voltage ranges. The device is offered with fixed voltage versions of 3.3 V and 5.0 V available in 2% output voltage accuracy. It has a high peak input voltage tolerance and reverse input voltage protection. It also provides overcurrent protection, overtemperature protection and enable function for control of the state of the output voltage. The NCV4266 is available in SOT−223 surface mount package. The output is stable over a wide output capacitance and ESR range. The NCV4266 has improved startup behavior during input voltage transients.

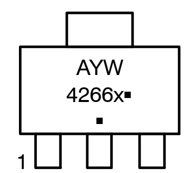
Features

- 3.3 V and 5.0 V Output Voltage
- 150 mA Output Current
- 500 mV (max) Dropout Voltage
- Enable Input
- Very Low Current Consumption
- Fault Protection
  - +45 V Peak Transient Voltage
  - −42 V Reverse Voltage
  - Short Circuit
  - Thermal Overload
- NCV Prefix for Automotive and Other Applications Requiring Unique Site and Control Change Requirements; AEC−Q100 Qualified and PPAP Capable
- These are Pb−Free Devices



SOT−223
ST SUFFIX
CASE 318E

MARKING DIAGRAM



A	= Assembly Location
Y	= Year
W	= Work Week
x	= Voltage Option
	3.3 V (x = 3)
	5.0 V (x = 5)
▪	= Pb−Free Package

(Note: Microdot may be in either location)

ORDERING INFORMATION

See detailed ordering and shipping information in the ordering information section on page 10 of this data sheet.

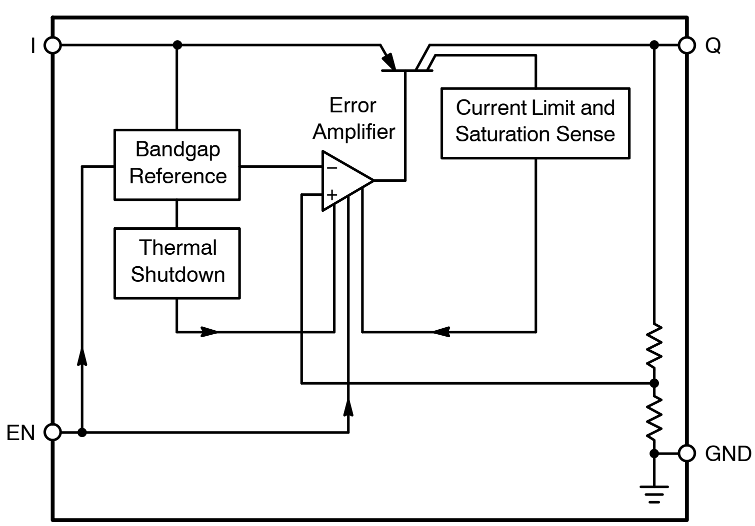


Figure 1. Block Diagram

November, 2018 − Rev. 3

Publication Order Number:
NCV4266/D

PIN FUNCTION DESCRIPTION

Pin No.	Symbol	Description
1	I	Input; Battery Supply Input Voltage.
2	EN	Enable Input; low level disables the IC.
3	Q	Output; Bypass with a capacitor to GND.
4	GND	Ground.

MAXIMUM RATINGS*

Rating	Symbol	Min	Max	Unit
Input Voltage	V_I	−42	45	V
Input Peak Transient Voltage	V_I	–	45	V
Enable Input Voltage	V_{EN}	−42	45	V
Output Voltage	V_Q	−1.0	40	V
Ground Current	I_q	–	100	mA
Input Voltage Operating Range	V_I	V_Q + 0.5 V or 4.5 (Note 1)	40	V
ESD Susceptibility (Human Body Model) (Machine Model)	– –	4.0 250	– –	kV V
Junction Temperature	T_J	−40	150	°C
Storage Temperature	T_{stg}	−50	150	°C

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

*During the voltage range which exceeds the maximum tested voltage of I, operation is assured, but not specified. Wider limits may apply. Thermal dissipation must be observed closely.

1. Minimum V_I = 4.5 V or (V_Q + 0.5 V), whichever is higher.

LEAD TEMPERATURE SOLDERING REFLOW AND MSL (Note 2)

Rating	Symbol	Min	Max	Unit
Lead Temperature Soldering Reflow (SMD styles only), Leaded, 60−150 s above 183, 30 s max at peak Reflow (SMD styles only), Free, 60−150 s above 217, 40 s max at peak Wave Solder (through hole styles only), 12 sec max	T_{SLD}	 – – –	 240 265 310	°C
Moisture Sensitivity Level	MSL	3		–

2. Per IPC / JEDEC J−STD−020C.

THERMAL CHARACTERISTICS

Characteristic	Test Conditions (Typical Value)		Unit
	Min Pad Board (Note 3)	**1″ Pad Board** (Note 4)	
Junction−to−Tab (psi−JL4, ψ_{JL4})	15.7	18	C/W
Junction−to−Ambient ($R_{\theta JA}$, θ_{JA})	96	77	C/W

3. 1 oz. copper, 0.26 inch^2 (168 mm^2) copper area, 0.062″ thick FR4.
4. 1 oz. copper, 1.14 inch^2 (736 mm^2) copper area, 0.062″ thick FR4.

ELECTRICAL CHARACTERISTICS (V_I = 13.5 V; −40°C < T_J < 150°C; unless otherwise noted.)

Characteristic	Symbol	Test Conditions	Min	Typ	Max	Unit
OUTPUT						
Output Voltage (5.0 V Version)	V_Q	5.0 mA < I_Q < 150 mA, 6 V < V_I < 28 V	4.9	5.0	5.1	V
Output Voltage (3.3 V Version)	V_Q	5.0 mA < I_Q < 150 mA, 4.5 V < V_I < 28 V	3.234	3.3	3.366	V
Output Current Limitation	I_Q	V_Q = 90% V_{QTYP}	150	200	500	mA
Quiescent Current (Sleep Mode) $I_q = I_I - I_Q$	I_q	V_{EN} = 0 V	–	–	10	μA
Quiescent Current, $I_q = I_I - I_Q$	I_q	I_Q = 1.0 mA	–	130	200	μA
Quiescent Current, $I_q = I_I - I_Q$	I_q	I_Q = 150 mA	–	10	15	mA
Dropout Voltage (5.0 V Version)	V_{DR}	I_Q = 150 mA, $V_{DR} = V_I - V_Q$ (Note 5)	–	250	500	mV
Load Regulation	$\Delta V_{Q,LO}$	I_Q = 5.0 mA to 150 mA	–	3.0	20	mV
Line Regulation (5.0 V Version)	ΔV_Q	ΔV_I = 6.0 V to 28 V, I_Q = 5.0 mA	–	10	25	mV
Line Regulation (3.3 V Version)	ΔV_Q	ΔV_I = 4.5 V to 28 V, I_Q = 5.0 mA	–	10	25	mV
Power Supply Ripple Rejection	PSRR	f_r = 100 Hz, V_r = 0.5 V_{PP}	–	70	–	dB
Temperature Output Voltage Drift	$d_{VQ/dT}$	–	–	0.5	–	mV/K
ENABLE INPUT						
Enable Voltage, Output High	V_{EN}	$V_Q \geq V_{QMIN}$	–	2.3	2.8	V
Enable Voltage, Output Low (Off)	V_{EN}	$V_Q \leq$ 0.1 V	1.8	2.2	–	V
Enable Input Current	I_{EN}	V_{EN} = 5.0 V	5.0	10	20	μA
THERMAL SHUTDOWN						
Thermal Shutdown Temperature*	T_{SD}		150	–	210	°C

*Guaranteed by design, not tested in production.
5. Measured when the output voltage V_Q has dropped 100 mV from the nominal value obtained at V = 13.5 V.

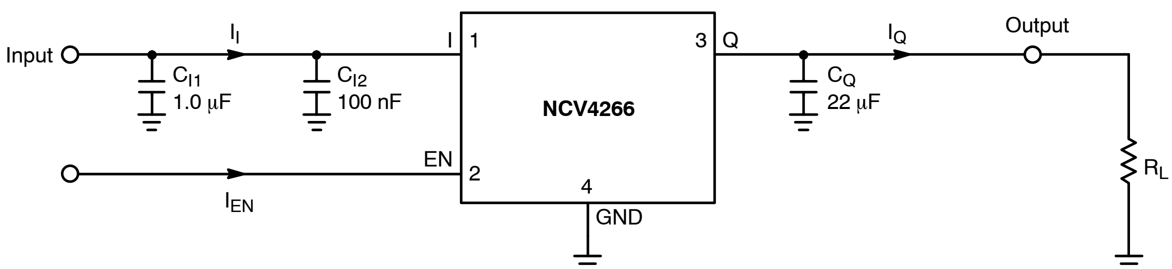


Figure 2. Applications Circuit

TYPICAL PERFORMANCE CHARACTERISTICS

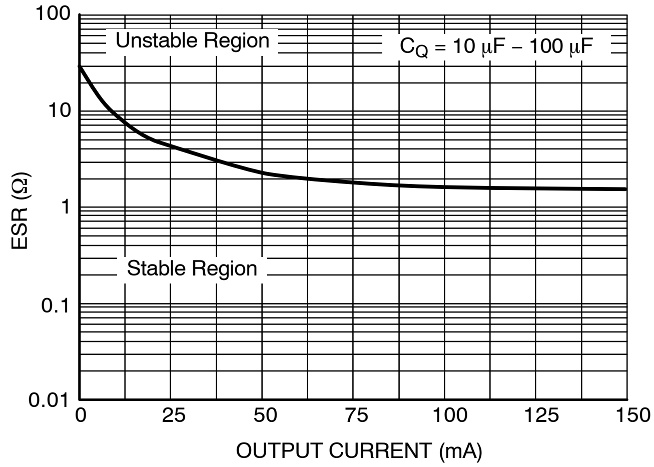


Figure 3. Output Stability with Output Capacitor ESR

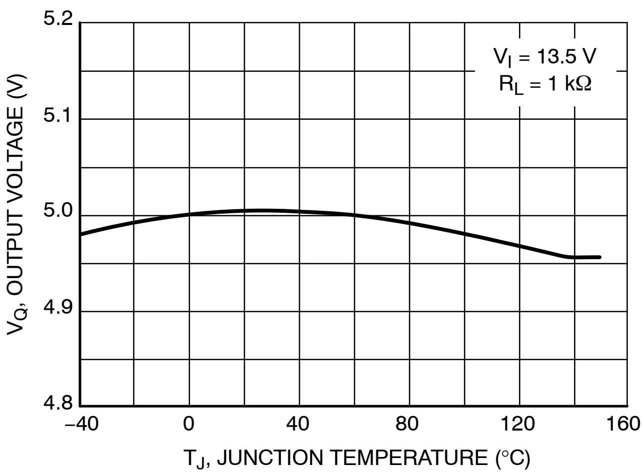


Figure 4. Output Voltage vs. Junction Temperature, 5.0 V Version

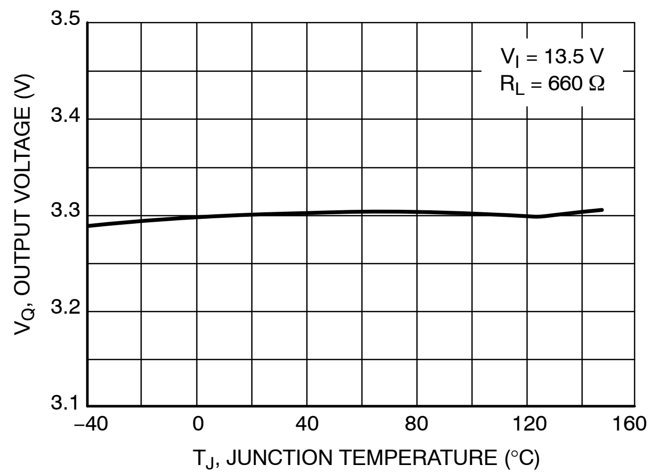


Figure 5. Output Voltage vs. Junction Temperature, 3.3 V Version

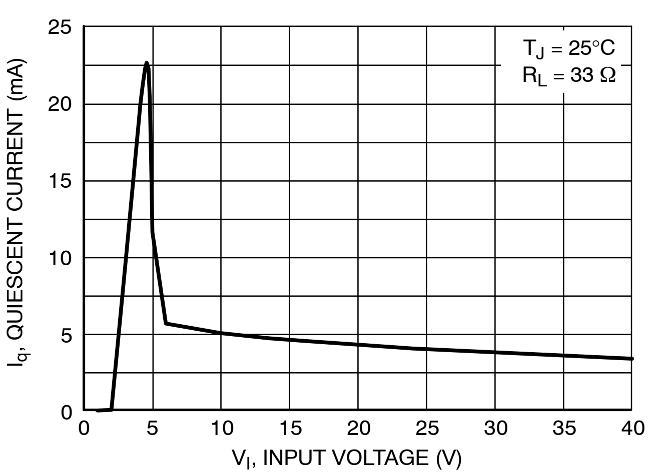


Figure 6. Quiescent Current vs. Input Voltage, 5.0 V Version

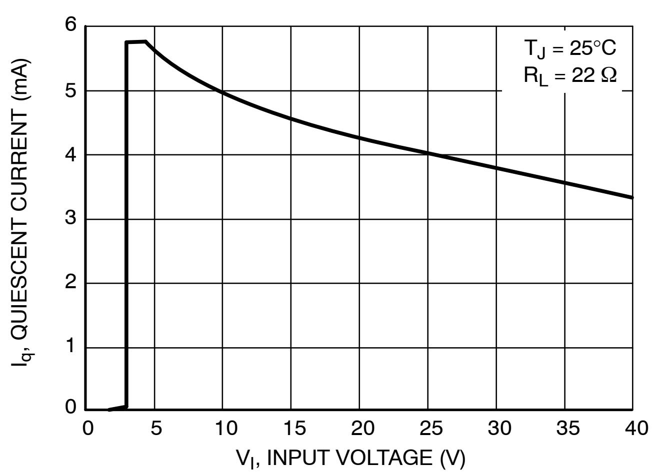


Figure 7. Quiescent Current vs. Input Voltage, 3.3 V Version

TYPICAL PERFORMANCE CHARACTERISTICS

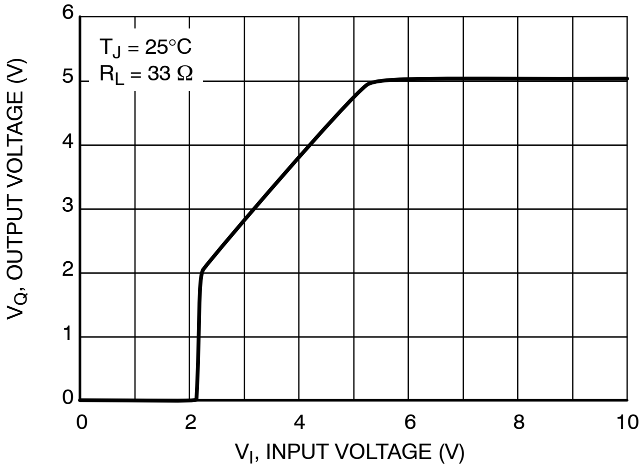


Figure 8. Output Voltage vs. Input Voltage, 5.0 V Version

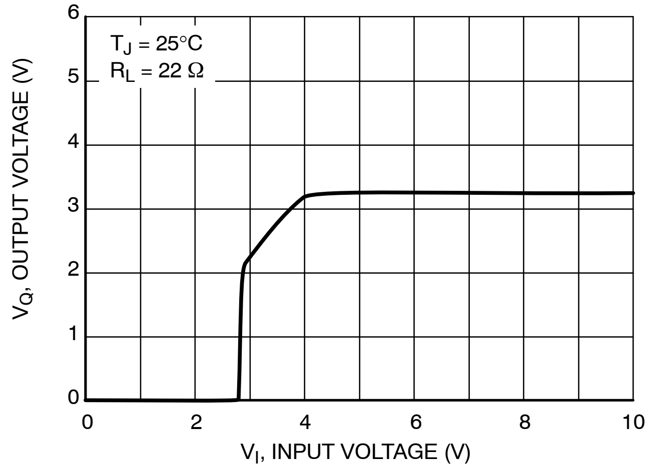


Figure 9. Output Voltage vs. Input Voltage, 3.3 V Version

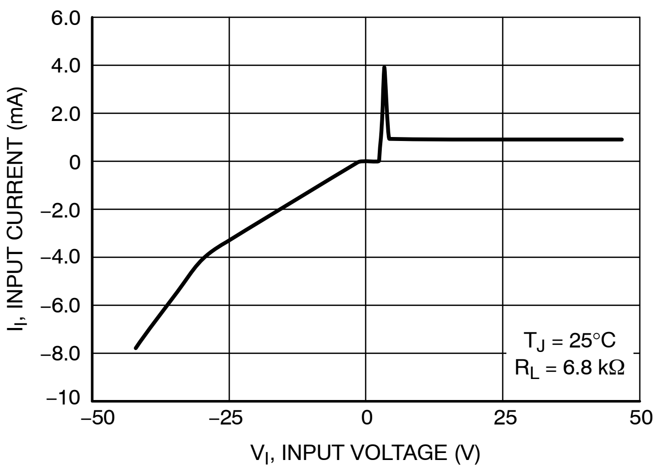


Figure 10. Input Current vs. Input Voltage, 5.0 V Version

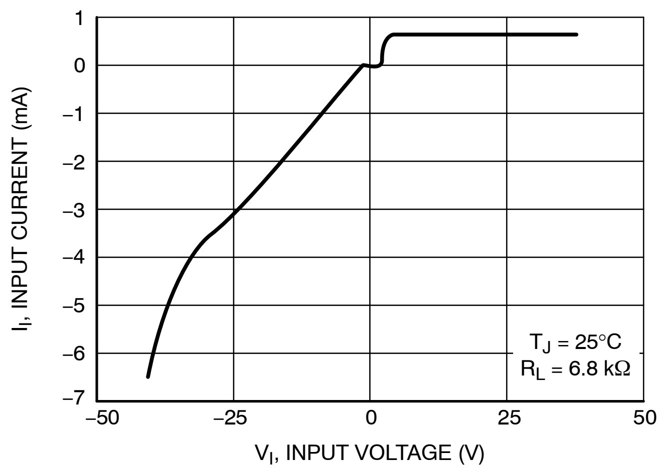


Figure 11. Input Current vs. Input Voltage, 3.3 V Version

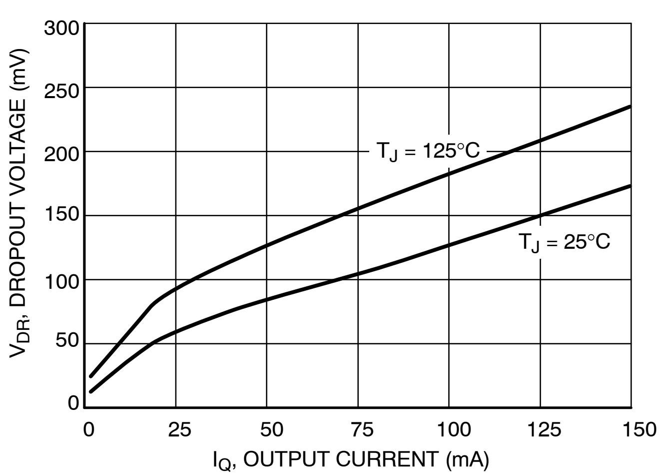


Figure 12. Dropout Voltage vs. Output Current (5.0 V Version only)

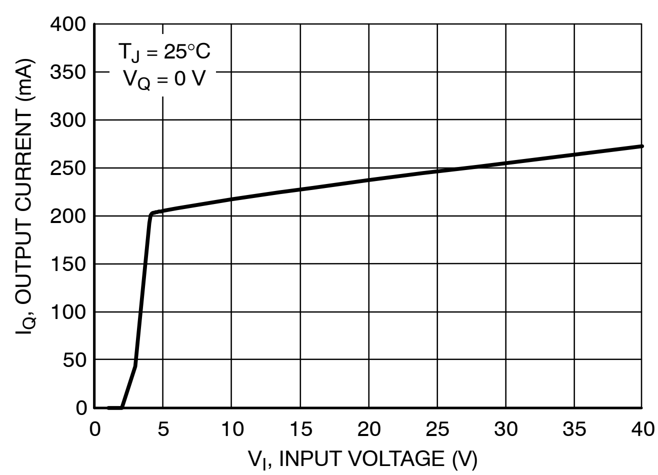


Figure 13. Maximum Output Current vs. Input Voltage

TYPICAL PERFORMANCE CHARACTERISTICS

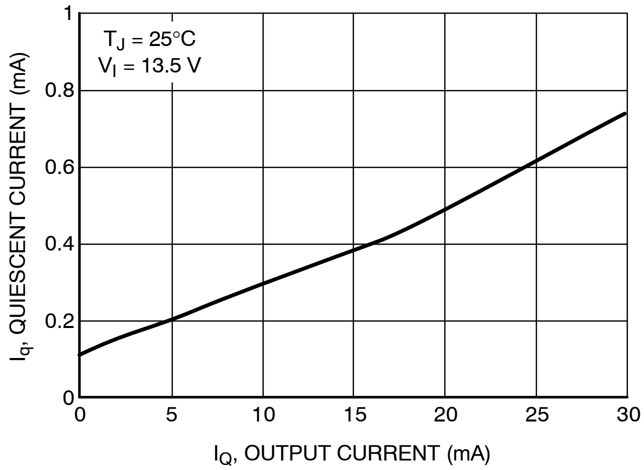


Figure 14. Quiescent Current vs. Output Current (Low Load), 5.0 V Version

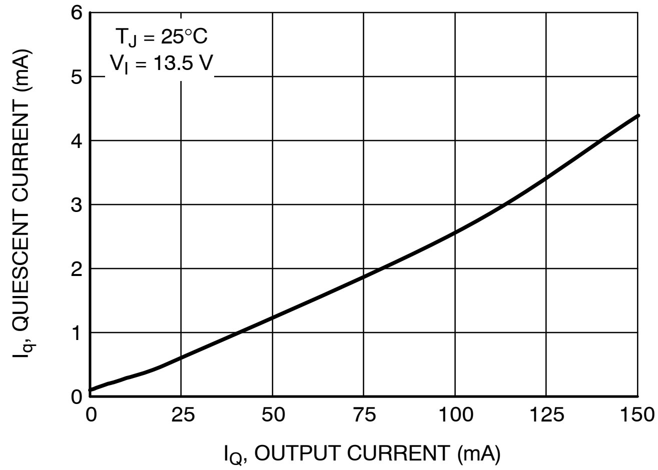


Figure 15. Quiescent Current vs. Output Current (High Load), 5.0 V Version

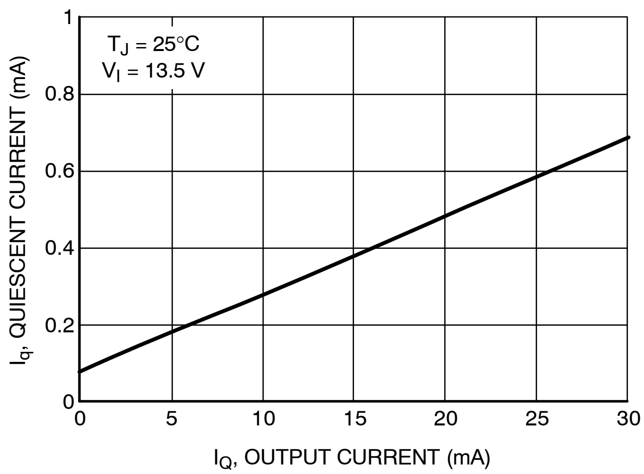


Figure 16. Quiescent Current vs. Output Current (Low Load), 3.3 V Version

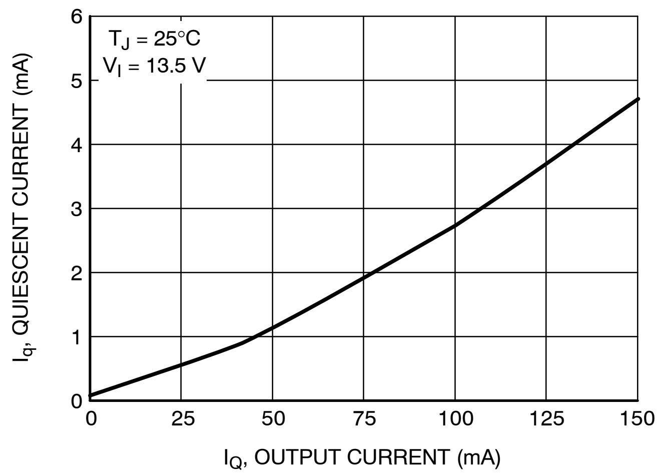


Figure 17. Quiescent Current vs. Output Current (High Load), 3.3 V Version

Circuit Description

The NCV4266 is an integrated low dropout regulator that provides a regulated voltage at 150 mA to the output. It is enabled with an input to the enable pin. The regulator voltage is provided by a PNP pass transistor controlled by an error amplifier with a bandgap reference, which gives it the lowest possible dropout voltage. The output current capability is 150 mA, and the base drive quiescent current is controlled to prevent oversaturation when the input voltage is low or when the output is overloaded. The regulator is protected by both current limit and thermal shutdown. Thermal shutdown occurs above 150°C to protect the IC during overloads and extreme ambient temperatures.

Regulator

The error amplifier compares the reference voltage to a sample of the output voltage (V_Q) and drives the base of a PNP series pass transistor via a buffer. The reference is a bandgap design to give it a temperature−stable output. Saturation control of the PNP is a function of the load current and input voltage. Oversaturation of the output power device is prevented, and quiescent current in the ground pin is minimized. See Figure 2, Test Circuit, for circuit element nomenclature illustration.

Regulator Stability Considerations

The input capacitors (C_{I1} and C_{I2}) are necessary to stabilize the input impedance to avoid voltage line influences. Using a resistor of approximately 1.0 Ω in series with C_{I2} can stop potential oscillations caused by stray inductance and capacitance.

The output capacitor helps determine three main characteristics of a linear regulator: startup delay, load transient response and loop stability. The capacitor value and type should be based on cost, availability, size and temperature constraints. The aluminum electrolytic capacitor is the least expensive solution, but, if the circuit operates at low temperatures (−25°C to −40°C), both the value and ESR of the capacitor will vary considerably. The capacitor manufacturer's data sheet usually provides this information.

The value for the output capacitor C_Q, shown in Figure 2, should work for most applications; see also Figure 3 for output stability at various load and Output Capacitor ESR conditions. Stable region of ESR in Figure 3 shows ESR values at which the LDO output voltage does not have any permanent oscillations at any dynamic changes of output load current. Marginal ESR is the value at which the output voltage waving is fully damped during four periods after the load change and no oscillation is further observable.

ESR characteristics were measured with ceramic capacitors and additional series resistors to emulate ESR. Low duty cycle pulse load current technique has been used to maintain junction temperature close to ambient temperature.

Enable Input

The enable pin is used to turn the regulator on or off. By holding the pin down to a voltage less than 1.8 V, the output of the regulator will be turned off. When the voltage on the enable pin is greater than 2.8 V, the output of the regulator will be enabled to power its output to the regulated output voltage. The enable pin may be connected directly to the input pin to give constant enable to the output regulator.

Calculating Power Dissipation in a Single Output Linear Regulator

The maximum power dissipation for a single output regulator (Figure 18) is:

$$P_{D(max)} = [V_{I(max)} - V_{Q(min)}]\, I_{Q(max)} + V_{I(max)} I_q \qquad (1)$$

where

$V_{I(max)}$	is the maximum input voltage,
$V_{Q(min)}$	is the minimum output voltage,
$I_{Q(max)}$	is the maximum output current for the application,
I_q	is the quiescent current the regulator consumes at $I_{Q(max)}$.

Once the value of $P_{D(max)}$ is known, the maximum permissible value of $R_{\theta JA}$ can be calculated:

$$R_{\theta JA} = \frac{150^{o}C - T_A}{P_D} \qquad (2)$$

The value of $R_{\theta JA}$ can then be compared with those in the package section of the data sheet. Those packages with $R_{\theta JA}$ less than the calculated value in Equation 2 will keep the die temperature below 150°C.

In some cases, none of the packages will be sufficient to dissipate the heat generated by the IC, and an external heatsink will be required.

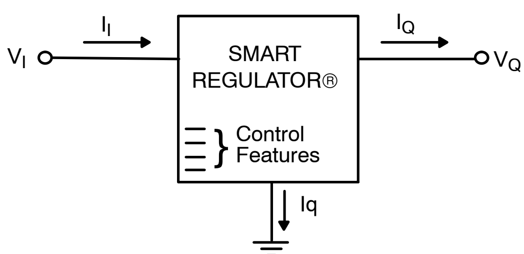


Figure 18. Single Output Regulator with Key Performance Parameters Labeled

Heatsinks

A heatsink effectively increases the surface area of the package to improve the flow of heat away from the IC and into the surrounding air.

Each material in the heat flow path between the IC and the outside environment will have a thermal resistance. Like series electrical resistances, these resistances are summed to determine the value of $R_{\theta JA}$:

$$R_{\theta JA} = R_{\theta JC} + R_{\theta CS} + R_{\theta SA} \qquad (3)$$

where

$R_{\theta JC}$	is the junction−to−case thermal resistance,
$R_{\theta CS}$	is the case−to−heatsink thermal resistance,
$R_{\theta SA}$	is the heatsink−to−ambient thermal resistance.

$R_{\theta JC}$ appears in the package section of the data sheet. Like $R_{\theta JA}$, it too is a function of package type. $R_{\theta CS}$ and $R_{\theta SA}$ are functions of the package type, heatsink and the interface between them. These values appear in data sheets of heatsink manufacturers.

Thermal, mounting, and heatsinking considerations are discussed in the ON Semiconductor application note AN1040/D.

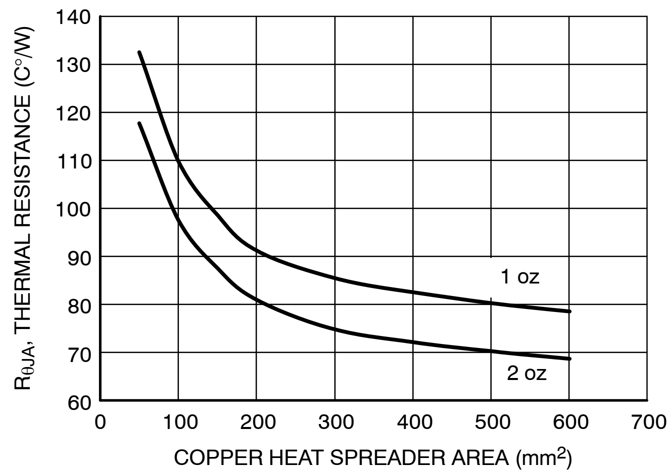


Figure 19. $R_{\theta JA}$ vs. Copper Spreader Area

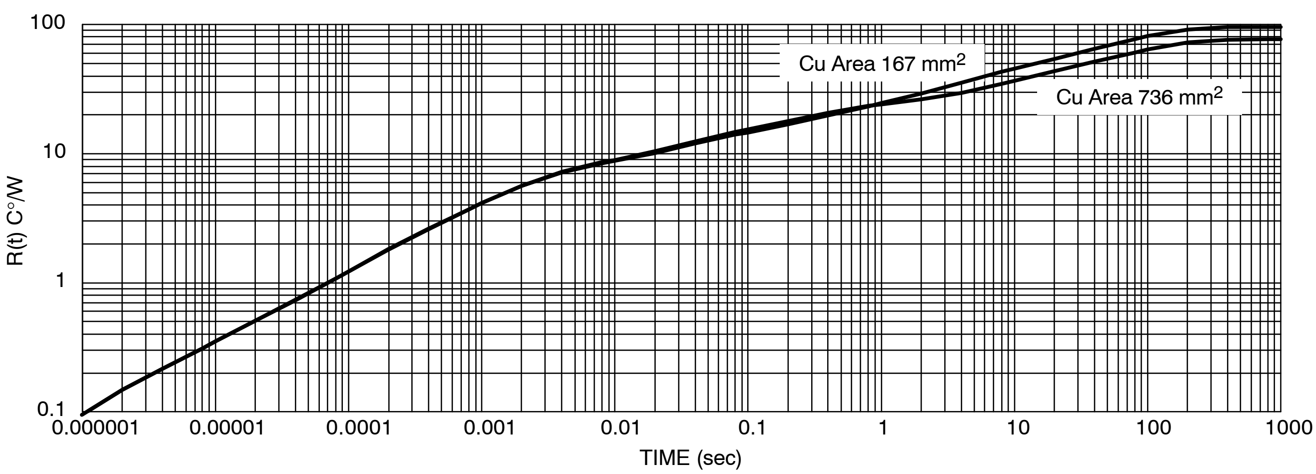


Figure 20. Single−Pulse Heating Curves

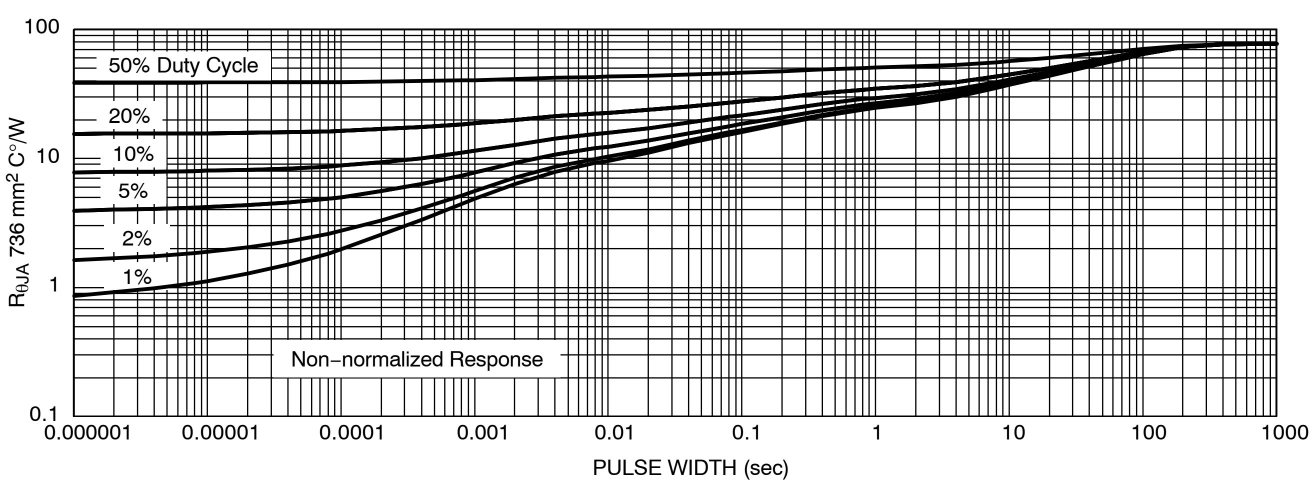


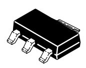
Figure 21. Duty Cycle for 1″ Spreader Boards

ORDERING INFORMATION

Device*	Output Voltage	Package	Shipping†
NCV4266ST33T3G	3.3 V	SOT−223 (Pb−Free)	4000 / Tape & Reel
NCV4266ST50T3G	5.0 V	SOT−223 (Pb−Free)	4000 / Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

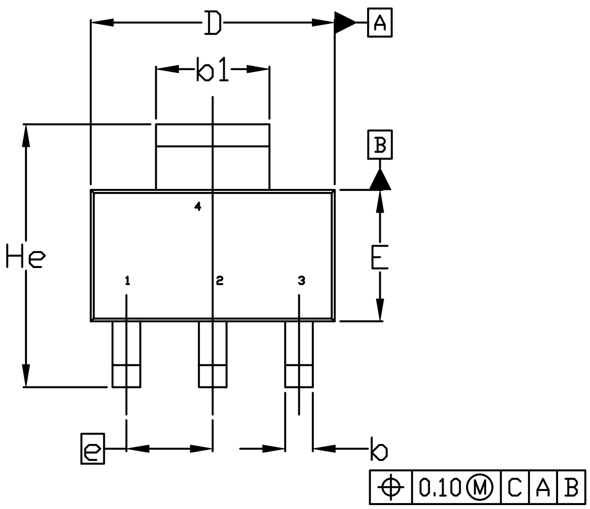
*NCV Prefix for Automotive and Other Applications Requiring Unique Site and Control Change Requirements; AEC−Q100 Qualified and PPAP Capable.



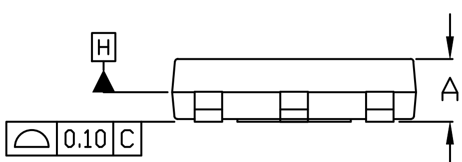
SCALE 1:1

SOT−223 (TO−261)
CASE 318E−04
ISSUE R

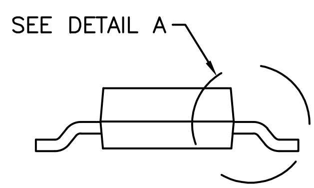
DATE 02 OCT 2018



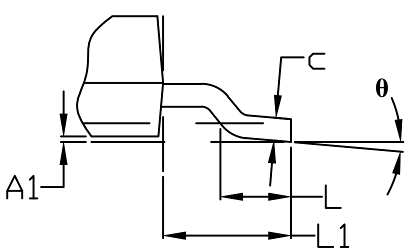
TOP VIEW



SIDE VIEW



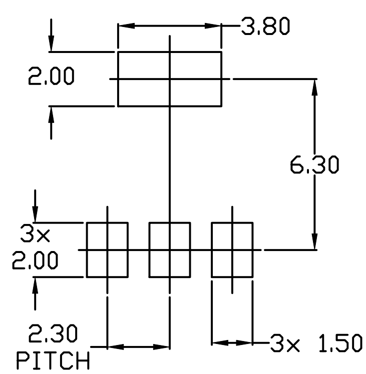
FRONT VIEW



DETAIL A

NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS
3. DIMENSIONS D & E DO NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS. MOLD FLASH, PROTRUSIONS OR GATE BURRS SHALL NOT EXCEED 0.200MM PER SIDE.
4. DATUMS A AND B ARE DETERMINED AT DATUM H.
5. A1 IS DEFINED AS THE VERTICAL DISTANCE FROM THE SEATING PLANE TO THE LOWEST POINT OF THE PACKAGE BODY.
6. POSITIONAL TOLERANCE APPLIES TO DIMENSIONS b AND b1.

	MILLIMETERS		
DIM	MIN.	NOM.	MAX.
A	1.50	1.63	1.75
A1	0.02	0.06	0.10
b	0.60	0.75	0.89
b1	2.90	3.06	3.20
c	0.24	0.29	0.35
D	6.30	6.50	6.70
E	3.30	3.50	3.70
e	2.30 BSC		
L	0.20	---	---
L1	1.50	1.75	2.00
He	6.70	7.00	7.30
θ	0°	---	10°



RECOMMENDED MOUNTING FOOTPRINT

DOCUMENT NUMBER:	98ASB42680B	Electronic versions are uncontrolled except when accessed directly from the Document Repository. Printed versions are uncontrolled except when stamped “CONTROLLED COPY” in red.
DESCRIPTION:	SOT−223 (TO−261)	PAGE 1 OF 2

SOT−223 (TO−261)
CASE 318E−04
ISSUE R

DATE 02 OCT 2018

STYLE 1:
PIN 1. BASE
2. COLLECTOR
3. EMITTER
4. COLLECTOR

STYLE 2:
PIN 1. ANODE
2. CATHODE
3. NC
4. CATHODE

STYLE 3:
PIN 1. GATE
2. DRAIN
3. SOURCE
4. DRAIN

STYLE 4:
PIN 1. SOURCE
2. DRAIN
3. GATE
4. DRAIN

STYLE 5:
PIN 1. DRAIN
2. GATE
3. SOURCE
4. GATE

STYLE 6:
PIN 1. RETURN
2. INPUT
3. OUTPUT
4. INPUT

STYLE 7:
PIN 1. ANODE 1
2. CATHODE
3. ANODE 2
4. CATHODE

STYLE 8:
CANCELLED

STYLE 9:
PIN 1. INPUT
2. GROUND
3. LOGIC
4. GROUND

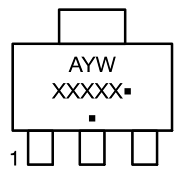
STYLE 10:
PIN 1. CATHODE
2. ANODE
3. GATE
4. ANODE

STYLE 11:
PIN 1. MT 1
2. MT 2
3. GATE
4. MT 2

STYLE 12:
PIN 1. INPUT
2. OUTPUT
3. NC
4. OUTPUT

STYLE 13:
PIN 1. GATE
2. COLLECTOR
3. EMITTER
4. COLLECTOR

GENERIC
MARKING DIAGRAM*



A = Assembly Location
Y = Year
W = Work Week
XXXXX = Specific Device Code
▪ = Pb−Free Package

(Note: Microdot may be in either location)

*This information is generic. Please refer to device data sheet for actual part marking. Pb−Free indicator, “G” or microdot “▪”, may or may not be present. Some products may not follow the Generic Marking.

DOCUMENT NUMBER:	**98ASB42680B**	Electronic versions are uncontrolled except when accessed directly from the Document Repository. Printed versions are uncontrolled except when stamped “CONTROLLED COPY” in red.
DESCRIPTION:	**SOT−223 (TO−261)**	**PAGE 2 OF 2**

PUBLICATION ORDERING INFORMATION

LITERATURE FULFILLMENT:
Email Requests to: orderlit@onsemi.com

onsemi Website: www.onsemi.com

TECHNICAL SUPPORT
North American Technical Support:
Voice Mail: 1 800−282−9855 Toll Free USA/Canada
Phone: 011 421 33 790 2910

Europe, Middle East and Africa Technical Support:
Phone: 00421 33 790 2910
For additional information, please contact your local Sales Representative

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